

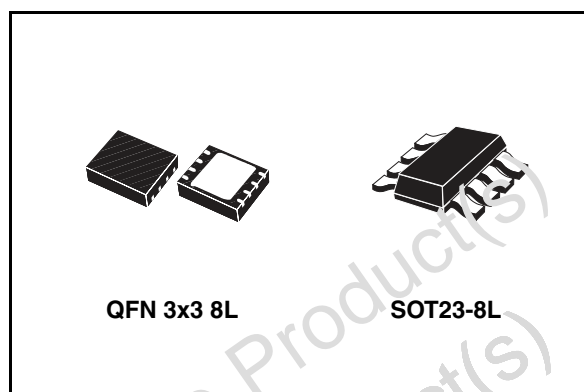
White LED power supply

General features

- Typical guaranteed efficiency: 80%
- Drives up to 4 LEDs in series from a 2.8V up to 4.2V supply voltage
- Constant current regulation over the whole operating voltage range
- PWM control mode
- Integrated load disconnect switch that opens the LEDs path in shutdown mode
- Integrated soft start peak inductor current
- Programmable peak inductor current (STLD20D-C8 only)
- Shutdown pin allows digital dimming control up to 10kHz
- Over voltage and over temperature protection with automatic restart
- Low shutdown current ($< 1\mu\text{A}$)
- Small external inductor (10 μH)
- Tiny external ceramic capacitor (1 μF)

Application

- White LED supply for LCD backlight
- Mobile phone
- PDA and organizers, MP3 players, Toys



Description

The STLD20D is a constant switching frequency boost regulator mainly dedicated to supply up to 4 white LEDs connected in series. A constant LED current is achieved by sensing the LED current through a sensing resistor R_{LED} (see [Figure 3](#)). The device also includes a supply voltage rejection circuit that prevents from any possible flickering effect on the display that might happen during input supply voltage variation. An integrated Load Disconnect Switch open the LED path to eliminate the current consumption in shutdown mode. The maximum peak inductor current can be programmed (STLD20D-C8 only).

Order code

Part number	Package	Marking	Packing
STLD20D-C8	SOT23-8L	L2D	Tape and reel
STLD20D-DEF	QFN 3x3 8L	L2D	Tape and reel

Contents

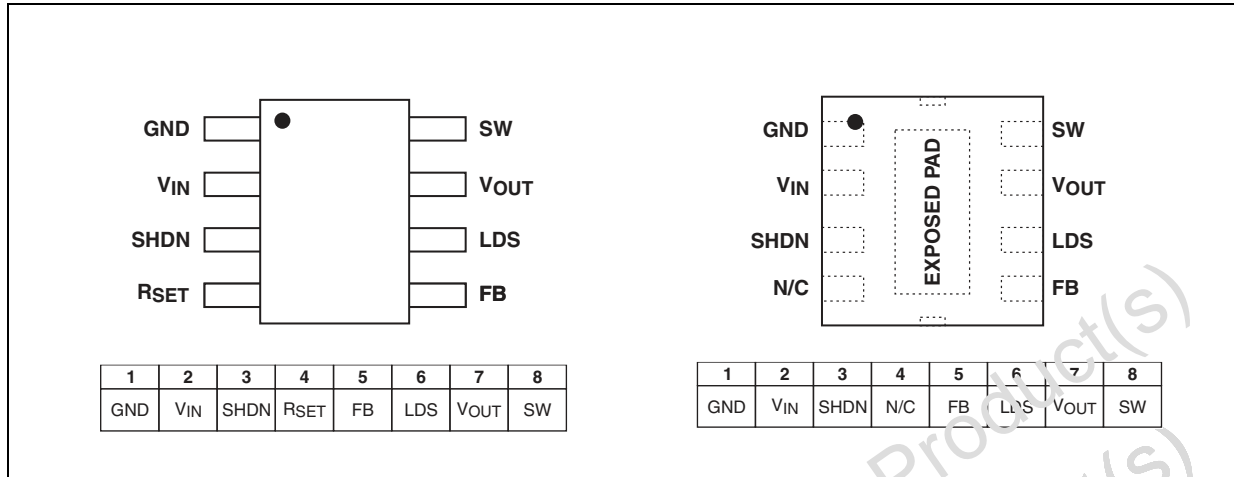
1	Pin description	4
2	Block diagram	5
3	Maximum ratings	7
4	Electrical characteristics	8
5	Functional description	9
5.1	Boost converter	9
5.2	Peak inductor current limitation and soft start function	9
5.3	Peak inductor current programmability (STLD20D-C8 only)	9
5.4	Shutdown	9
5.5	Brightness control	9
5.6	Over temperature protection (OTP)	10
5.7	Over voltage protection (OVP)	10
5.8	Efficiency	10
6	Typical performance characteristics	11
7	Components selection	14
7.1	L, Boost inductor selection	14
7.1.1	Calculation of the inductor value	14
7.1.2	Calculation of the saturation current I(sat)	15
7.1.3	Choice of the R _{SET} resistor	16
7.1.4	Reference selection	16
7.2	C _{IN} and C _{OUT} capacitors selection	17
7.3	1.3. D, Boost diode selection	17
7.3.1	Electrical characteristic	17
7.4	R _{LED} feedback resistance selection	18
7.5	Efficiency	18
8	PWM dimming control	19

9	Analog dimming control	20
9.1	Minimum dimming current	20
9.2	Rd1 Calculation	21
9.3	Rdim calculation for dimming mode control	22
10	Layout recommendation	23
11	Evaluation board	24
12	Package mechanical data	25
13	Revision history	30

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Obsolete Product(s) - Obsolete Product(s)

1 Pin description

Figure 1. Pin configuration (top view)



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2 Block diagram

Figure 2. Block diagram

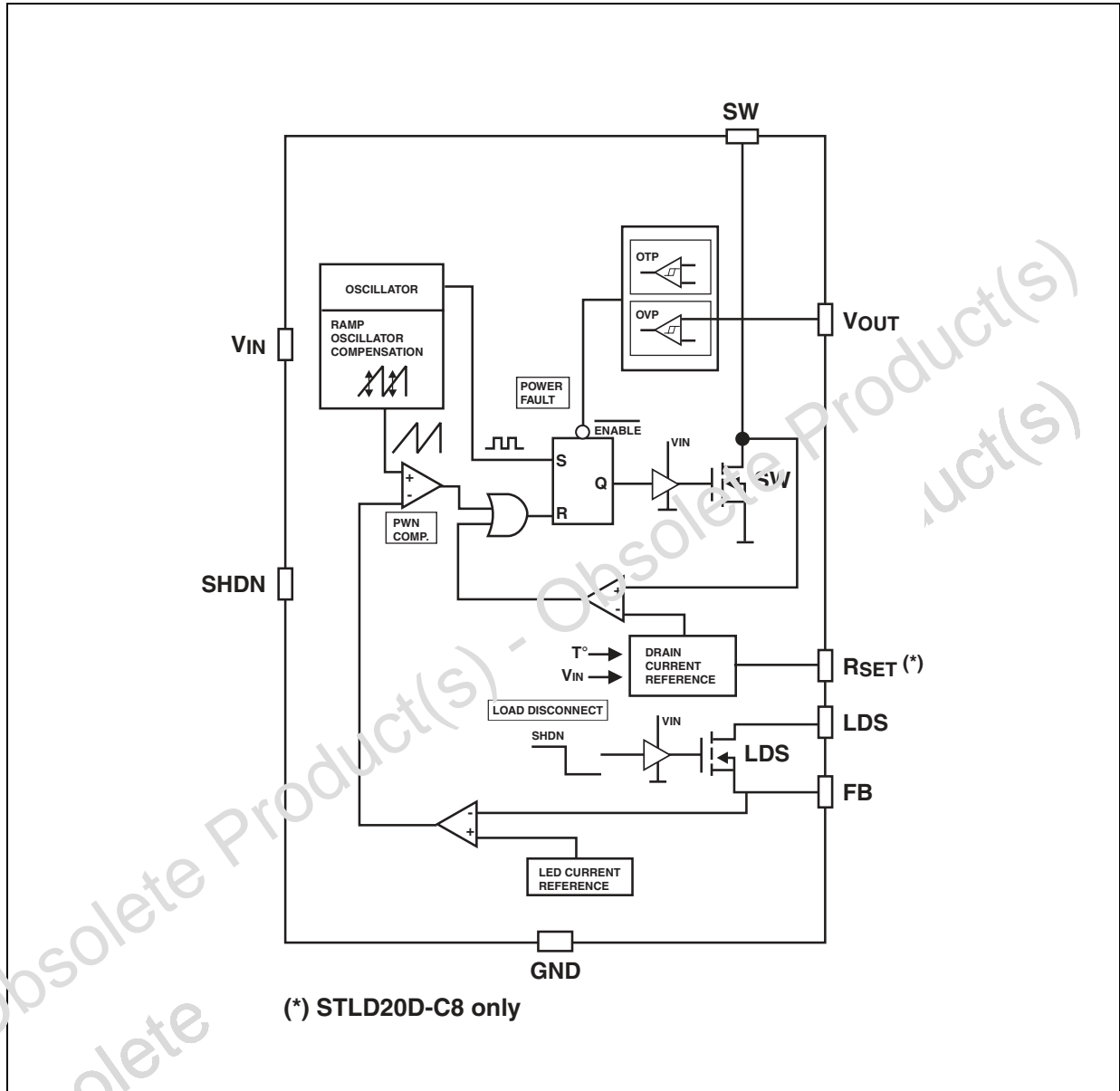


Figure 3. Basic connection

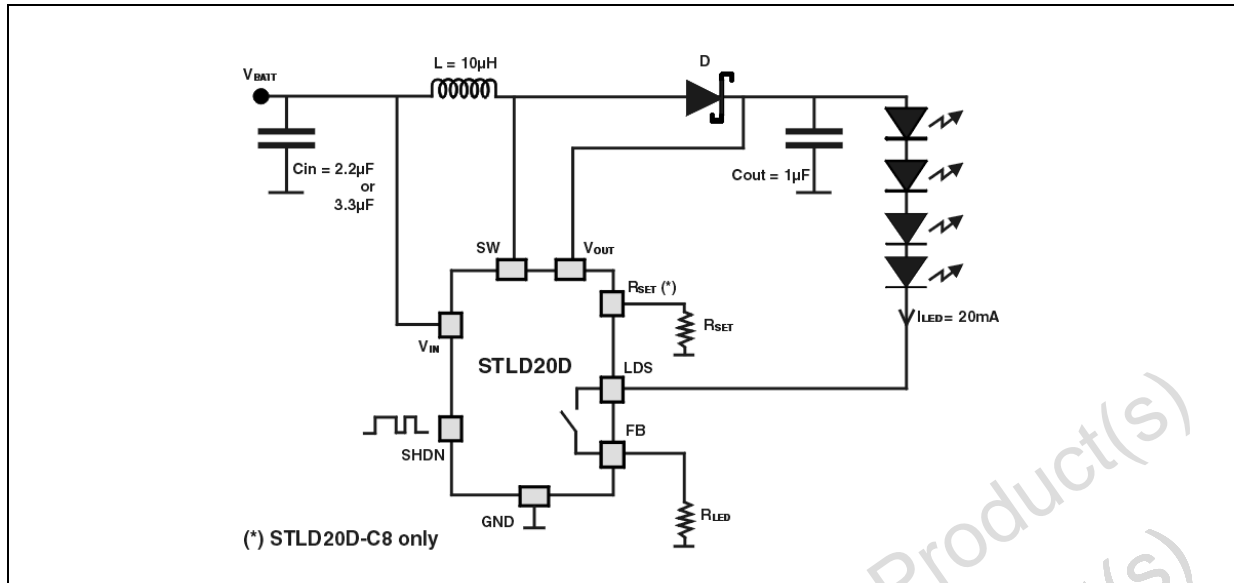


Table 1. External components proposal

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
R_{LED}	LED current resistance			15		Ω
C_{IN}	Input filtering capacitor	Ceramic type		2.2		μF
C_{OUT}	Output capacitance			1		
L	Boost inductor (length < 2mm)	Inductance		10		μH
		Resistance at 500kHz			1	Ω
		I_{SAT} ($R_{SET} = 100k\Omega$)	300			mA
D	Boost diode (STMicroelectronics STPS1L40M type)	V_{RRM}	40			V_{dc}
		I_F (peak forward current)		1		A
		$V_F @ I_F = 1A \quad T_j = 25^\circ C$		0.40	0.46	V

Note: The external components proposal should be considered as a design reference guide. The performances mentioned in the electrical characteristics table are not guaranteed for all the possible electrical parameters of the components included in this list. On the other hand the operation of STLD20D is not limited with the use of components included in this list.

3 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
V _{IN}	Supply voltage range		2.5		5	V
V _{ESD}	ESD ratings	HBM MIL STD 883C	2			kV
T _{OP}	Operating temperature		- 40		+ 85	°C
T _{stg}	Storage temperature		- 65		150	°C
B _{VDS}	Breakdown voltage at pin SW and TSS and V _{OUT}		20			V
SHDN	Maximum voltage applied on SHDN pin				V _{IN}	V

Table 3. Thermal data

Symbol	Parameter		Value			Unit
			Min.	Typ.	Max.	
R _{thJA}	Mounted on epoxy board without copper heatsink	SOT23-6L			300	°C/W
		QFN			350	

4 Electrical characteristics

Table 4. Electrical characteristics ($V_{IN} = 2.8$ to $4.2V$ and $T_J = 25^\circ C$)

Symbol	Parameter		Test conditions		Value			Unit
					Min.	Typ.	Max.	
V_{IN}	Operating Input voltage range				2.8		4.2	V
I_{LED}	Average regulated current $I_{LED} = 20mA$ $R_{LED} = 15\Omega$				19	20	21	mA
I_{SD}	Stand-by current		SHDN = low $V_{IN} = 4.2V$				1	μA
I_Q	Quiescent current consumption		SHDN = high $V_{IN} = 4.2V$			0.43	0.6	mA
SW	Boost switch R_{DSON}	SOT23-8L	$T_J = 25^\circ C$ $I_{SW} = 250mA$	$V_{IN} = 2.8V$		0.48	Ω	
				$V_{IN} = 4.2V$		0.33		
		QFN	$T_J = 25^\circ C$ $I_{SW} = 250mA$	$V_{IN} = 2.8V$		0.57		
				$V_{IN} = 4.2V$		0.42		
LDS	Load Disconnect Switch R_{DSON}	SOT23-8L	$T_J = 25^\circ C$ $I_{LDS} = 20mA$	$V_{IN} = 2.8V$		5.0	Ω	
				$V_{IN} = 4.2V$		4.2		
		QFN	$T_J = 25^\circ C$ $I_{LDS} = 20mA$	$V_{IN} = 2.8V$		5.1		
				$V_{IN} = 4.2V$		4.3		
FB	Feedback voltage				0.285	0.302	0.315	V
Line	Variation of the LED current versus the input voltage: $R_{LED} = 15\Omega$						0.9	mA/V
Eff	Efficiency with 4 LEDs, $V_{OUT} = 16V$		$V_{IN} = 2.8V$		80			%
			$V_{IN} = 4.2V$			85		
f_{SW}	Switching frequency				400	500	600	kHz
DC_{MIN}	Minimum duty cycle					20		%
I_{LIM}	Peak current boost switch ⁽¹⁾		$L = 10\mu H$ $R_{SET} = GND$ (STLD20D-C8)				640	mA
CVP	Overvoltage protection				17.5	18.5	20	V_{DC}
Hyst _{OV}	Overvoltage hysteresis					0.7		V_{DC}
OTP	Over temperature protection				110			$^\circ C$
Hyst _{OT}	Over temperature protection hysteresis					5		$^\circ C$
SHDN	Shutdown signal logic		Disable Low V_{IL}				0.3	V
			Enable high V_{IH}		1.2			

1. Guaranteed by design.

5 Functional description

5.1 Boost converter

The STLD20D is a PWM mode control boost converter operating at 500kHz.

An automatic compensation of the oscillation ramp allows rejection of the battery voltage transient. The LED current regulation (see [Figure 3](#).) is done by sensing the LED current through the resistance R_{LED} . The voltage across R_{LED} is used by the feedback loop of the controller (FB pin).

5.2 Peak inductor current limitation and soft start function

An integrated current sensor limits the switching current at 640 mA maximum.

Should the peak drain current exceed 640mA (if $R_{SET} = 0$ for STLD20D-C2) the flip flop will turn off the switch SW. During start up, this peak drain current limitation acts like a soft start function.

5.3 Peak inductor current programmability (STLD20D-C8 only)

The converter peak current must be always below the inductor saturation current. For flexibility reasons, the maximum peak inductor current can be programmed by connecting a resistor at the pin R_{SET} .

The [Figure 12](#) gives the value of the resistance R_{SET} versus the peak inductor current limit I_{LMAX} .

5.4 Shutdown

The SHDN pin is a low logic input signal and allows turning off the controller without cutting the input voltage from the boost regulator circuit.

An integrated Load Disconnect Switch LDS disconnects the LEDs branch in shutdown mode. This arrangement allows eliminating the DC current path that normally exists with traditional boost regulator in shutdown mode.

5.5 Brightness control

The brightness of the LED is adjusted by pulsing the shutdown pin with a PWM signal as high as 10kHz.

By using such a PWM signal the controller is alternatively ON and OFF and the LED current changes from full current to zero.

The duty cycle allows regulating the average LED current. This scheme ensures that when the LEDs are ON, they are driven at the full current without risk of color change.

5.6 Over temperature protection (OTP)

An integrated temperature sensor senses the temperature of the junction of the controller. As soon as this temperature exceeds 110°C min fixed internally, the controller is automatically turned OFF. When the temperature is reduced of 5°C the operation of the device automatically recovers.

5.7 Over voltage protection (OVP)

In case of failure and if the LED branch is cut, then there is no signal at the feedback pin FB ([Figure 3.](#)), the PWM controller will then switches with a maximum duty cycle. This will generate a voltage at the pin SW and V_{OUT} that can exceed the maximum rating of the device.

The overvoltage protection block senses the output voltage at the pin V_{OUT} ([Figure 3.](#)). If the voltage exceeds 18.5V_{DC} typical the controller is automatically turned OFF.

When the voltage is reduced of 0.7V, the operation of the device automatically recovers.

5.8 Efficiency

([Figure 4.](#) & [Figure 9.](#))

The efficiency takes into account these following losses:

- R_{LED} ohmic losses
- Boost switch SW losses
- Load Disconnect Switch LLS
- Boost inductor losses
- Boost diode losses

6 Typical performance characteristics

Figure 4. 4 LEDs efficiency measurement

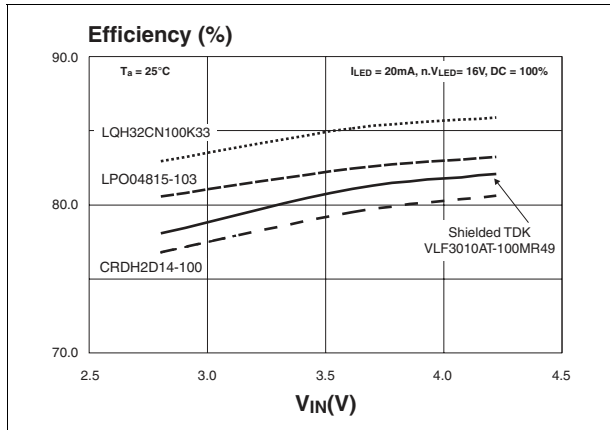


Figure 5. LED current vs input voltage

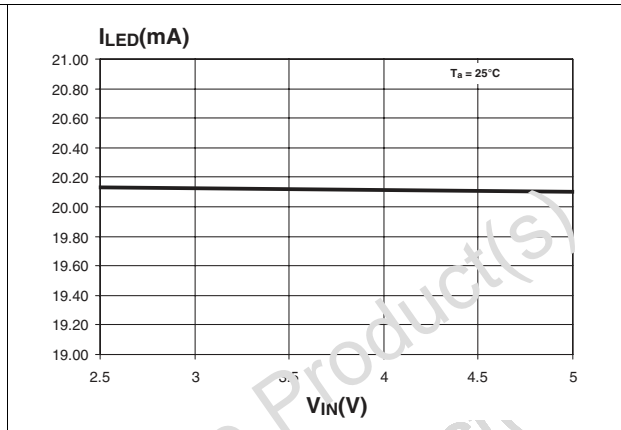


Figure 6. Feedback voltage

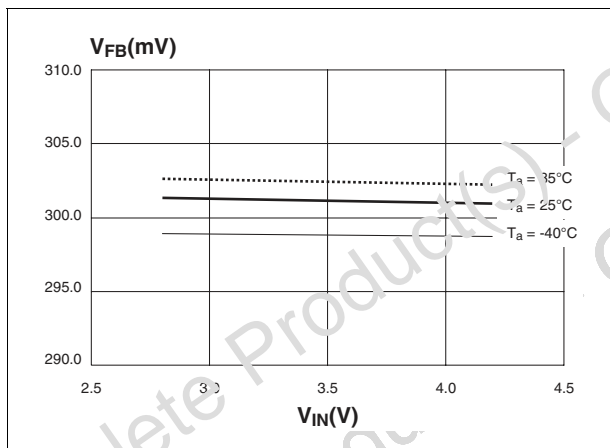


Figure 7. Boost switch resistance (STLD20D-C3)

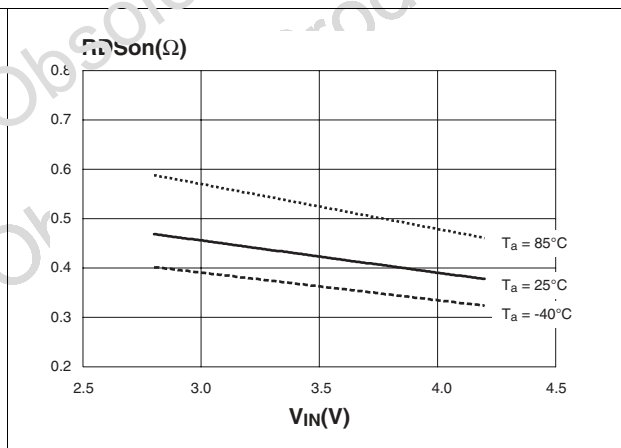


Figure 8. Boost switch resistance (STLD20D-DEF)

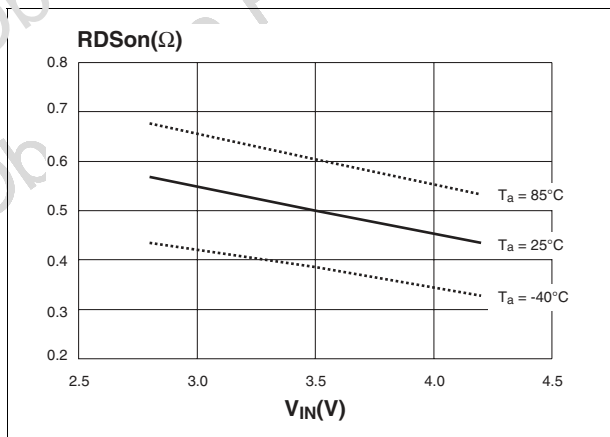


Figure 9. Efficiency vs input voltage (ILED=20mA; TA=25°C)

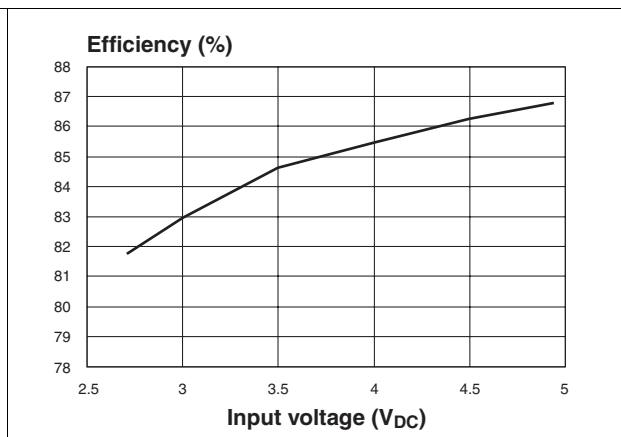


Figure 10. Load disconnect switch resistance Figure 11. Quiescent Current consumption

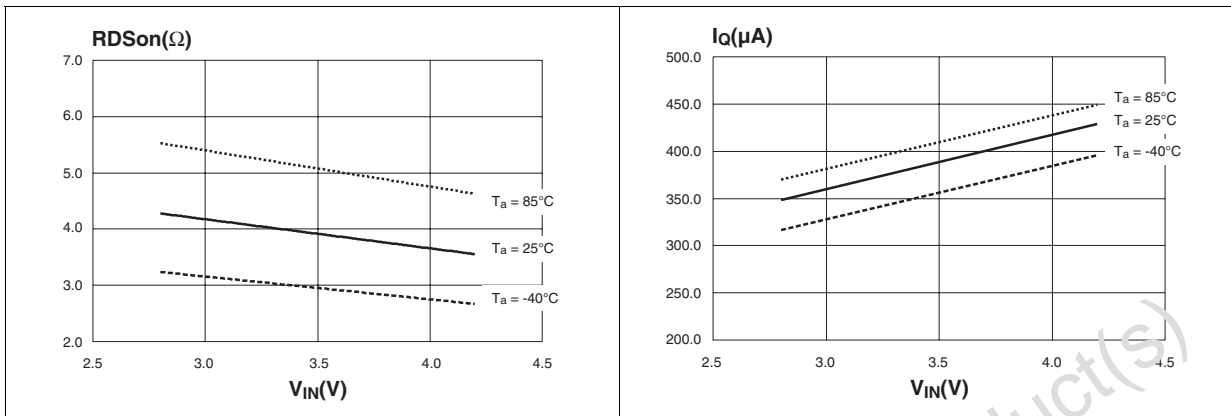


Figure 12. Max peak inductor current IL versus L and RSET Figure 13. Max peak inductor current IL versus RSET

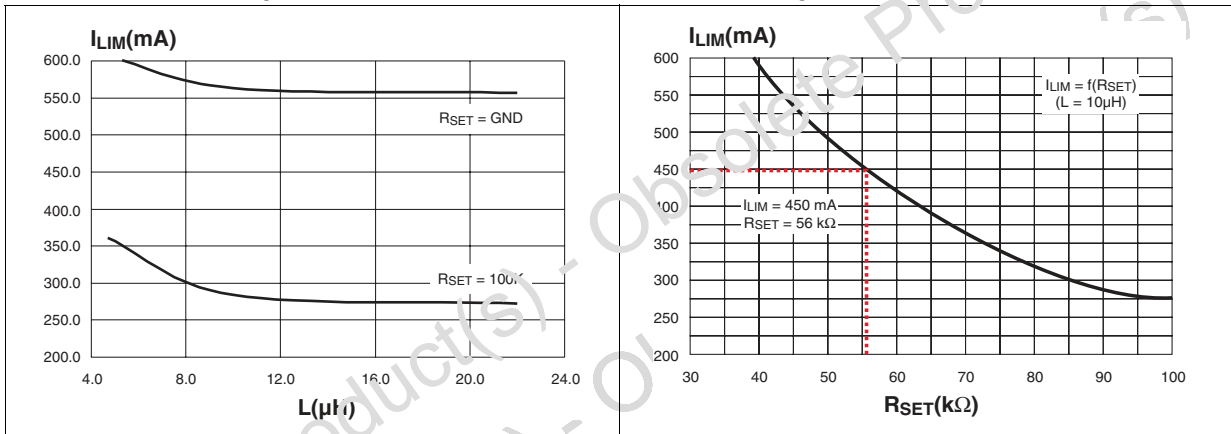


Figure 14. ILED versus duty cycle

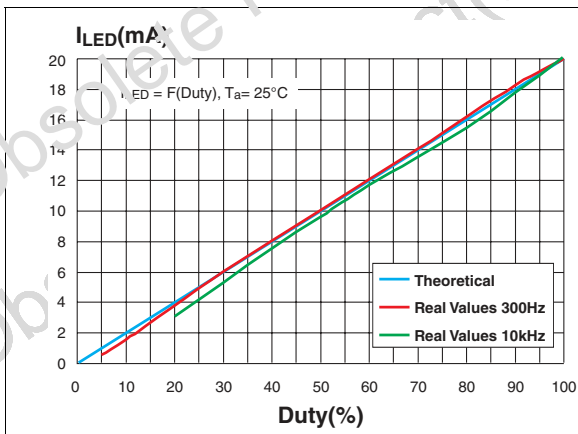


Figure 15. Typical waveform

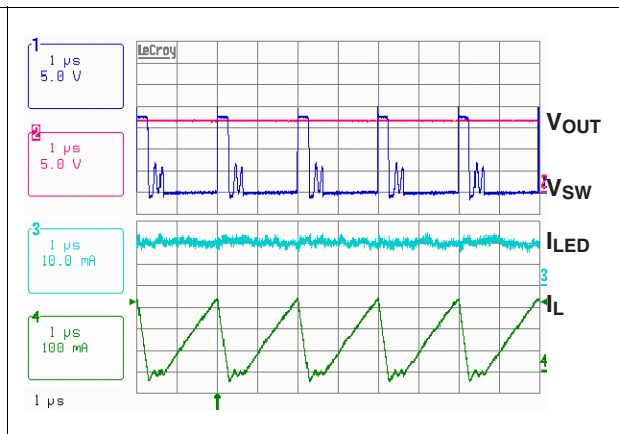


Figure 16. Supply voltage rejection

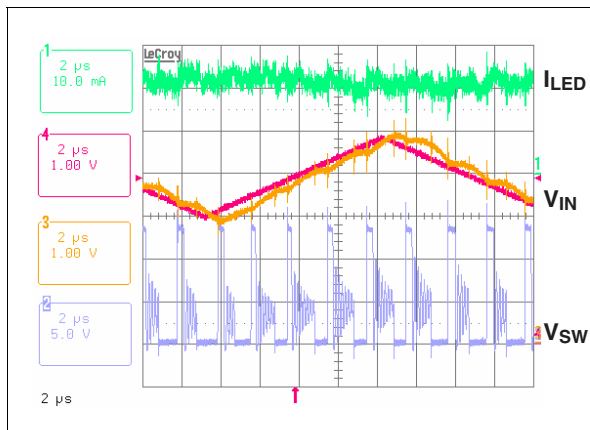
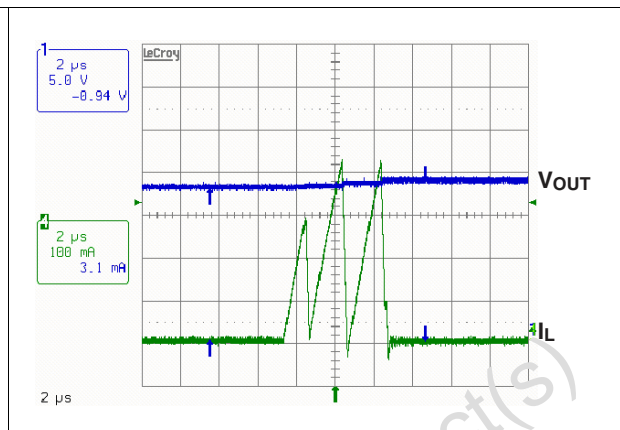


Figure 17. Overvoltage protection



7 Components selection

7.1 L, Boost inductor selection

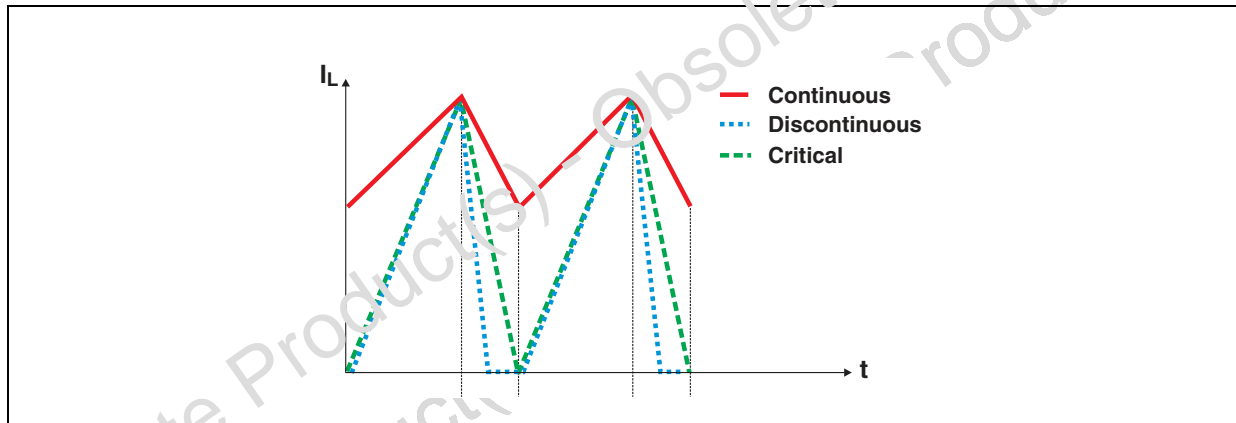
To get a good trade-off thickness/efficiency, an attention must be given on the inductor choice.

- The inductance value must be selected to remain in the discontinuous conduction mode.
- Its saturation current (I_{sat}) must be equal or higher than the programmed current (I_{LIM}).
- An attention must be taken on the dynamic inductor parameters. Actually, some power losses can occur in the boost inductor when it works at several hundred KHz and can reduce the efficiency.

7.1.1 Calculation of the inductor value

The inductor must be dimensioned so that the STLD20D stays running in discontinuous conduction mode operation in the worst operation condition ($V_{IN} = V_{in(min)} = 2.8V$). The limit between continuous and discontinuous mode is called critical mode and characterized by an uninterrupted current through the inductor (see figure 18).

Figure 18. 3 different conduction modes



The formula [1] gives the maximum typical value of the inductor for a discontinuous mode operation in the worst case condition (critical mode). Figure 19 shows the typical L value versus the voltage across the LED branch $N \cdot V_{LED}$. Note that this curve includes the STLD20D and inductance dispersions (20%).

$$N \cdot V_{LED} = 4 \times 4V = 16V \text{ and } I_{LOAD} = 20mA$$

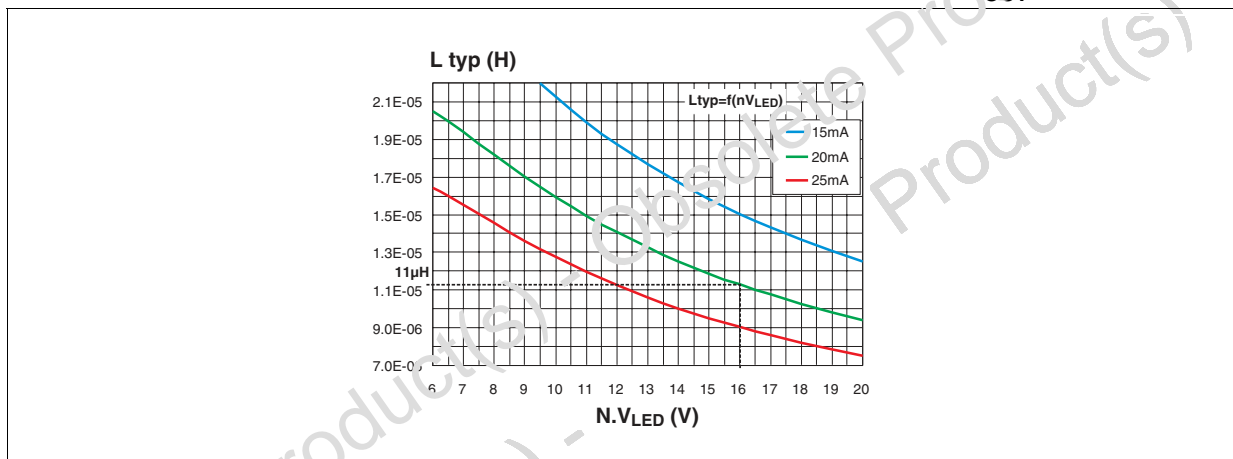
$$L_{typ} \leq \frac{\eta \cdot V_{in(min)}^2 (N \cdot V_{LED} - V_{in(min)} + V_{FB} + I_{LED} \cdot R_{LDS})}{2.4 \cdot I_{LED} \cdot N \cdot V_{LED} \cdot F_{max} \cdot (N \cdot V_{LED} + I_{LED} \cdot R_{LDS})} \quad [1]$$

Where:

- η is the efficiency (80%)
- N is the number of the white LEDs in series
- V_{LED} is the forward voltage of the LED for the I_{LED} current ($V_{LED} = 4V$ in our example)
- $V_{IN(min)}$ is the minimum input voltage (2.8V)
- V_{FB} is the error amplifier reference (0.3V)
- R_{LDS} is the internal resistance of the Load Disconnect Switch power MosFET (6 Ω)
- F_{max} is the maximum frequency of the STLD20D (600kHz)
- I_{LED_MAX} is the current through the LED

For example, the case with 4 white LEDs can be considered in order to evaluate L value in the worst case conduction.

Figure 19. Typical inductance value versus the white LED voltage for three I_{OUT}



From figure 19, typical inductance must be lower than 11 μ H. By minimizing the inductance to ensure the discontinuous mode operation, the standard coil value is equal to 10 μ H. Then: $L = 10\mu$ H

7.1.2 Calculation of the saturation current $I_{(sat)}$

The maximum peak current ($I_{p(max)}$) during steady state can be estimated by the formula [2]:

$$I_{p(max)} = \sqrt{\frac{2 \cdot I_{LED} \cdot N \cdot V_{LED} \cdot (N \cdot V_{LED} - V_{IN(min)} + V_{FB} + I_{LED} \cdot R_{LDS})}{\eta \cdot F_{min} \cdot 0.8 \cdot L_{typ} \cdot (N \cdot V_{LED} + V_{FB} + I_{LED} \cdot R_{LDS})}} \quad [2]$$

Where:

- L_{typ} is the typical inductance value
- F_{min} is the minimum frequency due to the STLD20D spread-off (400kHz)

Figure 20. Maximum peak current ($I_{p(max)}$) versus the white LEDs voltages for 3 outputs current - $V_{IN} > 2.8V$

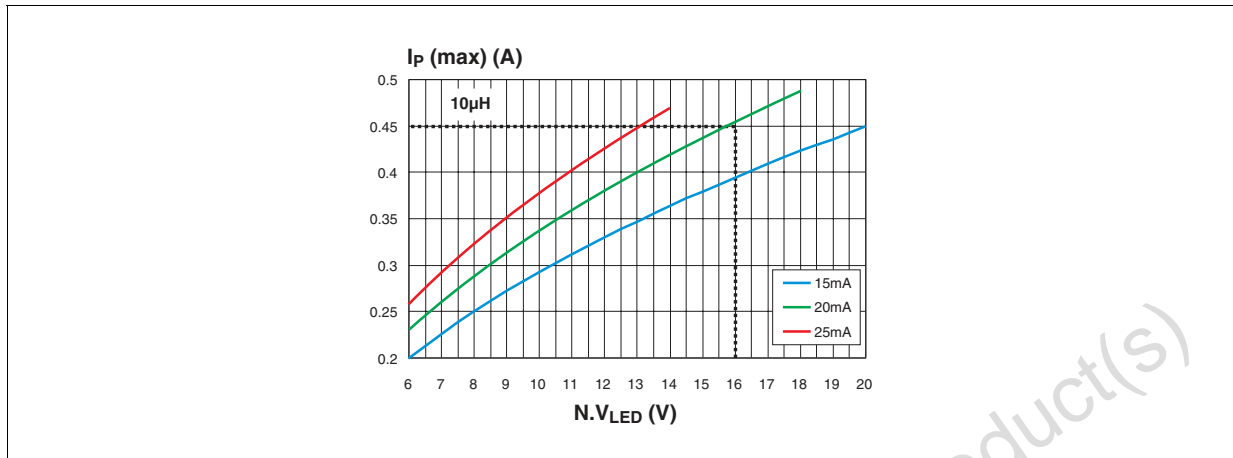


Figure 20 shows the maximum peak current $I_{p(max)}$ through the coil for $L=10\mu H$ versus the voltage across the LED branch, $N.V_{LED}$ and the LED current I_{LED} for $V_{IN} > 2.8V$. As $N.V_{LED} = 16V$ and $I_{LED} = 20mA$, then $I_{p(max)} = 0.45A$. The curve below ends when the converter reaches the critical mode operation.

Therefore, the saturation current (I_{sat}) of the inductor must be higher than 0.45A. To conclude:

$$I_{sat} \geq I_{p(max)}$$

$$I_{sat} \geq 0.4A$$

7.1.3 Choice of the R_{SET} resistor

The resistor R_{SET} fixes the maximum peak current flowing through the inductor whatever the operating conditions. Thus, current saturation (I_{sat}) is never reached. If the height constraint is important, this function allows using low profile inductor with a small saturation current.

The [Figure 12](#) on page 12 gives the corresponding typical value of the external resistor R_{SET} versus the I_{LIM} value. This curve is slightly dependent of the temperature and the input voltage.

To prevent the coil saturation R_{SET} must be equal to 56k Ω , see [Figure 12](#). Thus:

$$I_{sat} \geq I_{LIM} \geq I_{p(max)}$$

7.1.4 Reference selection

The table below gives some coil references suitable for the STLD20D versus L, DCR, I_{sat} value and sizing requirements.

Table 5. Reference selection

Name	Ref	Height (mm)	L typ (μH)	DCR (Ω)	I_{SAT} (A)
Murata	LQH32CN4R7M33	2	4.7	0.15	0.65
	LQH32CN100K33	2	10	0.3	0.45
	LQH32CN4R7M53	1.55	4.7	0.15	0.65
	LQH32CN100K53	1.55	10	0.3	0.45
Coilcraft	LP04815-472MXC	1.5	4.7	0.15	0.77
	LP04815-103MXC	1.5	10	0.23	0.55
Würth Elektronik (WE)	744031100	1.65	10	0.205	0.74
	744031150	1.65	15	0.285	0.62
	744042100	1.8	10	0.15	1.3
Sumida	CDRH2014-100	1.855	10	0.294	0.7
	CLS4D14	1.5	6.8	0.13	0.8
	CLS4D14	1.5	10	0.18	0.65
TDK	VLF3010AT 100HR49 shielded	10	10	0.67	0.49

7.2 C_{IN} and C_{OUT} capacitors selection

The capacitance values and its intrinsic resistance (ESR) must be selected in order to reduce the output ripple

The ceramic capacitor technology offers the best compromise between the space and the performance (low ESR, value, voltage rating). Nevertheless, their values changes with the time as well as with temperature, DC bias voltage and switching frequency. Thus it might be necessary to use higher capacitor value if low ripple is an absolute need.

7.3 1.3. D, Boost diode selection

The diode selection is based upon two major criteria:

- Low losses to get the best converter efficiency
- Mechanical size

7.3.1 Electrical characteristic

V_{RRM} (Repetitive peak reverse voltage) is the first parameter to consider in the selection of the boost diode. Its value must be always higher than the reverse voltage (V_{R}) occurring during the steady state. Note that, some transient voltages occurs during the commutation period due to the leakage inductance of the PCB. Generally, a power diode with a maximum reverse voltage equal or just higher than 20V suits perfectly. Therefore a Schottky diode technology can be used.

Schottky diode has a low forward voltage, nevertheless they have an additional reverse current which provides additional losses at high ambient temperature.

In fact, in boost backlighting converter, the conduction losses (P_{cond}) lead by the forward characteristics can be negligible compared to the losses induced by the reverse current (P_{rev}), especially at high temperature.

7.4 R_{LED} feedback resistance selection

The average output current is regulated by sensing a low external ohmic sensing resistor R_{LED} . Thus, a constant current value is fixed for each LED whatever the ambient temperature conditions. R_{LED} is given by:

$$R_{\text{LED}} = \frac{V_{\text{FB}}}{I_{\text{LED}}} = \frac{0.3\text{V}}{20\text{mA}} = 15\Omega \quad [7]$$

7.5 Efficiency

Efficiency is a significant parameter for the application. The higher the efficiency, the longer the life time of the battery. The efficiency is given by:

$$\text{Efficiency} = \frac{P_{\text{output}}}{P_{\text{input}}} = \frac{N \cdot V_{\text{LED}} \cdot I_{\text{LED}}}{V_{\text{IN}} \cdot I_{\text{input}}} \quad [8]$$

9 Analog dimming control

Some application are sensitive to low frequency dimming signal; in this case an analog dimming control technic with a DC voltage V_{dim} to control the brightness of the LED can be used with the circuit shown [Figure 22](#).

The formula below gives the LED current versus the dimming voltage V_{dim} :

$$I_{LED} = \frac{V_{FB} \cdot (R_{dim} + R_{d1} + R_{LED}) - V_{dim} \cdot (R_{LED} + R_{d1})}{R_{dim} \cdot R_{LED}} \quad [19]$$

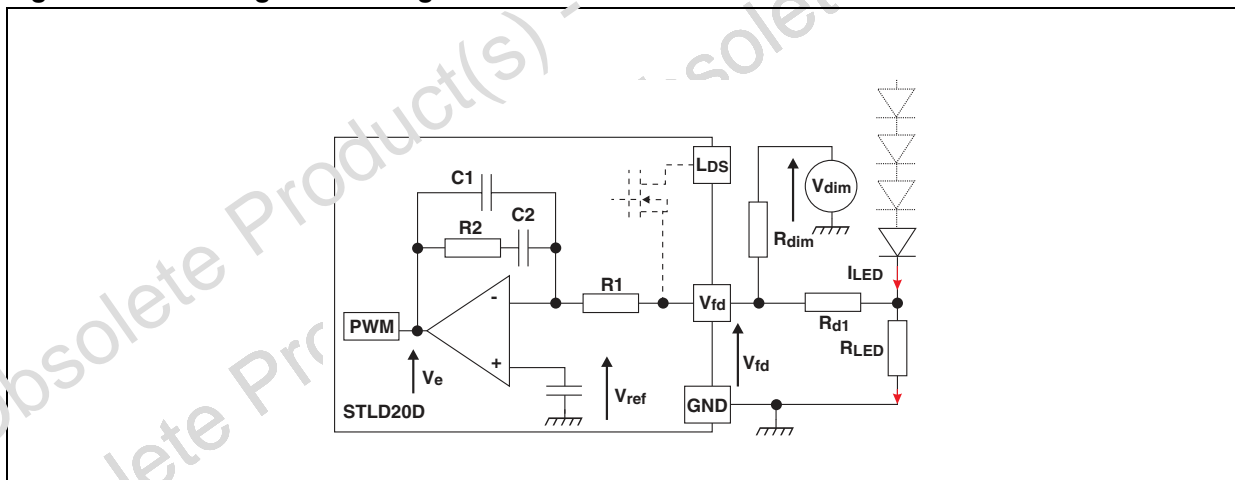
Where:

- V_{dim} : Analog Dimming Voltage
- R_{dim}, R_{d1} : Resistors of the dimming circuit (see figure 26)

9.1 Minimum dimming current

The PWM control of the STLD20D has a minimum duty cycle DC_{MIN} that limits the dimming current range. It exists a minimum dimming current I_{LEDC} corresponding to the typical DC_{MIN} of the control loop.

Figure 22. Analogical dimming schematics



This minimum dimming current depends on the maximum input voltage and the forward voltage of the LED and can be estimated by:

$$I_{LEDC} \approx \frac{(DC_{min} \cdot V_{IN(max)})^2}{2 \cdot L_{typ} \cdot F_{typ} \cdot [N \cdot V_{LED} + V_{FB} - V_{IN(max)}]} \quad [20]$$

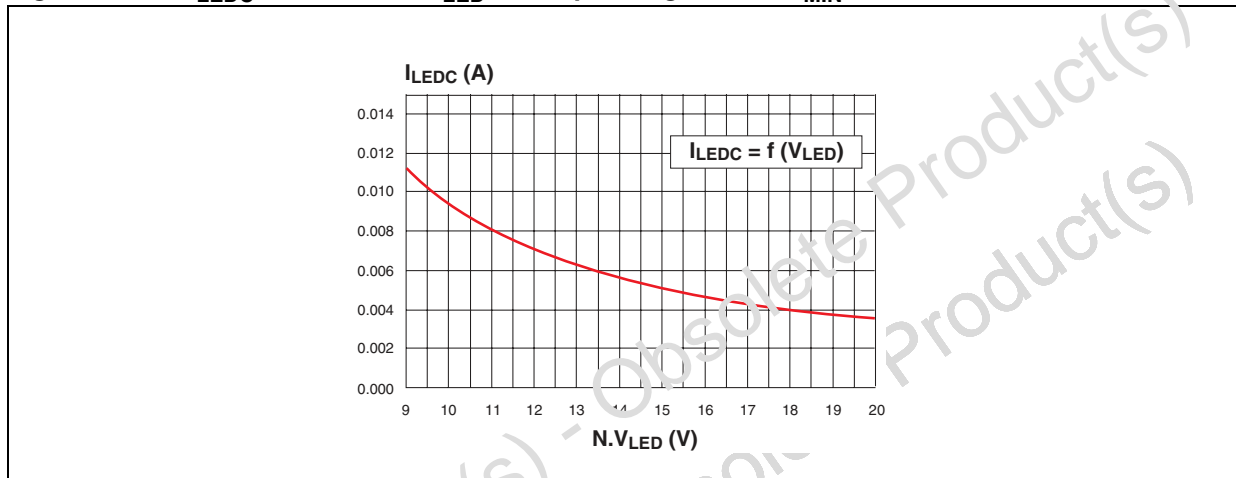
Where:

- $V_{IN(max)}$: is the maximum input voltage
- DC_{MIN} : is the typical minimum duty cycle of the STLD20D (18%)
- L_{typ} : is the typical value of the inductance
- F_{typ} : is the typical switching frequency

Figure 23. gives the I_{LED} versus the LED branch voltage $N.V_{LED}$. This curve is calculated with:

$$L_{typ} = 10\mu H, F_{typ} = 500kHz, DC_{MIN} = 18\% \text{ and } V_{IN(max)} = 4.2VDC.$$

Figure 23. I_{LEDC} current vs $N.V_{LED}$ corresponding at the DC_{MIN}



Higher the voltage across the branch LEDs, higher the range current control. After these considerations, it is described here the basics rule to help the designer to choose the external components such as R_{d1} , R_{dim} and R_{LED} versus V_{dim} and brightness control current I_{LED} .

9.2 R_{d1} Calculation

To avoid significant shifting of the cross over frequency and to keep enough high the corrector network gain of the error amplifier, it is recommended to dimension the resistor R_{d1} below $10k\Omega$ (10% of R_1).

Dimension R_{LED} for full brightness operating mode

R_{LED} is dimensioned to get the nominal current I_{LED} for the full brightness of the LED.

It is recommended to fix $V_{dim} = V_{FB}$ during the full brightness operating mode so that the LED current correspond to the programmed value I_{LED} . Thus:

$$R_{LED} = \frac{V_{FB}}{I_{LED}} \quad [21]$$

Where:

- V_{FB} is the feedback voltage
- I_{LED} is the LED current for full brightness

Note: If V_{dim} is equal to 0 the LED current can be higher the programmed value.

9.3 R_{dim} calculation for dimming mode control

R_{dim} and R_{d1} are dimensioned to get a current in the dimming circuit much smaller than the LED current. From the formula 19, R_{dim} can be calculated by:

$$R_{dim} = \frac{[R_{d1} + R_{LED}] \cdot [V_{FB} - V_{dim-max}]}{I_{LEDmin} R_{LED} - V_{FB}} \quad [22]$$

Where:

- V_{dimmax} is the maximum dimming voltage
- I_{LEDmin} is the expected minimum dimming current

10 Layout recommendation

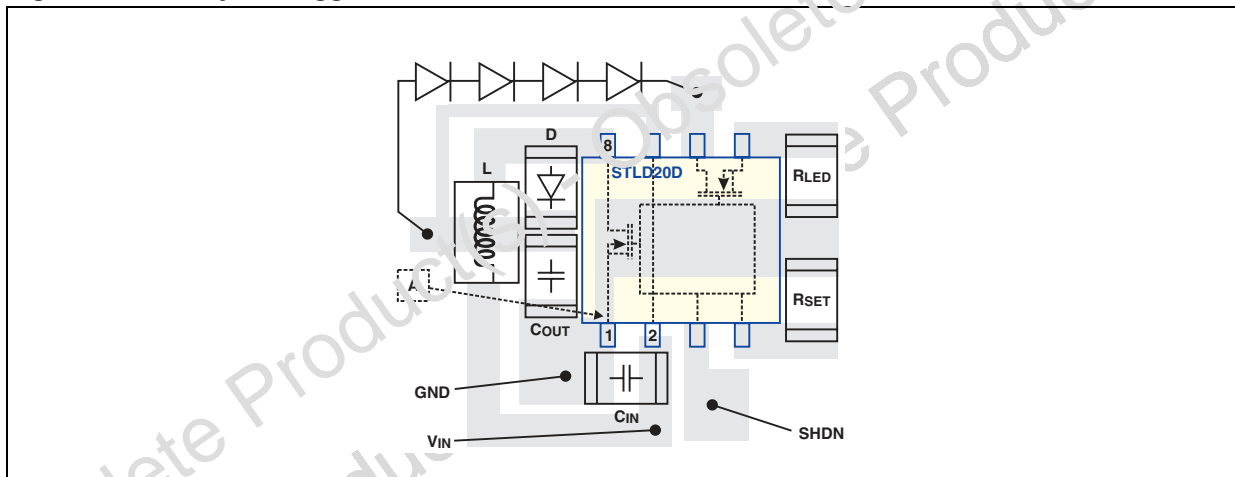
The package connection of the STLD20D has been realized in order to facilitate the layout of the PCB. The golden rule to obtain an optimized layout is to split the power and signal track as shown on the [Figure 24](#).

It is necessary to place the input capacitor as closed as possible between pin1 and pin2 of the STLD20D package. If the C_{IN} capacitor is not closed to the device, high frequency noise due to gate driver dI/dt flows through the copper track of the board and can generate some line voltage drop due to the line inductance.

For the same reason, in order to eliminate high frequency current loop, the connection of the diode (D) and the output capacitor (C_{OUT}) must be as close as possible to the internal power MosFET (SW) (close to pin 8 and 1).

Concerning the signal path, we recommend to create the PCB GND signal from the pin 1 ("A" point in the [Figure 24](#)). Thus all signal references such as feedback and tie voltage across R_{set} are not disturbed by the power stage.

Figure 24. Layout suggested



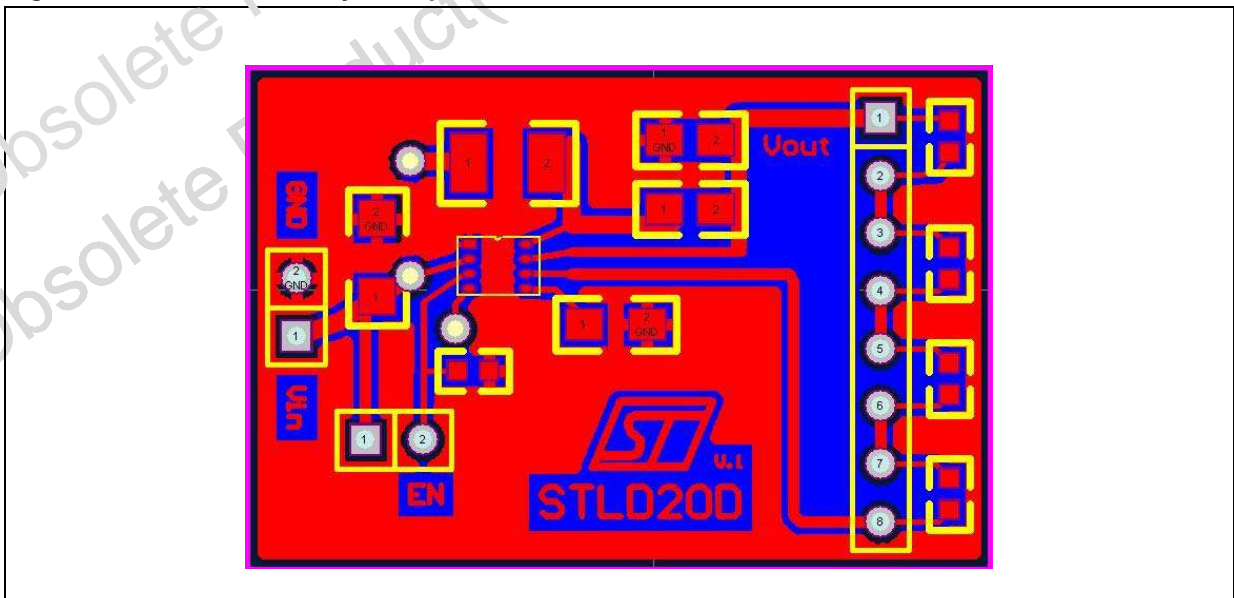
11 Evaluation board

Figure 25. shows the top view of the evaluation board that show all the application features of the STLD20D.

Figure 25. Evaluation board top view with its connections at the external equipment



Figure 26. Demo board layout top view



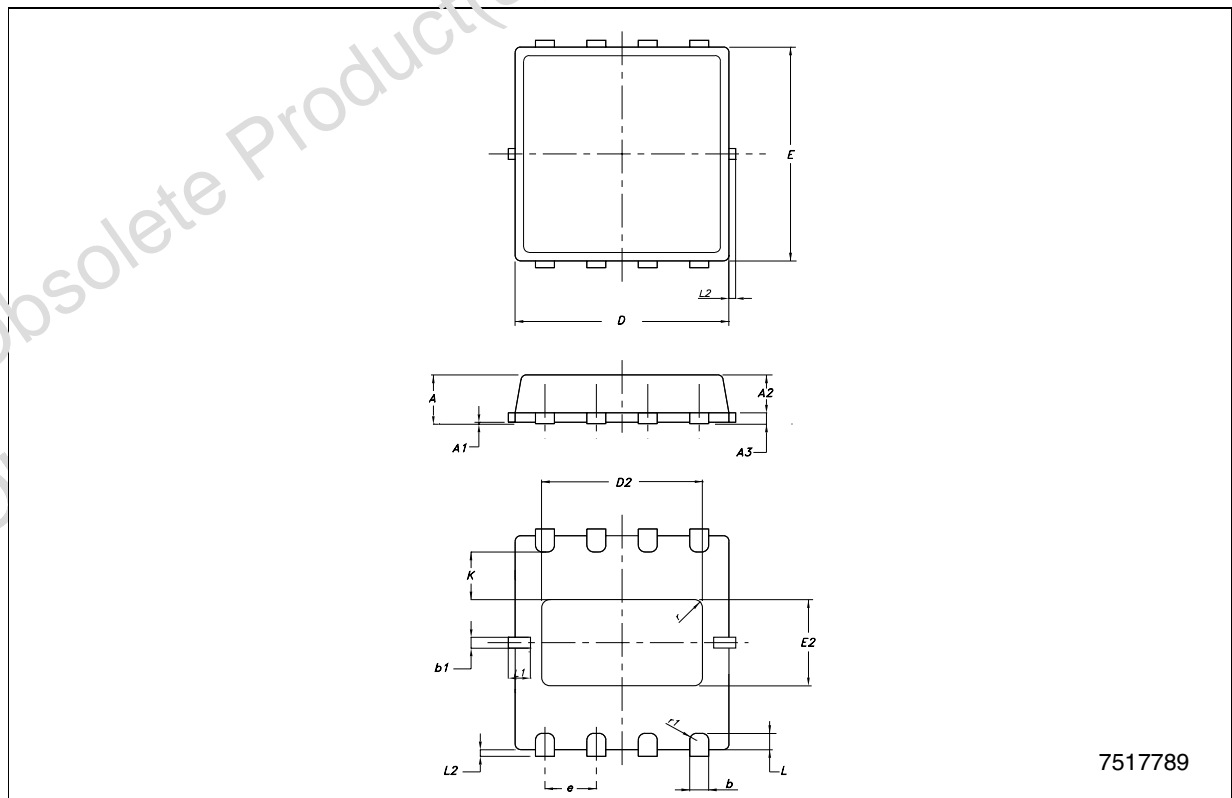
12 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Obsolete Product(s) - Obsolete Product(s)
Obsolete Product(s) - Obsolete Product(s)

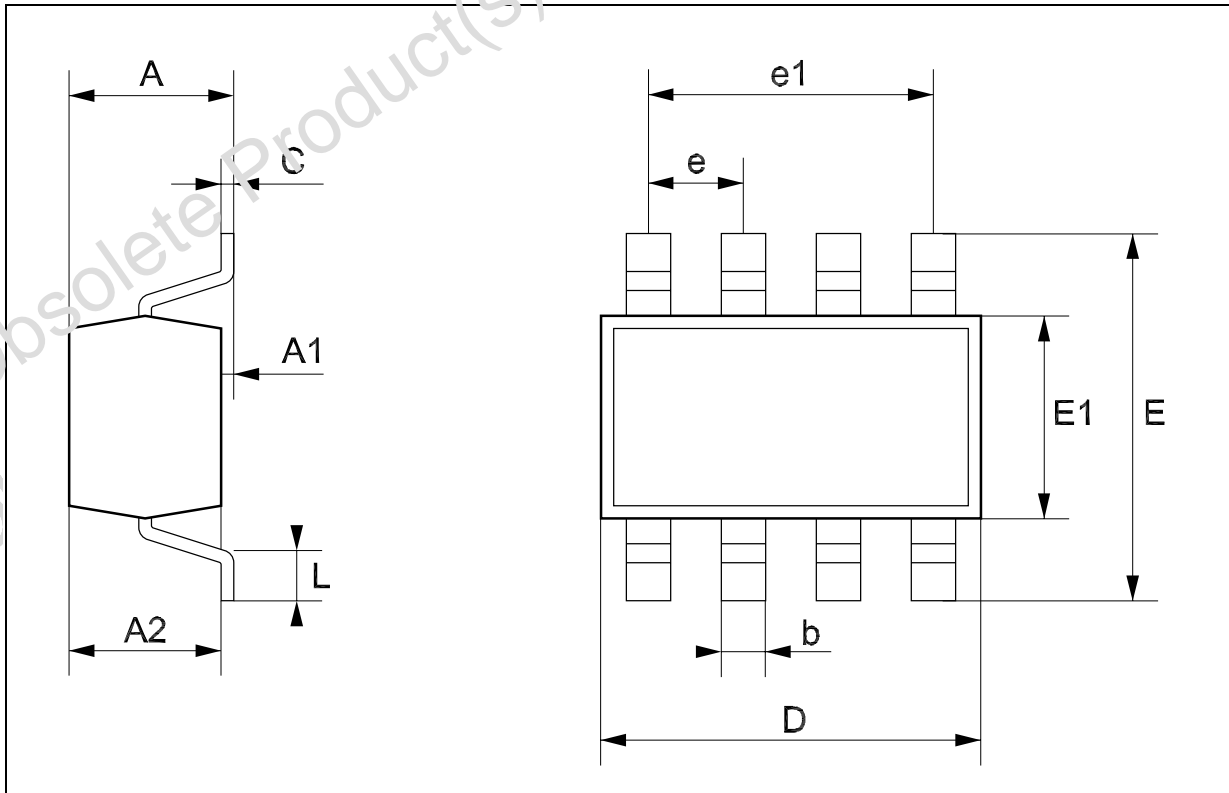
QFN8 (3x3) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.80	0.90	1.00	0.032	0.035	0.039
A1		0.03	0.05		0.001	0.002
A2	0.65	0.70	0.75	0.026	0.028	0.030
A3	0.15	0.20	0.25	0.006	0.008	0.010
b	0.29	0.31	0.39	0.011	0.012	0.015
b1	0.17		0.30	0.007		0.012
D		3.00			0.118	
D2	1.92	2.02	2.12	0.076	0.080	0.084
E		3.00			0.118	
E2	1.11	1.21	1.31	0.044	0.048	0.052
e		0.65			0.026	
K	0.20			0.008		
L	0.20	0.29	0.45	0.008	0.011	0.018
L1	0.16	0.24	0.40	0.006	0.009	0.016
L2			0.13			0.005
r		0.15			0.006	
r1		0.15			0.006	



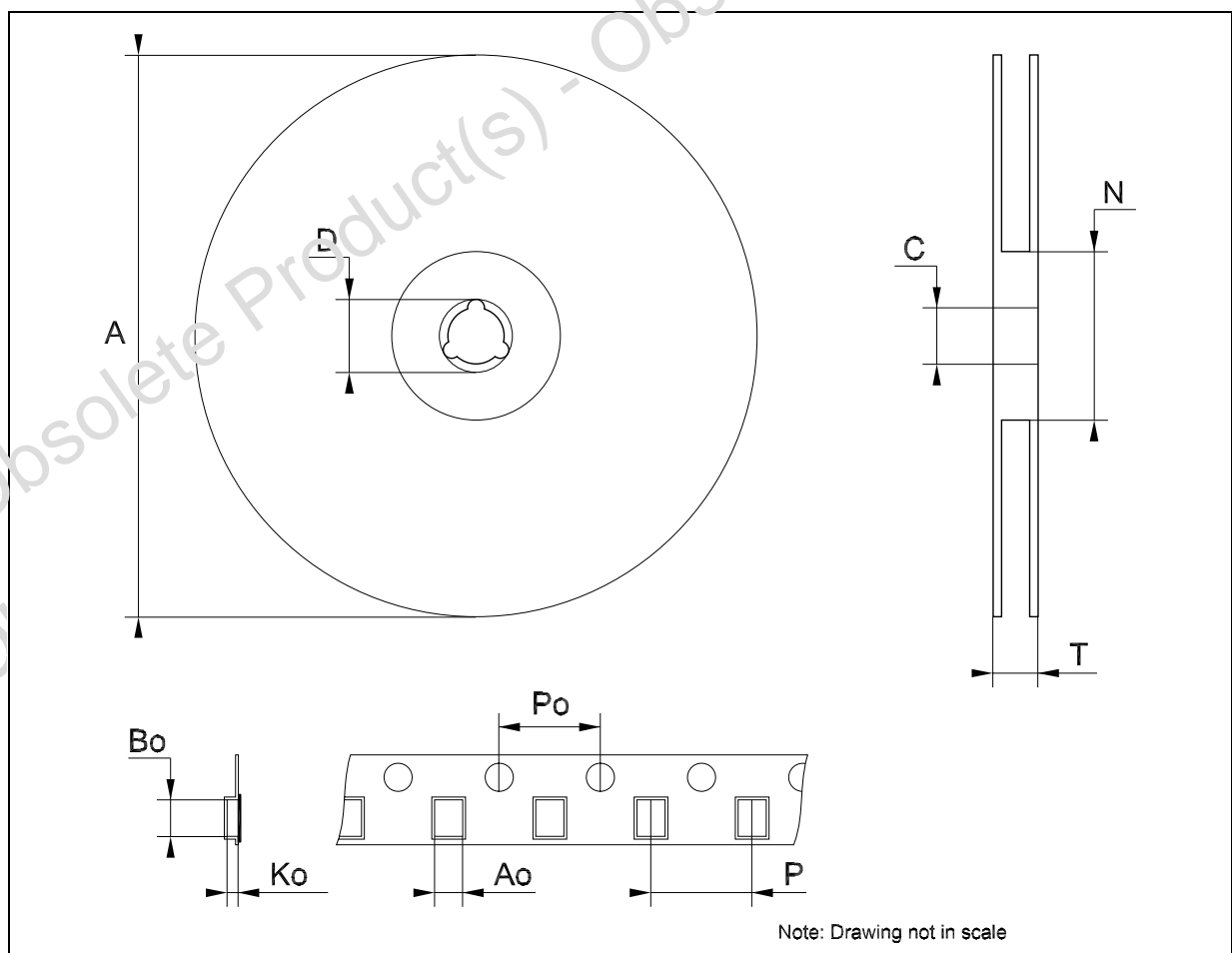
SOT23-8L MECHANICAL DATA

DIM.	mm.			mils		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.90		1.45	35.4		57.1
A1	0.00		0.15	0.0		5.9
A2	0.90		1.30	35.4		51.2
b	0.22		0.38	8.6		14.9
C	0.09		0.20	3.5		7.8
D	2.80		3.00	110.2		118.1
E	2.60		3.00	102.3		118.1
E1	1.50		1.75	59.1		68.8
e	0	.65		25.6		
e1		1.95		76.7		
L	0.35		0.55	13.7		21.6



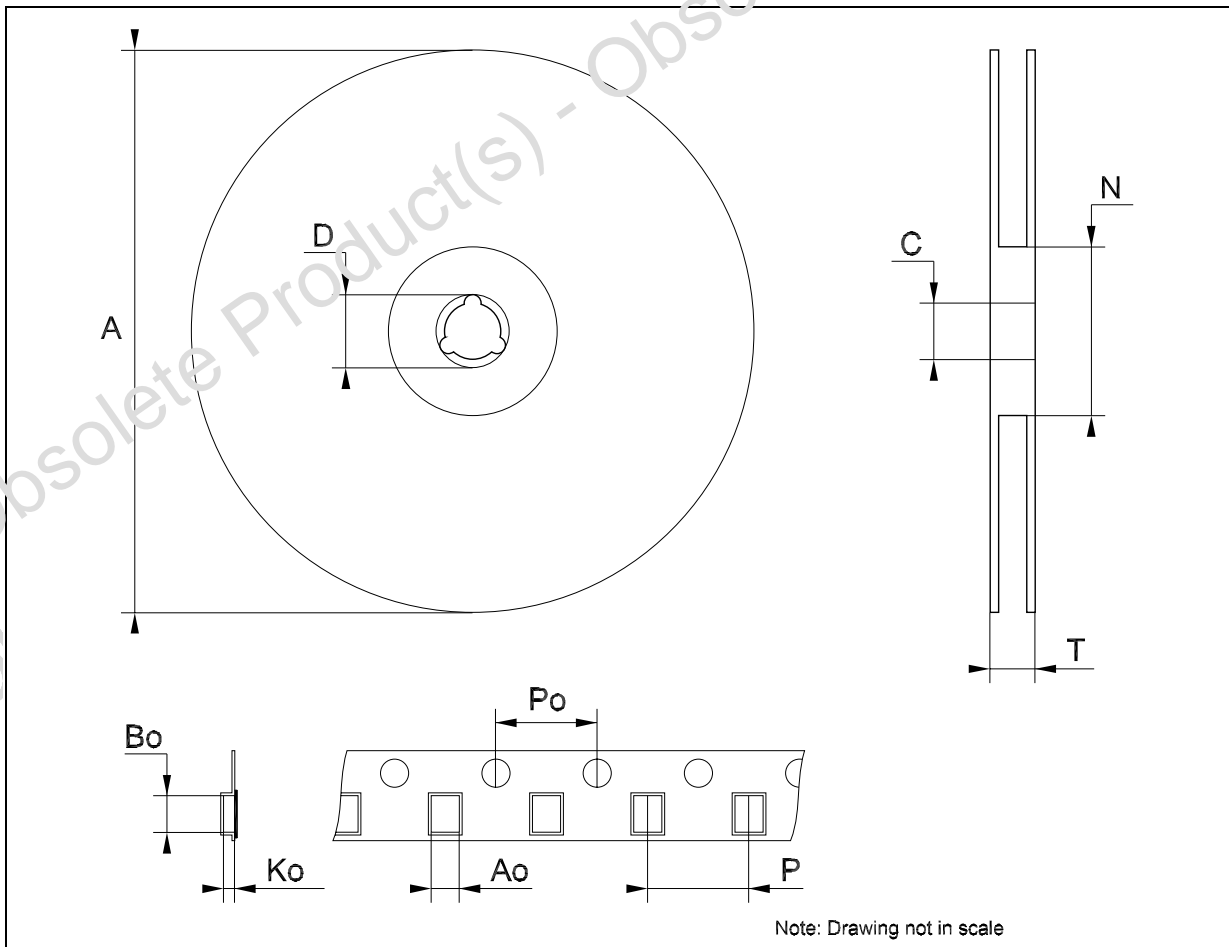
Tape & Reel QFNxx/DFNxx (3x3) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			18.4			0.724
Ao		3.3			0.130	
Bo		3.3			0.130	
Ko		1.1			0.043	
Po		4			0.157	
P		8			0.315	



Tape & Reel SOT23-xL MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			180			7.086
C	12.8	13.0	13.2	0.504	0.512	0.519
D	20.2			0.795		
N	60			2.362		
T			14.4			0.567
Ao	3.13	3.23	3.33	0.123	0.127	0.131
Bo	3.07	3.17	3.27	0.120	0.124	0.128
Ko	1.27	1.37	1.47	0.050	0.054	0.058
Po	3.9	4.0	4.1	0.153	0.157	0.161
P	3.9	4.0	4.1	0.153	0.157	0.161



13 Revision history

Table 6. Revision history

Date	Revision	Changes
3-Aug-2004	1	Initial release.
12-Oct-2004	2	Table 4 on page 4 following parameters values updated: · I_{LED} (min), I_Q (min), SW (QFN max), LDS (QFN max), I_{LIM} , Hyst OT · FB VAR symbol changed to Line and value changed from 0.7 to 0.9 mA/V
08-May-2006	3	Change figure 25, add figure 26 and new template.
23-Oct-2006	4	The SW, LDS and DC_{MIN} values on table 4 have been updated, add note in I_{LIM} .

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