# AK4345

## 100dB 96kHz 24-Bit Stereo 3.3V ΔΣ DAC with DIT

### GENERAL DESCRIPTION

The AK4345 is a 24bit low voltage and low power stereo DAC with an integrated Digital Audio Interface Transmitter. The AK4345 uses an Advanced Multi-Bit ΔΣ architecture, which achieves 100dB dynamic range at 3.3V operation. The AK4345 integrates both switched-capacitor and continuous time filters, enabling performance for systems that have excessive clock jitter. The output voltage level can be set as high as 1Vrms. The AK4345 is offered in a space saving 16pin TSSOP package.

### FEATURES

- ☐ **Sampling Rate: 8kHz ~ 96kHz**
- ☐ **24-Bit 8 times FIR Digital Filter**
- ☐ **SCF with high tolerance to clock jitter**
- ☐ **Single-ended output buffer**
- ☐ **Digital de-emphasis for 32kHz, 44.1kHz, 48kHz sampling**
- ☐ **I/F Format: 24-Bit MSB justified, 16/24-Bit LSB justified, $I^2S$ Compatible**
- ☐ **Master Clock:**
  - **512/768/1024/1536fs for Half Speed (8kHz ~ 24kHz)**
  - **256/384/512/768fs for Normal Speed (8kHz ~ 48kHz)**
  - **128/192/256/384fs for Double Speed (48kHz ~ 96kHz)**
- ☐ **μP Interface: 4-wire/3-wire**
- ☐ **DIT Bypass mode**
- ☐ **CMOS Input Level**
- ☐ **THD+N: -90dB**
- ☐ **DR, S/N: 100dB**
- ☐ **DAC output voltage level: 1Vrms (@VDD=3.3V)**
- ☐ **DIT**
  - **- AES3, IEC60958, S/PDIF, EIAJ CP1201 Compatible**
  - **- 1-channel Transmission output**
  - **- 42-bit Channel Status Buffer**
- ☐ **Power Supply: 2.7 to 3.6V**
- ☐ **Ta = –20 ~ 85°C**
- ☐ **16pin TSSOP**

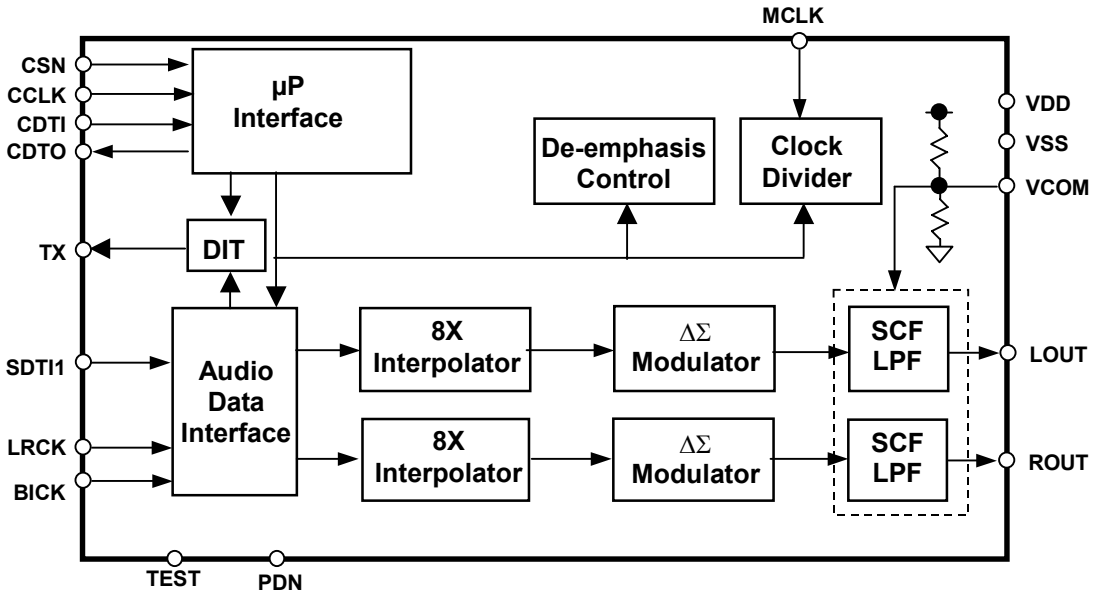



Figure 1. AK4345 Block Diagram (Mode= "0")

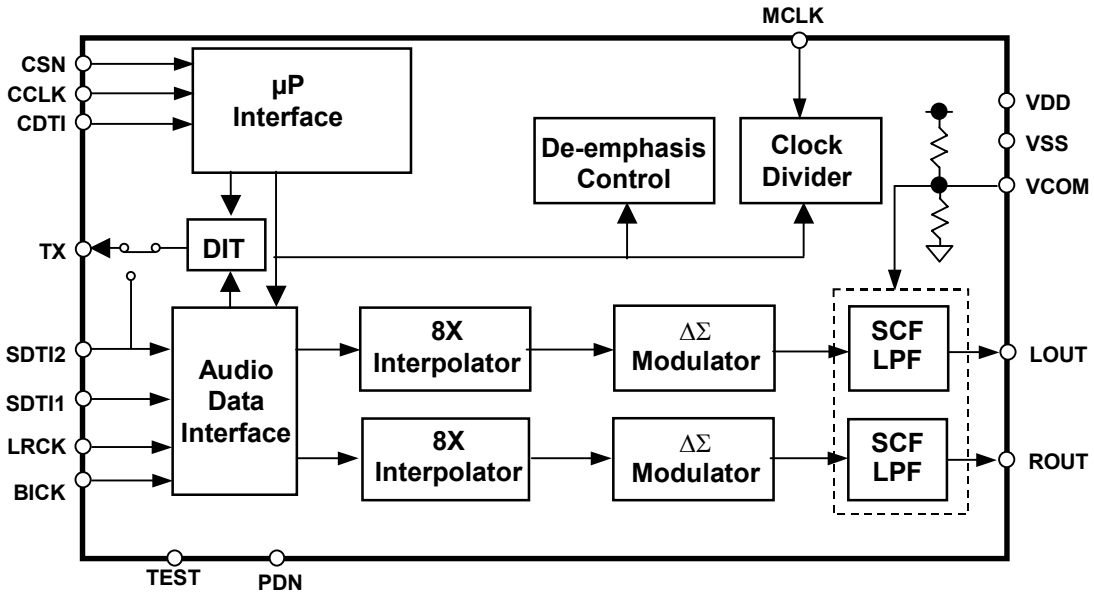
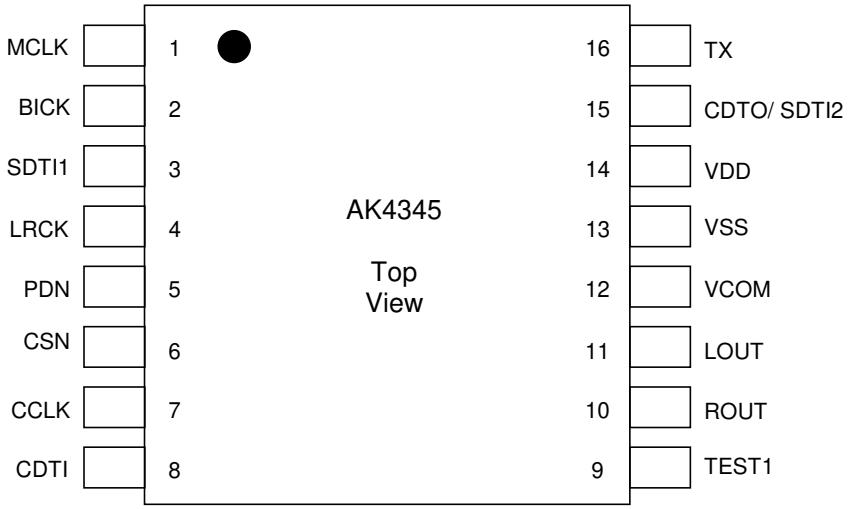



Figure 2. AK4345 Block Diagram (Mode= "1")

## ■ Ordering Guide

| | | |
|---|---|---|
| AK4345ET | –20 ~ +85°C | 16pin TSSOP (0.65mm pitch) |
| AKD4345 | Evaluation Board for AK4345 | |

## ■ Pin Layout



## PIN/FUNCTION

| No. | Pin Name | I/O | Function |
|---|---|---|---|
| 1 | MCLK | I | Master Clock Input Pin |
| 2 | BICK | I | Audio Serial Data Clock Pin |
| 3 | SDTI1 | I | Audio Serial Data Input Pin1 |
| 4 | LRCK | I | Input Channel Clock Pin |
| 5 | PDN | I | Full Power Down Mode Pin<br>"L" : Power down, "H" : Power up |
| 6 | CSN | I | Chip Select Pin |
| 7 | CCLK | I | Control Data Clock Pin |
| 8 | CDTI | I | Control Data Input Pin |
| 9 | TEST1 | I | TEST Pin<br>This pin must be OPEN. |
| 10 | ROUT | O | Rch Analog Output Pin, The output is "Hi-Z" when PDN pin = "L". |
| 11 | LOUT | O | Lch Analog Output Pin, The output is "Hi-Z" when PDN pin = "L". |
| 12 | VCOM | O | Common Voltage Output Pin, 0.5 × VDD<br>Normally connected to VSS with a 4.7μF (min. 1μF, max. 10μF) electrolytic Capacitor. The output is "L" when PDN pin = "L". |
| 13 | VSS | - | Ground Pin |
| 14 | VDD | - | Power Supply Pin, 2.7 ~ 3.6V |
| 15 | CDTO | O | Control Data Output Pin, The output is "Hi-Z" when PDN pin = "L". |
| | SDTI2 | I | Audio Serial Data Input Pin2 |
| 16 | TX | O | Transmit Channel Output Pin, The output is "L" when PDN pin = "L". |

Note: All digital input pins should not be left floating.

## ABSOLUTE MAXIMUM RATINGS

(VSS=0V; Note 1)

| Parameter | Symbol | min | max | Units |
|---|---|---|---|---|
| Power Supply | VDD | −0.3 | 4.6 | V |
| Input Current, Any Pin Except Supplies | IIN | - | ±10 | mA |
| Digital Input Voltage (Note 2) | VIND | −0.3 | VDD+0.3 | V |
| Ambient Temperature (Powered applied) | Ta | −20 | 85 | °C |
| Storage Temperature | Tstg | −65 | 150 | °C |

Note 1. All voltages with respect to ground.
Note 2. MCLK, BICK, SDTI1, LRCK, PDN, CSN, CCLK, CDTI, SDTI2

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

## RECOMMENDED OPERATING CONDITIONS

(VSS=0V; Note 1)

| Parameter | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|
| Power Supply | VDD | 2.7 | 3.3 | 3.6 | V |

Note 1. All voltages with respect to ground.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

## ANALOG CHARACTERISTICS

(Ta=25°C; VDD=3.3V; VSS=0V; fs=44.1kHz, 96kHz; BICK=64fs; Signal Frequency=1kHz; 24bit Data; Measurement frequency=20Hz ~ 20kHz at fs=44.1kHz, 20Hz ~ 40kHz at fs=96kHz; unless otherwise specified)

| Parameter | | | min | typ | max | Units |
|---|---|---|---|---|---|---|
| **Dynamic Characteristics (GAIN bit= "1") :** | | | | | | |
| Resolution | | | | | 24 | Bits |
| THD+N | fs=44.1kHz BW=20kHz | 0dBFS | | -90 | -80 | dB |
| | | –60dBFS | | –37 | - | dB |
| | fs=96kHz BW=40kHz | 0dBFS | | -88 | - | dB |
| | | –60dBFS | | –34 | - | dB |
| DR | (–60dBFS with A-weighted) | | 92 | 100 | | dB |
| S/N | (A-weighted) | | 92 | 100 | | dB |
| Interchannel Isolation | | | 80 | 100 | | dB |
| **DC Accuracy:** | | | | | | |
| Interchannel Gain Mismatch | | | | 0.2 | 0.5 | dB |
| Gain Drift | | | | 100 | - | ppm/°C |
| Output Voltage: GAIN bit= "1" | | (Note 3) | 2.60 | 2.8 | 3.0 | Vpp |
| Output Voltage: GAIN bit="0" | | (Note 4) | 2.05 | 2.2 | 2.35 | Vpp |
| Load Resistance | | (Note 5) | 10 | | | kΩ |
| Load Capacitance | | | | | 25 | pF |
| **Power Supplies** | | | | | | |
| Power Supply Current | | | | | | |
| Normal Operation (PDN pin = "H", fs=44.1kHz) | | (Note 6) | | 7.0 | | mA |
| Normal Operation (PDN pin = "H", fs=96kHz) | | (Note 6) | | 8.5 | 12.8 | mA |
| Full Power-down mode (PDN pin = "L") | | (Note 7) | | 10 | 50 | μA |

Note 3. Full-scale voltage (0dB). Output voltage scales with the voltage of VDD, Vout = 0.85 × VDD (typ).
Note 4. Full-scale voltage (0dB). Output voltage scales with the voltage of VDD, Vout = 0.67 × VDD (typ).
Note 5. For AC-load.
Note 6. RSTN bit= "1", PW bit= "1", TX pin: open. When TX pin = 20pF, power supply current (IDD@3.3V) is 9.0mA(typ)@fs= 96kHz.
Note 7. All digital input pins are fixed to VDD or VSS.

## FILTER CHARACTERISTICS

(Ta=25°C; VDD=2.7 ~ 3.6V; fs=44.1kHz; DEM1 bit= "0", DEM0 bit= "1")

| Parameter | | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|---|
| **DAC Digital Filter:** | | | | | | |
| Passband (Note 8) | ±0.05dB | PB | 0 | | 20.0 | kHz |
| | −6.0dB | | - | 22.05 | - | kHz |
| Stopband (Note 8) | | SB | 24.1 | | | kHz |
| Passband Ripple | | PR | | | ±0.01 | dB |
| Stopband Attenuation | | SA | 54 | | | dB |
| Group Delay (Note 9) | | GD | - | 24.0 | - | 1/fs |
| **Digital Filter + SCF + CTF:** | | | | | | |
| Frequency Response | 0 ~ 20kHz | FR | - | ±0.1 | - | dB |
| | ~ 40kHz (Note 10) | | - | ±0.2 | - | dB |

Note 8. The passband and stopband frequencies scale with fs (system sampling rate).
Note 9. The calculating delay time which occurred by digital filtering. This time is from setting the 16/24bit data of both channels to input register to the output of analog signal.
Note 10. At fs=96kHz.

## DC CHARACTERISTICS

(Ta=25°C; VDD=2.7 ~ 3.6V)

| Parameter | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|
| High-Level Input Voltage | VIH | 70%VDD | - | - | V |
| Low-Level Input Voltage | VIL | - | - | 30%VDD | V |
| High-Level Output Voltage (Iout=-80μA) | VOH1 | VDD-0.4 | - | - | V |
| Low-Level Output Voltage (Iout=80μA) | VOL1 | - | - | 0.4 | V |
| Input Leakage Current | Iin | - | - | ± 10 | μA |

## TX CHARACTERISTICS

(Ta=25°C; VDD=2.7 ~ 3.6V)

| Parameter | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|
| High-Level Output Voltage ( Iout=-400μA) | VOH2 | VDD-0.4 | - | - | V |
| Low-Level Output Voltage ( Iout=400μA) | VOL2 | - | - | 0.4 | V |
| Load Capacitance | CL | - | - | 50 | pF |

## SWITCHING CHARACTERISTICS

(Ta=25°C; VDD=2.7 ~ 3.6V; $C_L$ = 20pF)

| Parameter | | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|---|
| **Master Clock Frequency** | | | | | | |
| Half Speed Mode (512/768/1024/1536fs) | | fCLK | 4.096 | | 36.864 | MHz |
| Normal Speed Mode (256/384/512/768fs) | | fCLK | 2.048 | | 36.864 | MHz |
| Double Speed Mode (128/192/256/384fs) | | fCLK | 6.144 | | 36.864 | MHz |
| Duty Cycle | | dCLK | 40 | | 60 | % |
| **LRCK Frequency** | | | | | | |
| Half Speed Mode | (DFS1-0 = "10") | fsh | 8 | | 24 | kHz |
| Normal Speed Mode | (DFS1-0 = "00") | fsn | 8 | | 48 | kHz |
| Double Speed Mode | (DFS1-0 = "01") | fsd | 48 | | 96 | kHz |
| Duty Cycle | | dCLK | 45 | | 55 | % |
| **Audio Interface Timing** | | | | | | |
| BICK Period | | | | | | |
| Half Speed Mode | | tBCK | 1/128fs | | | ns |
| Normal Speed Mode | | tBCK | 1/128fs | | | ns |
| Double Speed Mode | | tBCK | 1/64fs | | | ns |
| BICK Pulse Width Low | | tBCKL | 70 | | | ns |
| Pulse Width High | | tBCKH | 70 | | | ns |
| BICK "↑" to LRCK Edge | (Note 11) | tBLR | 40 | | | ns |
| LRCK Edge to BICK "↑" | (Note 11) | tLRB | 40 | | | ns |
| SDTI Hold Time | | tSDH | 40 | | | ns |
| SDTI Setup Time | | tSDS | 40 | | | ns |
| **Control Interface Timing** | | | | | | |
| CCLK Period | | tCCK | 200 | | | ns |
| CCLK Pulse Width Low | | tCCKL | 80 | | | ns |
| Pulse Width High | | tCCKH | 80 | | | ns |
| CDTI Setup Time | | tCDS | 40 | | | ns |
| CDTI Hold Time | | tCDH | 40 | | | ns |
| CSN "H" Time | | tCSW | 150 | | | ns |
| CSN "↓" to CCLK "↑" | | tCSS | 150 | | | ns |
| CCLK "↑" to CSN "↑" | | tCSH | 50 | | | ns |
| CDTO Delay | | tDCD | | | 45 | ns |
| CSN "↑" to CDTO Hi-Z | | tCCZ | | | 70 | ns |
| **Power-Down & Reset Timing** | | | | | | |
| PDN Pulse Width | (Note 12) | tPD | 4 | | | ms/µF |

Note 11. BICK rising edge must not occur at the same time as LRCK edge.

Note 12. The AK4345 can be reset by bringing PDN pin = "L".

The PDN pulse width is proportional to the value of the capacitor (C) connected to VCOM pin. tPD = 4000× C.

When C = 4.7µF, tPD is 19ms(min).

The value of the capacitor (C) connected with VCOM pin should be 1µF ≤ C ≤ 10µF.

## ■ Timing Diagram

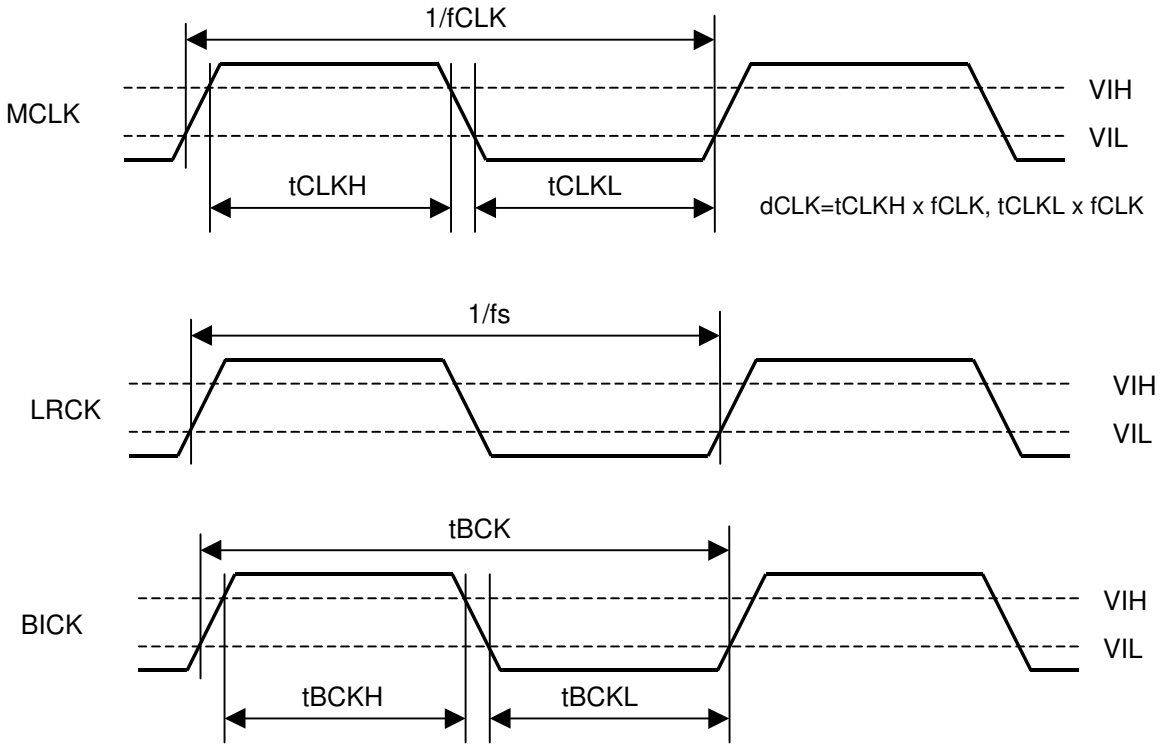



Figure 3. Clock Timing

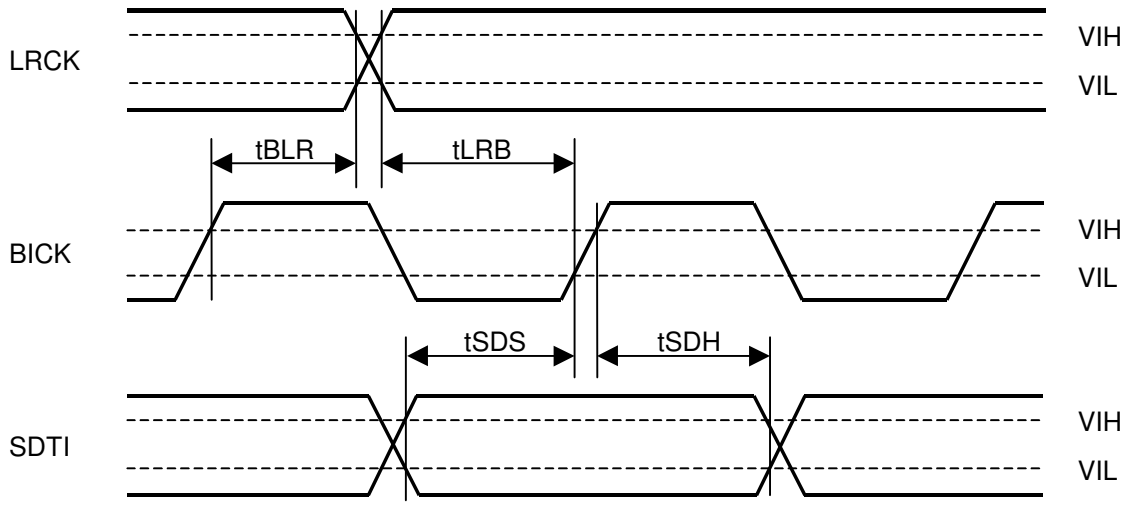



Figure 4. Serial Interface Timing

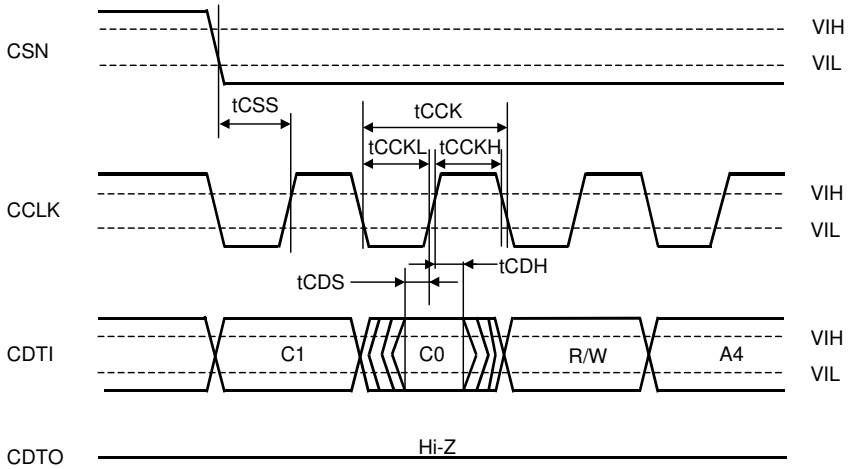



Figure 5. WRITE/READ Command Input Timing in 3-wire/4-wire serial mode

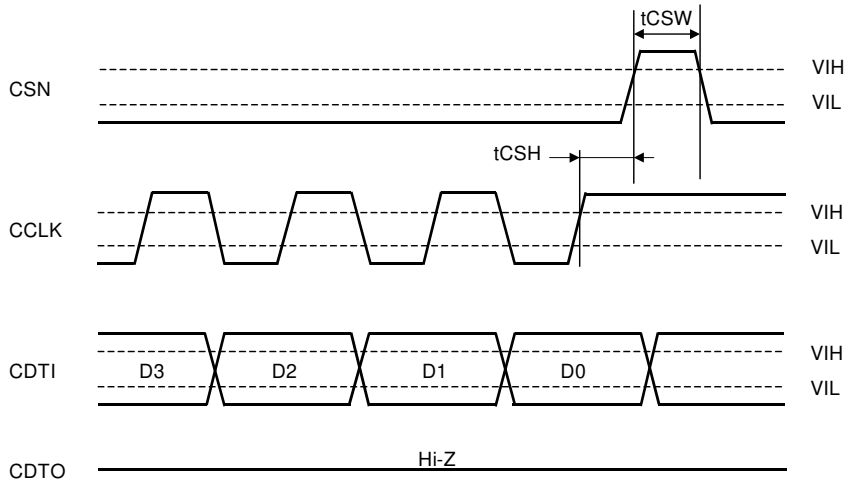



Figure 6. WRITE Data Input Timing in 3-wire/4-wire serial mode

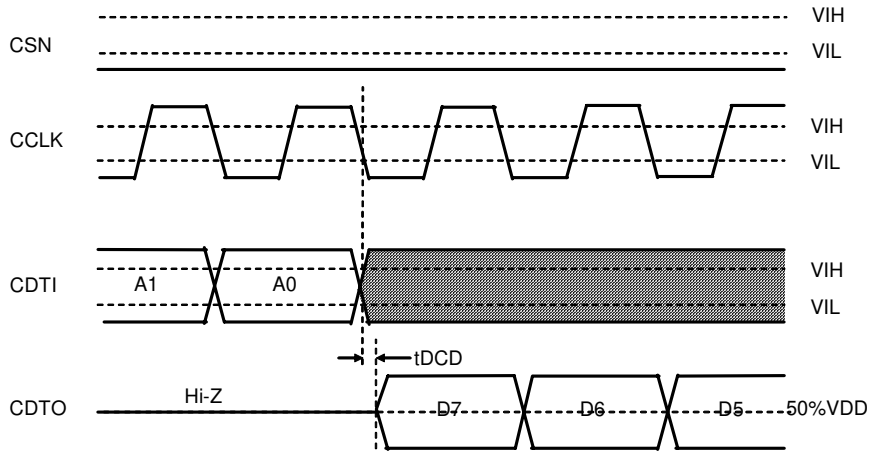



Figure 7. READ Data Output Timing 1 in 4-wire serial mode

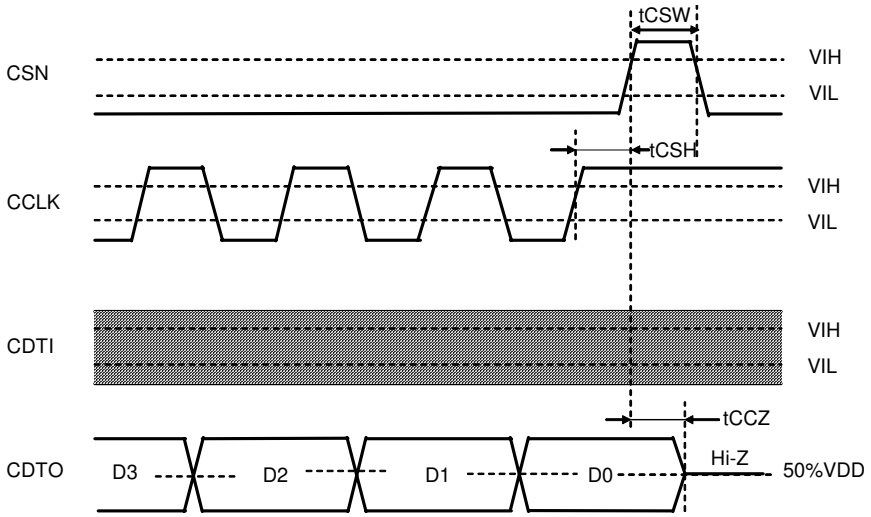



Figure 8. READ Data Output Timing 2 in 4-wire serial mode

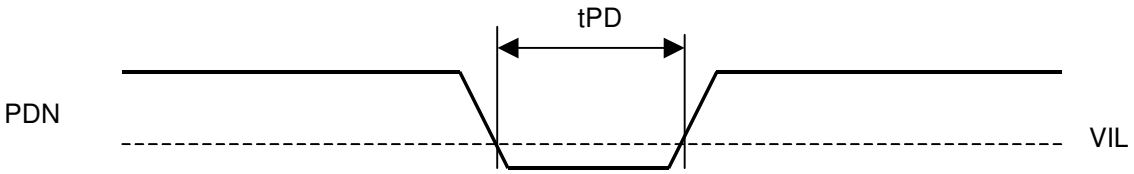



Figure 9. Power-Down & Reset Timing

# OPERATION OVERVIEW

## ■ System Clock

The external clocks, which are required to operate the AK4345, are MCLK, BICK and LRCK. The master clock (MCLK) should be synchronized with LRCK but the phase is not critical. The MCLK is used to operate the digital interpolation filter and the delta-sigma modulator. The MCLK frequency is detected from the relation between MCLK and LRCK automatically. The Half speed, the Normal speed and the Double speed mode are selected with the DFS1-0 bits (Table 1). The sampling speed mode is set depending on the MCLK frequency automatically for Auto mode (DFS1 bit = DFS0 bit = "1") (Table 2).

The AK4345 is automatically placed in the reset mode when MCLK stops in the normal operation mode (PDN pin = "H"), and the analog output becomes the VCOM voltage. After MCLK is input again, the AK4345 is powered up. After exiting reset by PDN pin at power-up etc., the AK4345 is in the reset mode until MCLK and LRCK are input.

| Mode | DFS1 | DFS0 | fs | MCLK Frequency |
|---|---|---|---|---|
| Normal Speed | 0 | 0 | 8 ~ 48kHz | 256/384/512/768fs |
| Double Speed | 0 | 1 | 48 ~ 96kHz | 128/192/256/384fs |
| Half Speed | 1 | 0 | 8 ~ 24kHz | 512/768/1024/1536fs |
| Auto | 1 | 1 | 8 ~ 96kHz | Table 2 |

Table 1. System Clock Example

| MCLK Frequency | Sampling Speed Mode | Fs |
|---|---|---|
| 512/768fs | Normal Speed | 8 ~ 48kHz |
| 128/192/256/384fs | Double Speed | 48 ~ 96kHz |
| 1024/1536fs | Half Speed | 8 ~ 24kHz |

Table 2. Auto Mode

## ■ Audio Interface Format

The Data is shifted in via the SDTI pin using BICK and LRCK inputs. The DIF1-0 bits as shown in Table 3 can select four serial data modes. In all modes the serial data is MSB-first, 2's compliment format and is latched on the rising edge of BICK. Mode 3 can be used for 16bit $I^2S$ Compatible format by zeroing the unused LSBs at BICK ≥ 48fs or BICK = 32fs.

| Mode | DIF1 | DIF0 | SDTI Format | BICK | Figure |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 16bit, LSB justified | ≥ 32fs | Figure 10 |
| 1 | 0 | 1 | 24bit, LSB justified | ≥ 48fs | Figure 11 |
| 2 | 1 | 0 | 24bit, MSB justified | ≥ 48fs | Figure 12 |
| 3 | 1 | 1 | 16/24bit, $I^2S$ Compatible | ≥ 48fs or 32fs | Figure 13 |

Table 3. Audio Interface Format

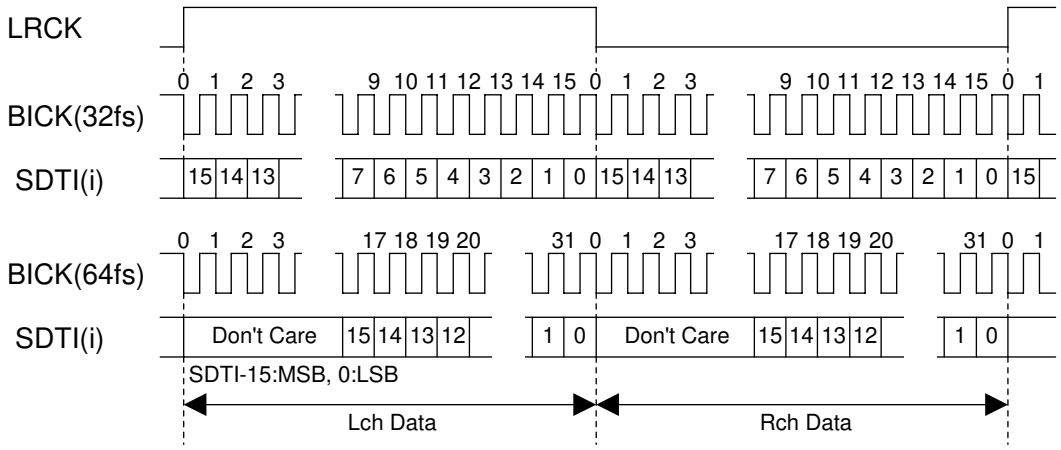



Figure 10. Mode 0 Timing

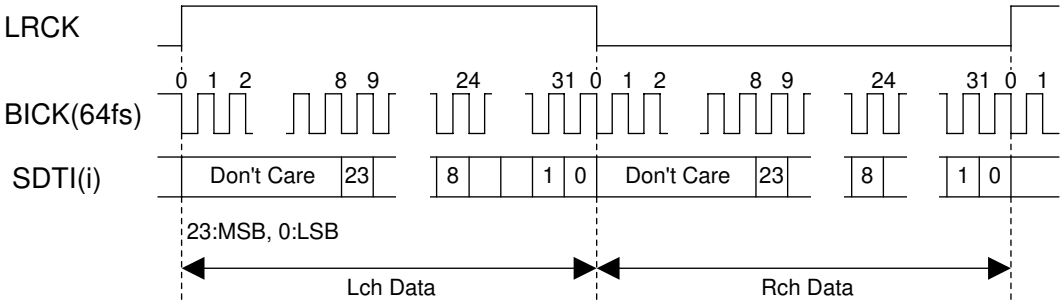



Figure 11. Mode 1 Timing

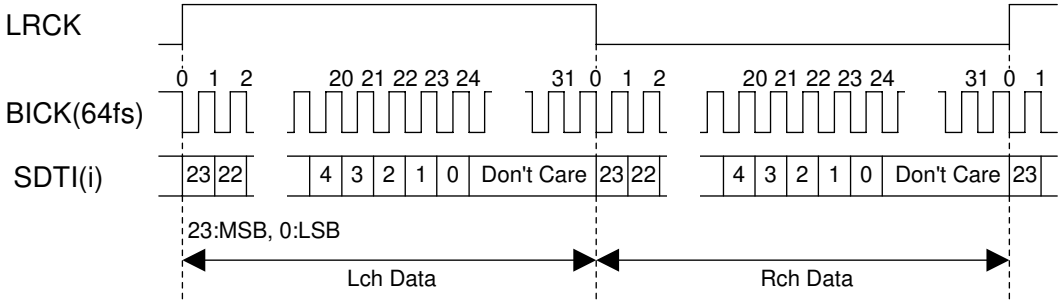



Figure 12. Mode 2 Timing

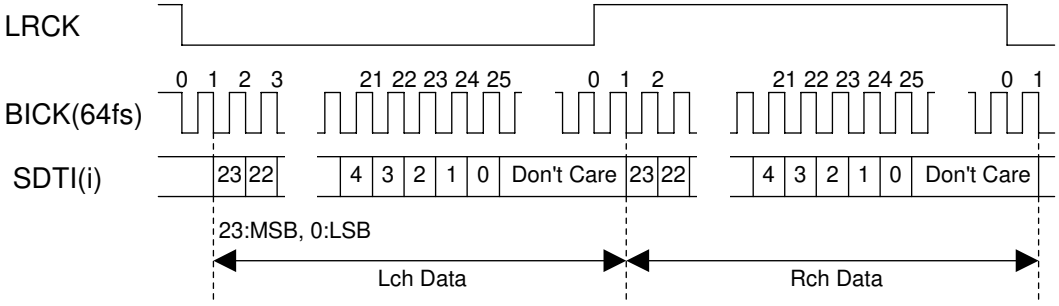



Figure 13. Mode 3 Timing

## ■ Data Transmission Format

Data transmitted on the TX outputs is formatted in blocks as shown in Figure 14. Each block consists of 192 frames. A frame of data contains two sub-frames. A sub-frame consists of 32 bits of information. Each received data bit is coded using a bi-phase mark encoding as a two binary state symbol. The preambles violate bi-phase encoding so they may be differentiated from data. In bi-phase encoding, the first state of an input symbol is always the inverse of the last state of the previous data symbol. For a logic 0, the second state of the symbol is the same as the first state. For a logic 1, the second state is the opposite of the first. Figure 15 illustrates a sample stream of 8 data bits encoded in 16 symbol states.

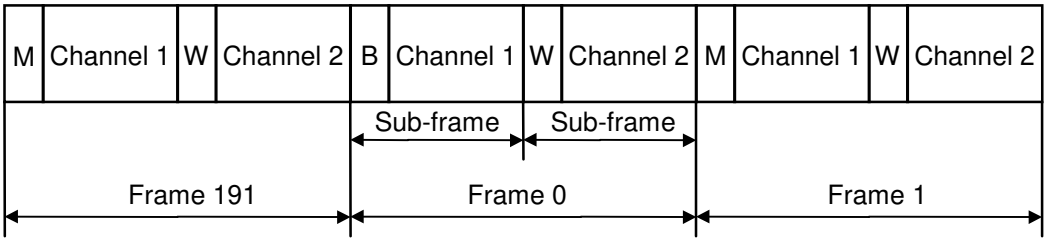



Figure 14. Block format

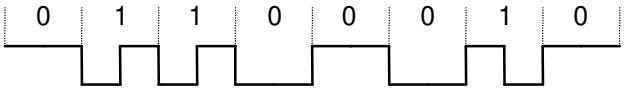



Figure 15. A biphase-encoded bit stream

The sub-frame is defined in Figure 16 below. Bits 0-3 of the sub-frame represent a preamble for synchronization. There are three preambles. The block preamble, B, is contained in the first sub-frame of Frame 0. The channel 1 preamble, M, is contained in the first sub-frame of all other frames. The channel 2 preamble, W, is contained in all of the second sub-frames.
Table 4 below defines the symbol encoding for each of the preambles. Bits 4-27 of the sub-frame contain the 24 bit audio sample in 2's complement format with bit 27 as the most significant bit. For 16 bit mode, Bits 4-11 are all 0. Bit 28 is the validity flag. This is "H" if the audio sample is unreliable. Bit 29 is a user data bit. Frame 0 contains the first bit of a 192 bit user data word. Frame 191 contains the last bit of the user data word. Bit 30 is a channel status bit. Again frame 0 contains the first bit of the 192 bit word with the last bit in frame 191. Bit 31 is an even parity bit for bits 4-31 of the sub-frame.

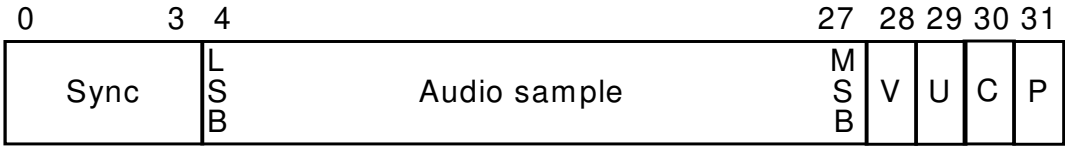



Figure 16. Sub-frame format

The block of data contains consecutive frames transmitted at a state-bit rate of 64 times the sample frequency, fs. For stereophonic audio, the left or A channel data is in channel 1 while the right or B data is in channel 2. For monophonic audio, channel 1 contains the audio data.

| Preamble | Preceding state = 0 | Preceding state = 1 |
|---|---|---|
| B | 11101000 | 00010111 |
| M | 11100010 | 00011101 |
| W | 11100100 | 00011011 |

Table 4. Sub-frame preamble encoding

## ■ Channel Status bit

In the consumer mode (bit0 = "0"), bits20-23(audio channel) must be controlled by the CS20 bit. When the CS20 bit is "1", the AK4345 corresponds to "stereo mode", bits20-23 are set to "1000"(left channel) in sub-frame 1, and is set to "0100"(right channel) in sub-frame 2. When the CS20 bit is "0", bits20-23 is set to "0000" in both sub-frame 1 and sub-frame 2.

## ■ De-emphasis Filter

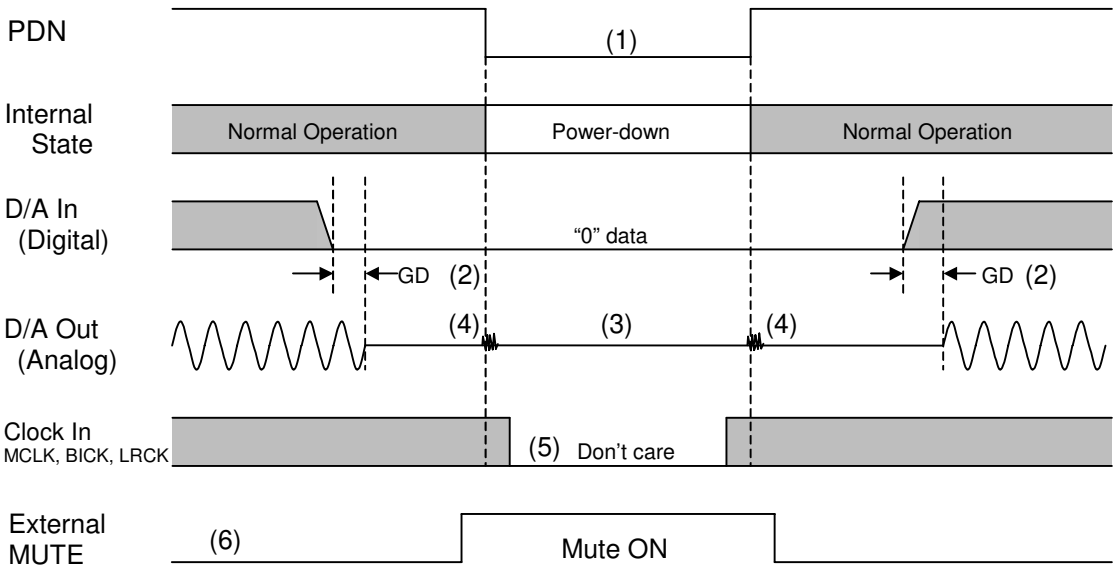
A digital de-emphasis filter is available for 32, 44.1 or 48kHz sampling rates (tc = 50/15μs) and is controlled by DEM0 and DEM1. In double speed and quad speed mode, the digital de-emphasis filter is always off.

| DEM1 | DEM0 | Mode | |
|---|---|---|---|
| 0 | 0 | 44.1kHz | |
| 0 | 1 | OFF | (default) |
| 1 | 0 | 48kHz | |
| 1 | 1 | 32kHz | |

Table 5. De-emphasis Filter Control (Normal Speed Mode)

## ■ Power-down

The AK4345 is placed in the power-down mode by bringing PDN pin = "L". and the digital filter is reset at the same time. This reset should always be done after power up.




Notes:

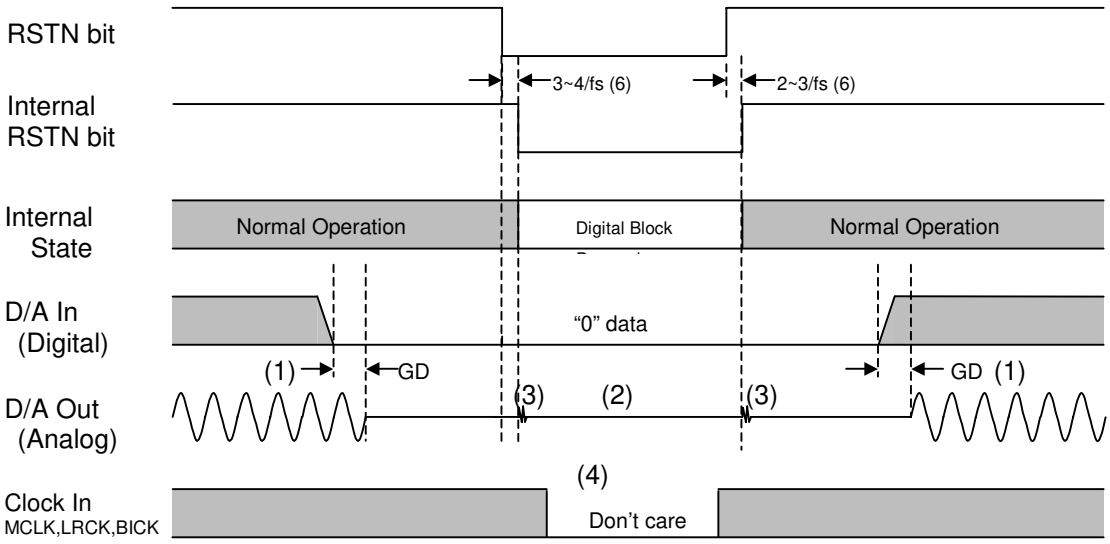
(1) PDN pin should be "L" for 19ms or more when an electrolytic capacitor 4.7μF is attached between VCOM pin and VSS.
(2) The analog output corresponding to digital input has the group delay (GD).
(3) When PDN pin = "L", the analog output is Hi-Z.
(4) Click noise occurs in 3 ~ 4LRCK at both edges (↑ ↓) of PDN signal. This noise is output even if "0" data is input.
(5) The external clocks (MCLK, BICK and LRCK) can be stopped in the power down mode (PDN pin = "L").
(6) Please mute the analog output externally if the click noise (4) influences system application. The timing example is shown in this figure.

Figure 17. Power-down/up sequence example

## ■ Reset Function

(1) Reset by RSTN bit

When RSTN bit =0, DAC is powered down but the internal register values are not initialized. The analog outputs go to VCOM voltage Figure 18 shows the example of reset by RSTN bit.

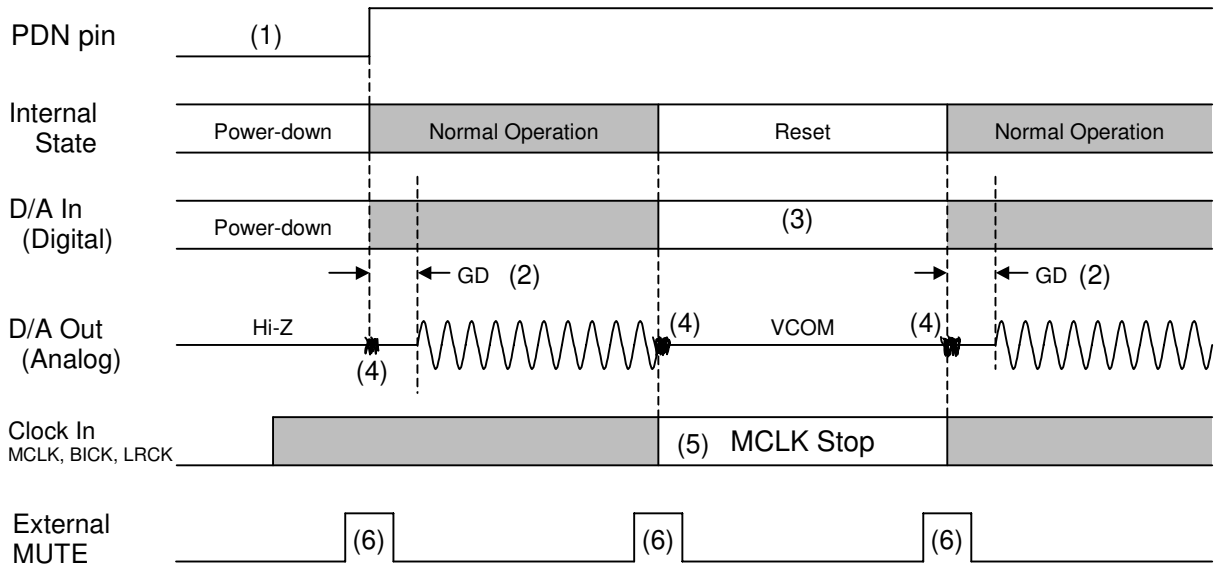



Notes:

(1) The analog output corresponding to digital input has the group delay (GD).
(2) Analog outputs go to VCOM voltage (VDD/2).
(3) Click noise occurs at the edges("↑ ↓") of the internal timing of RSTN bit. This noise is output even if "0" data is input.
(4) The external clocks (MCLK, BICK and LRCK) can be stopped in the reset mode (RSTN bit = "0").
(5) There is a delay, 3~4/fs from RSTN bit "0" to the internal RSTN bit "0", and 2~3/fs from RSTN bit "1" to the internal RSTN bit "1".

Figure 18. Reset Sequence Example1

(2) RESET by MCLK stop (PDN pin = "H")
When MCLK stops, DAC is powered down but the internal register values are not initialized. The analog outputs go to VCOM voltage.




Notes:
(1) PDN pin should be "L" for 19ms or more when an electrolytic capacitor 4.7μF is attached between VCOM pin and VSS.
(2) The analog output corresponding to digital input has the group delay (GD).
(3) The digital data can be stopped. The click noise after MCLK is input again by inputting the "0" data to this section can be reduced.
(4) Click noise occurs in 3 ~ 4LRCK at both edges (↑ ↓) of PDN signal, MCLK inputs and MCLK stops. This noise is output even if "0" data is input.
(5) The external clocks (BICK and LRCK) can be stopped in the power down mode (MCLK stop).
(6) Please mute the analog output externally if the click noise (4) influences system application. The timing example is shown in this figure.

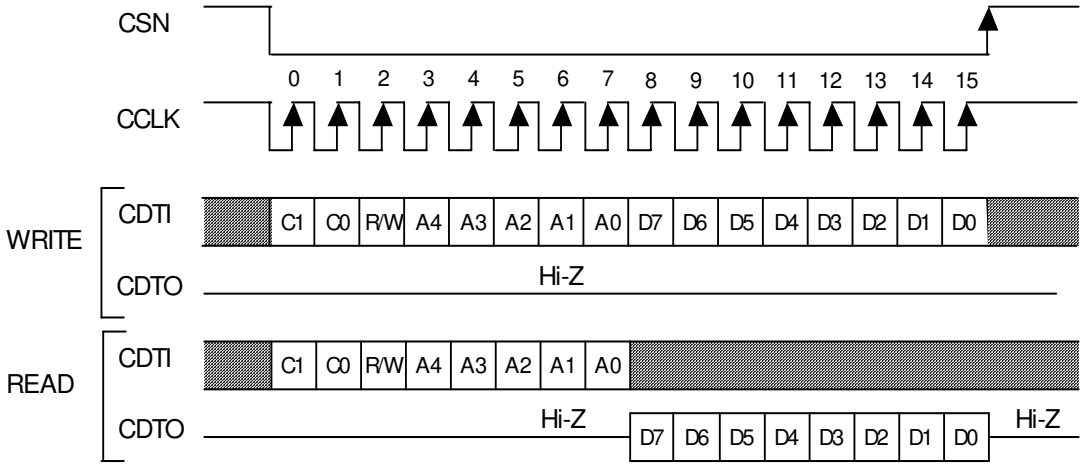
Figure 19. Reset Sequence Example 2

## ■ μP Control Interface

The AK4345 can select 4-wire μP I/F mode (MODE bit = "0") or 3-wire μP I/F mode (MODE bit = "1").

1.4-wire μP I/F mode (MODE bit = "0", default)

The internal registers may be either written or read by the 4-wire μP interface pins: CSN, CCLK, CDTI and CDTO. The data on this interface consists of Chip address (2bits, C1/0; fixed to "01"), Read/Write (1bit), Register address (MSB first, 5bits) and Control data (MSB first, 8bits). Address and data are clocked in on the rising edge of CCLK and data is clocked out on the falling edge. For write operations, data is latched after the 16th rising edge of CCLK, after a high-to-low transition of CSN. CSN should be set to "H" once after 16 CCLKs. For read operations, the CDTO output goes high impedance after a low-to-high transition of CSN. The maximum speed of CCLK is 5MHz. PDN pin = "L" resets the registers to their default values.




C1-C0: Chip Address: (Fixed to "01")
R/W: READ/WRITE (0:READ, 1:WRITE)
A4-A0: Register Address
D7-D0: Control Data

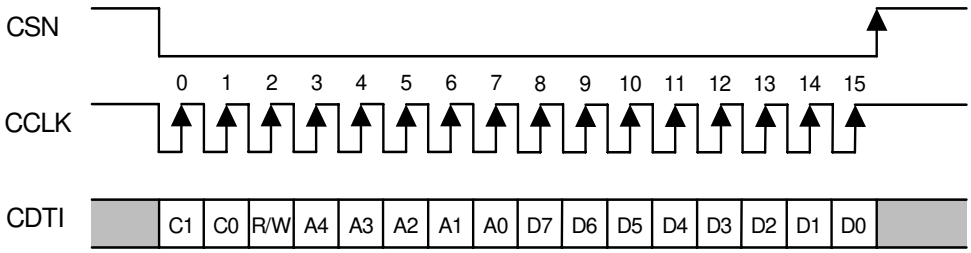
Figure 20. 4-wire Serial Control I/F Timing

*When the AK4345 is in the power down mode (PDN pin = "L") or the MCLK is not provided, writing into the control register is inhibited.

2.3-wire μP I/F mode (MODE bit = "1")

Internal registers may be written by 3-wire μP interface pins, CSN, CCLK and CDTI. The data on this interface consists of Chip Address (2bits, C1/0; fixed to "01"), Read/Write (1bit; fixed to "1", Write only), Register Address (MSB first, 5bits) and Control Data (MSB first, 8bits). AK4345 latches the data on the rising edge of CCLK, so data should clocked in on the falling edge. The writing of data becomes valid by 16th CCLK after a high to low transition of CSN. CSN should be set to "H" once after 16 CCLKs for each address. The clock speed of CCLK is 5MHz (max).

PDN pin = "L" resets the registers to their default values. The internal timing circuit is reset by RSTN bit, but the registers are not initialized.




C1-C0: Chip Address (Fixed to "01")
R/W: READ/WRITE (Fixed to "1", Write only)
A4-A0: Register Address
D7-D0: Control Data

Figure 21. Control I/F Timing

*The AK4345 does not support the read command and chip address. C1/0 and R/W are fixed to "011"
*When the AK4345 is in the power down mode (PDN pin = "L") or the MCLK is not provided, writing into the control register is inhibited.

## ■ DAC and DIT input select

The AK4345 can select 4-wire μP I/F mode (MODE bit = "0") or 3-wire μP I/F mode (MODE bit = "1"). In 3-wire μP I/F mode, the AK4345 can select the input data of DAC and DIT from SDTI1 or SDTI2 data.

| MODE | SEL1 | SEL0 | μP I/F | DAC input | DIT input |
|---|---|---|---|---|---|
| 0 | x | x | 4-wire | SDTI1 | SDTI1 |
| 1 | 0 | 0 | 3-wire | SDTI1 | SDTI1 |
| 1 | 0 | 1 | 3-wire | SDTI2 | SDTI2 |
| 1 | 1 | 0 | 3-wire | SDTI2 | Bypass |
| 1 | 1 | 1 | Reserved | | |

(x: Don't care)

Table 6. DAC and DIT Input

## ■ Register Map

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 00H | Control 1 | 1 | 0 | 0 | 0 | DIF1 | DIF0 | PW | RSTN |
| 01H | Control 2 | 0 | 1 | 0 | DFS1 | DFS0 | DEM1 | DEM0 | GAIN |
| 02H | Control 3 | 0 | 0 | 0 | INVL | INVR | MODE | SEL1 | SEL0 |
| 03H | TX | 0 | 0 | 0 | 0 | 0 | 0 | V | TXE |
| 04H | Channel Status Byte0 | CS7 | CS6 | CS5 | CS4 | CS3 | CS2 | CS1 | CS0 |
| 05H | Channel Status Byte1 | CS15 | CS14 | CS13 | CS12 | CS11 | CS10 | CS9 | CS8 |
| 06H | Channel Status Byte2 | CS23 | CS22 | CS21 | CS20 | CS19 | CS18 | CS17 | CS16 |
| 07H | Channel Status Byte3 | CS39 | CS38 | CS37 | CS36 | CS35 | CS34 | CS33 | CS32 |
| 08H | Channel Status Byte4 | CS39 | CS38 | CS37 | CS36 | CS35 | CS34 | CS33 | CS32 |
| 09H | Channel Status Byte5 | 0 | 0 | 0 | 0 | 0 | 0 | CS41 | CS40 |

Notes:

For addresses from 0AH to 1FH, data must not be written.

When PDN pin goes “L”, the registers are initialized to their default values.

When RSTN bit goes “0”, the only internal timing is reset and the registers are not initialized to their default values. All data can be written to the register even if PW or RSTN bit is “0”.

The bits shown as “0” should be written “0” and the bits shown as “1” should be written “1”.

## ■ Register Definitions

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 00H | Control 1 | 1 | 0 | 0 | 0 | DIF1 | DIF0 | PW | RSTN |
| R/W | | R/W | | | | | | | |
| Default | | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

RSTN: Internal timing reset control

0: Reset. All registers are not initialized.

1: Normal Operation

When MCLK frequency or DFS changes the click noise occurs. It can be reduced by RSTN bit.

PW: Power down control

0: Power down. All registers are not initialized.

1: Normal Operation

DIF1-0: Audio data interface formats (Table 3)

Initial: “11”, Mode 3

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 01H | Control 2 | 0 | 1 | 0 | DFS1 | DFS0 | DEM1 | DEM0 | GAIN |
| R/W | | R/W | | | | | | | |
| Default | | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |

DEM1-0: De-emphasis Response (Table 5)
Initial: "01", OFF

DFS1-0: Sampling speed control
00: Normal speed
01: Double speed
10: Half speed
11: Auto (default)
When changing between Normal/Double Speed Mode and Half Speed Mode, some click noise occurs.

GAIN: Output Voltage scale
0: Vout = 0.67 × VDD (typ) at Full-scale voltage (0dB) .
1: Vout = 0.85 × VDD (typ) at Full-scale voltage (0dB) .

| | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 02H | Control 3 | 0 | 0 | 0 | INVL | INVR | MODE | SEL1 | SEL0 |
| R/W | | R/W | | | | | | | |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

INVR: Inverting Lch Output Polarity
0: Normal Output
1: Inverted Output

INVL: Inverting Rch Output Polarity
0: Normal Output
1: Inverted Output

MODE: Mode Control
0: 4 wire mode
1: 3 wire mode

SEL1-0: DAC and DIT input
00: SDTI1 input
01: SDTI2 input
10: SDTI2 input (DIT Bypass)
11: Reserved
SEL1-0 bits are disabled in 4-wire μP I/F mode (MODE bit = "0").
SDTI1 data is input to both DAC and DIT.

| | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 03H | TX | 1 | 0 | 0 | 0 | 0 | 0 | V | TXE |
| R/W | | R/W | | | | | | | |
| Default | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

V: Validity Flag
0: Valid
1: Invalid

TXE: TX output
0: "L"
1: Normal Operation

| | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 04H | Channel Status Byte0 | CS7 | CS6 | CS5 | CS4 | CS3 | CS2 | CS1 | CS0 |
| Default | | 0 | 0 | 0 | 0 | 0 | **1** | 0 | 0 |
| 05H | Channel Status Byte1 | CS15 | CS14 | CS13 | CS12 | CS11 | CS10 | CS9 | CS8 |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 06H | Channel Status Byte2 | CS23 | CS22 | CS21 | CS20 | CS19 | CS18 | CS17 | CS16 |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 07H | Channel Status Byte3 | CS31 | CS30 | CS29 | CS28 | CS27 | CS26 | CS25 | CS24 |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 08H | Channel Status Byte4 | CS39 | CS38 | CS37 | CS36 | CS35 | CS34 | CS33 | CS32 |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 09H | Channel Status Byte5 | 0 | 0 | 0 | 0 | 0 | 0 | CS41 | CS40 |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

CS7-0: Transmitter Channel Status Byte 0
Default: "00000100"
CS39-8: Transmitter Channel Status Byte 4-1
Default: "00000000"
CS41-CS40: Transmitter Channel Status Byte 5
Default: "00000000", D7-D2 bits should be written "0".

## SYSTEM DESIGN

Figure 22 and Figure 23 shows the system connection diagram. The evaluation board is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.

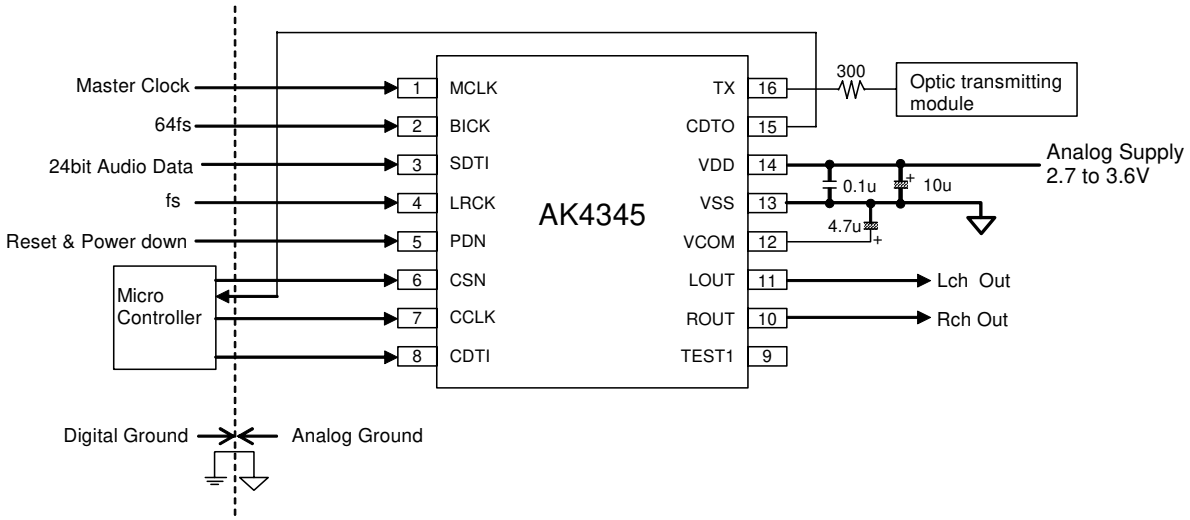



Figure 22. Typical Connection Diagram (Mode bit = "0", 4 wire mode )

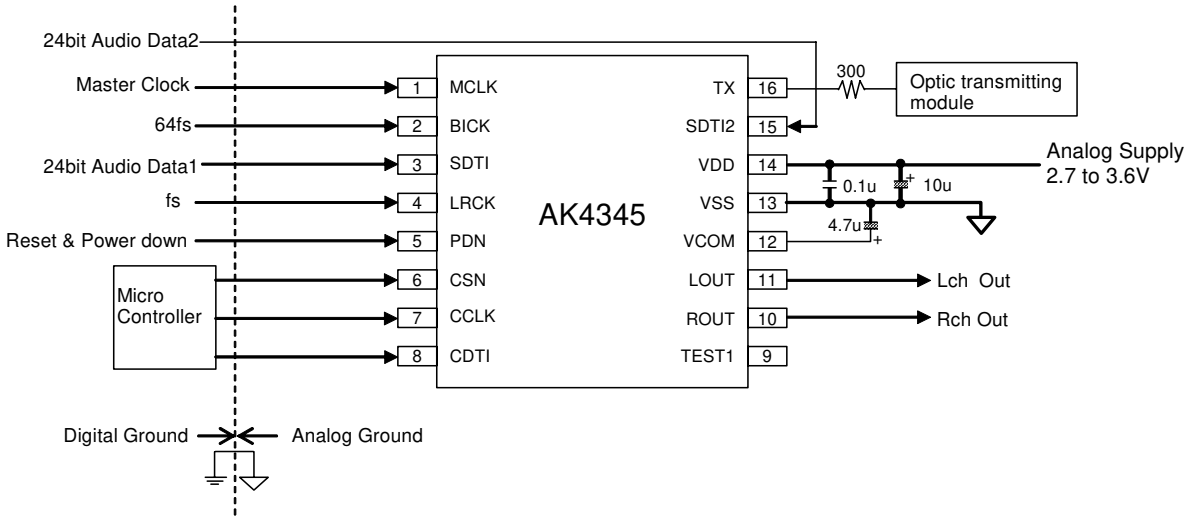



Figure 23. Typical Connection Diagram (Mode bit = "1", 3 wire mode )

### 1. Grounding and Power Supply Decoupling

The AK4345 requires careful attention for power supply and grounding arrangements. VDD is usually supplied from the analog supply in the system. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4345 as possible, with the small value ceramic capacitor being the closest.

### 2. Voltage Reference

The differential Voltage between VDD and VSS sets the analog output range. VCOM is used as a common voltage of the analog signal. VCOM pin is a signal ground of this chip. An electrolytic capacitor about 4.7μF should be attached between VCOM pin and VSS. No load current may be drawn from VCOM pin. Especially, the ceramic capacitor should be connected to this pin as near as possible.

### 3. Analog Outputs

The analog outputs are single-ended and centered around the VCOM voltage (0.5 × VDD). The output signal range is typically 2.8Vpp (typ@VDD=3.3V). The internal switched-capacitor filter and continuous-time filter attenuate the noise generated by the delta-sigma modulator beyond the audio passband. The output voltage is a positive full scale for 7FFFFFH (@24bit) and a negative full scale for 800000H (@24bit). The ideal output is VCOM voltage (0.5 × VDD) for 000000H (@24bit).

DC offsets on analog outputs are eliminated by AC coupling since analog outputs have DC offsets of VCOM + a few mV. Figure 24 shows an example of the external LPF with 2.8Vpp (1Vrms) output.

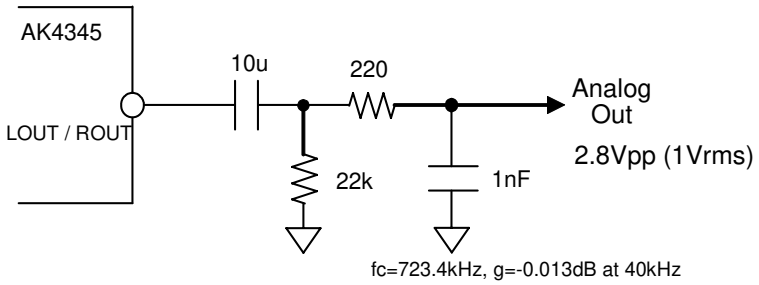
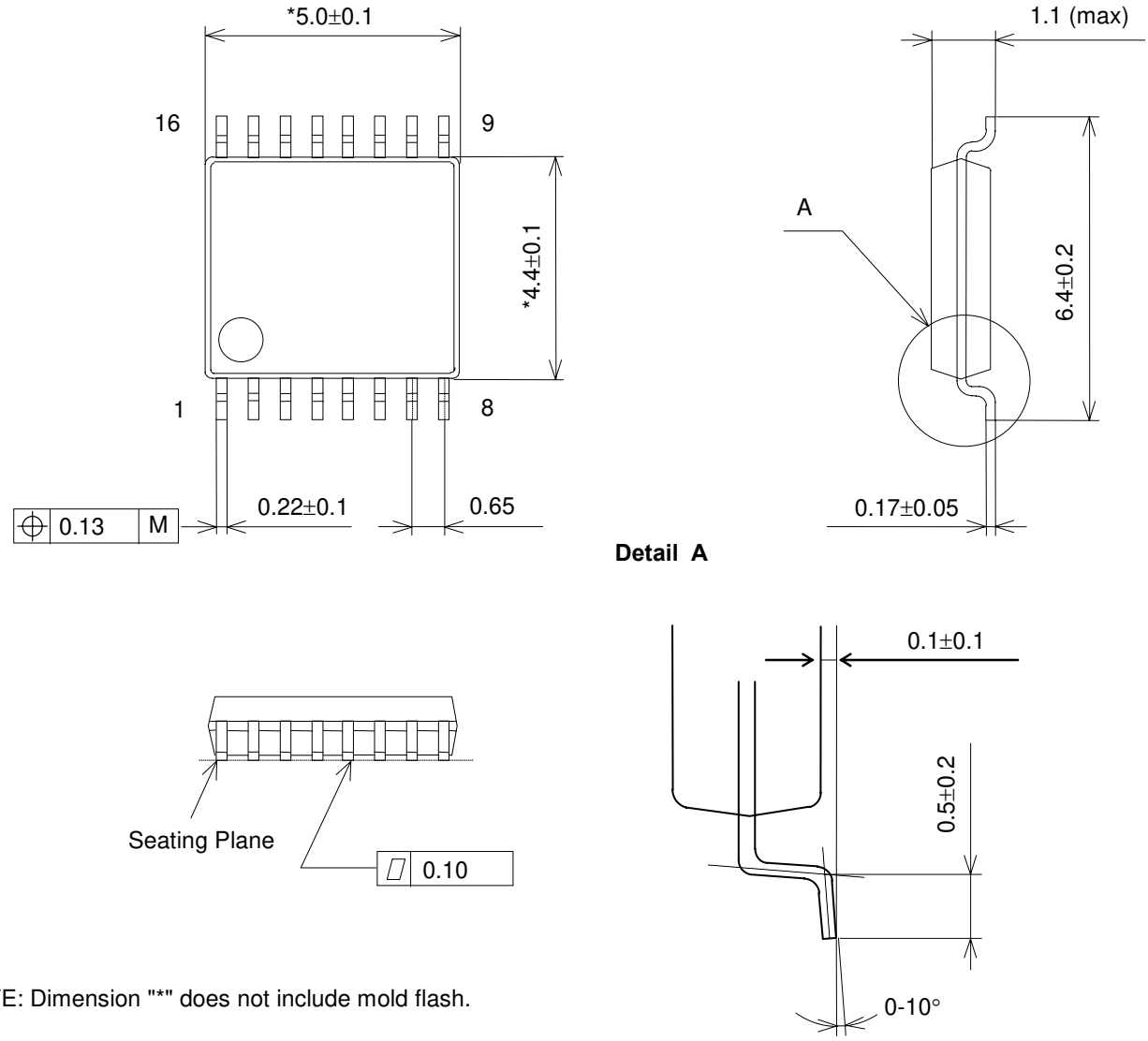



Figure 24. External 1st order LPF Circuit Example

## PACKAGE

# 16pin TSSOP (Unit: mm)

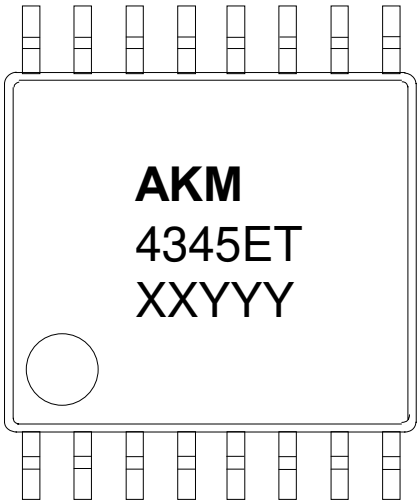



NOTE: Dimension "*" does not include mold flash.

### ■ Package & Lead frame material

| | |
|---|---|
| Package molding compound: | Epoxy |
| Lead frame material: | Cu |
| Lead frame surface treatment: | Solder (Pb free) plate |

## MARKING




1) Pin #1 indication
2) Date Code : XXYYY (5 digits)
   XX: Lot#
   YYY: Date Code
3) Marketing Code : 4345ET
4) Asahi Kasei Logo

## REVISION HISTORY

| Date (YY/MM/DD) | Revision | Reason | Page | Contents |
|---|---|---|---|---|
| 07/06/20 | 00 | First Edition | | |
| 10/09/28 | 01 | Specification Change | 25 | PACKAGE<br>The package dimensions were changed. |

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