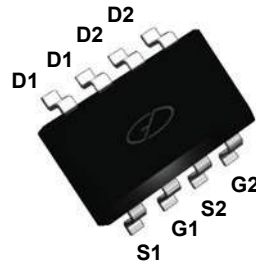
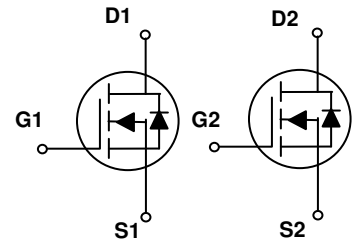


**Main Product Characteristics**

$V_{DS}$	60V
$R_{DS(ON)}$	120m $\Omega$
$I_D$	3.5A



SOP-8



Schematic Diagram

**Features and Benefits**

- Advanced MOSFET process technology
- Ideal for high efficiency switched mode power supplies
- Low on-resistance with low gate charge
- Fast switching and reverse body recovery



**Description**

The SSF6670 utilizes the latest techniques to achieve high cell density and low on-resistance. These features make this device extremely efficient and reliable for use in high efficiency switch mode power supply and a wide variety of other applications.

**Absolute Maximum Ratings** ( $T_A=25^{\circ}C$  unless otherwise specified)

Parameter	Symbol	Max.	Unit
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 25$	V
Drain Current-Continuous ( $T_C=25^{\circ}C$ ) <sup>1</sup>	$I_D$	3.5	A
Drain Current-Continuous ( $T_C=70^{\circ}C$ ) <sup>1</sup>		2.8	A
Drain Current-Pulsed <sup>1</sup>	$I_{DM}$	20	A
Power Dissipation	$P_D$	2.4	W
Thermal Resistance, Junction-to-Ambient <sup>2</sup>	$R_{\theta JA}$	62.5	$^{\circ}C/W$
Operating Junction Temperature Range	$T_J$	-55 To +175	$^{\circ}C$
Storage Temperature Range	$T_{STG}$	-55 To +175	$^{\circ}C$

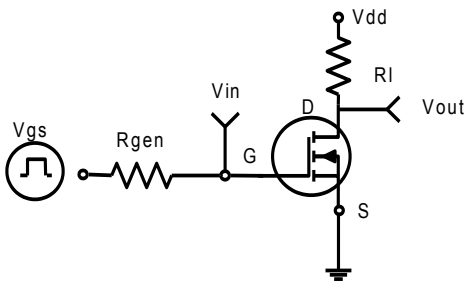
**Electrical Characteristics** ( $T_A=25^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	60	-	-	V
Drain-Source Leakage Current	$I_{DSS}$	$V_{DS}=60V, V_{GS}=0V$	-	-	10	$\mu A$
Gate-Source Leakage Current	$I_{GSS}$	$V_{GS}=\pm 25V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics<sup>3</sup></b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	1	-	3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=2A$	-	80	120	m $\Omega$
		$V_{GS}=10V, I_D=3A$	-	65	90	
Forward Transconductance	$g_{FS}$	$V_{DS}=10V, I_D=3A$	3	-	-	S
<b>Dynamic and Switching Characteristics<sup>4</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS}=25V, V_{GS}=0V, F=1MHz$	-	500	-	pF
Output Capacitance	$C_{oss}$		-	50	-	
Reverse Transfer Capacitance	$C_{rss}$		-	40	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DS}=30V, R_{GEN}=3\Omega, V_{GS}=10V, I_D=1A$	-	6	-	nS
Rise Time	$t_r$		-	5	-	
Turn-Off Delay Time	$t_{d(off)}$		-	16	-	
Fall Time	$t_f$		-	3	-	
Total Gate Charge	$Q_g$	$V_{DS}=48V, I_D=3A, V_{GS}=4.5V$	-	7	-	nC
Gate-Source Charge	$Q_{gs}$		-	2	-	
Gate-Drain Charge	$Q_{gd}$		-	3	-	
Body Diode Reverse Recovery Time	$T_{rr}$	$I_F=4A, di/dt=100A/\mu s$	-	27	-	nS
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	32	-	nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Diode Forward Voltage <sup>3</sup>	$V_{SD}$	$V_{GS}=0V, I_S=1.7A$	-	-	1.2	V

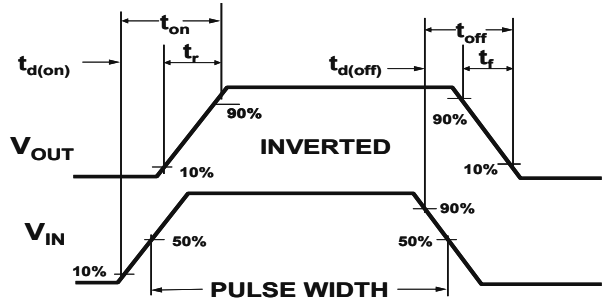
**NOTES:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on 1in<sup>2</sup> FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production testing.

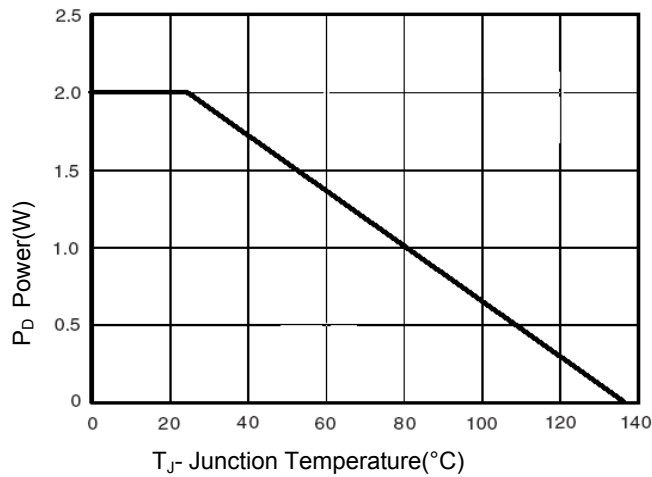
**Typical Electrical and Thermal Characteristic Curves**



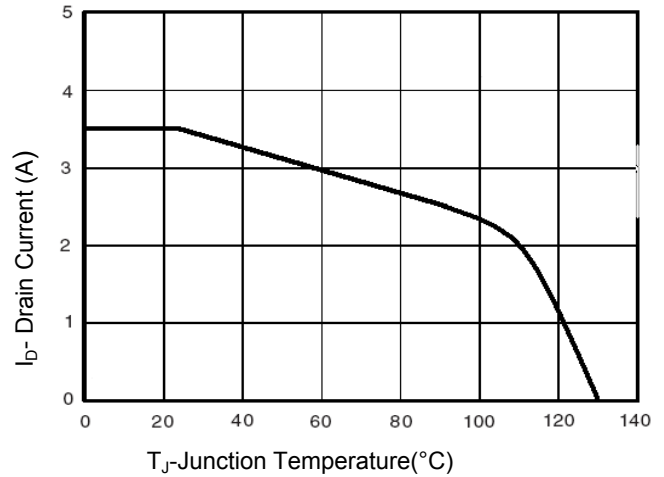
**Figure 1. Switching Test Circuit**



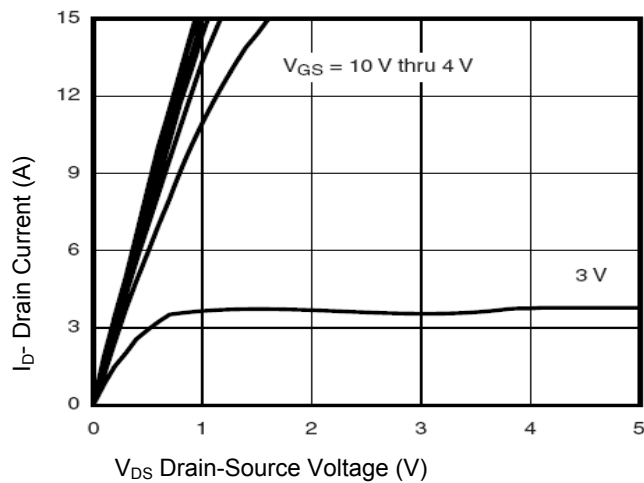
**Figure 2. Switching Waveforms**



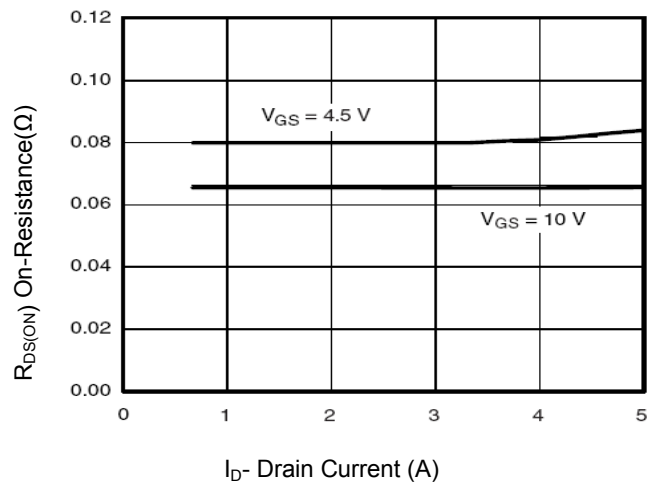
**Figure 3. Power Dissipation**



**Figure 4. Drain Current vs Junction Temperature**

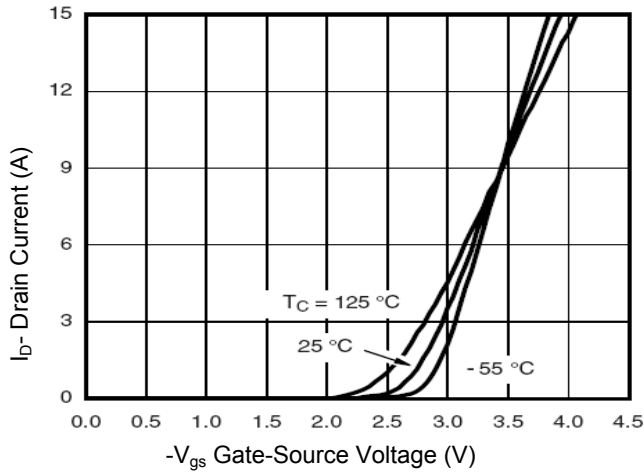


**Figure 5. Output Characteristics**

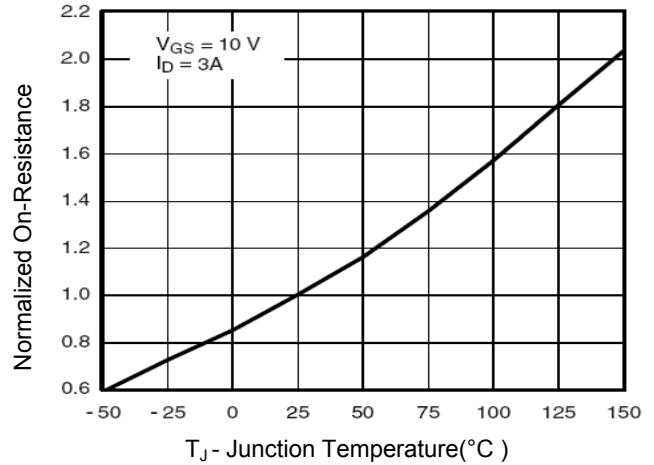


**Figure 6. Drain-Source On-Resistance**

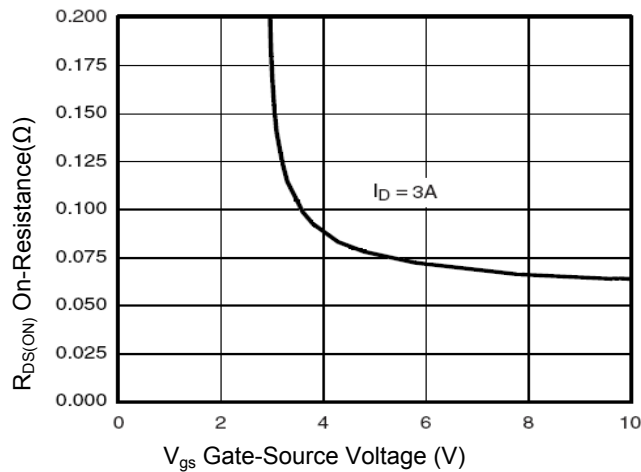
**Typical Electrical and Thermal Characteristic Curves**



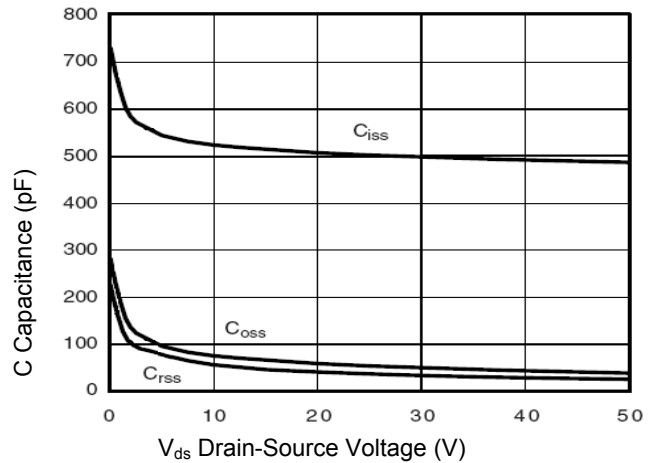
**Figure 7. Transfer Characteristics**



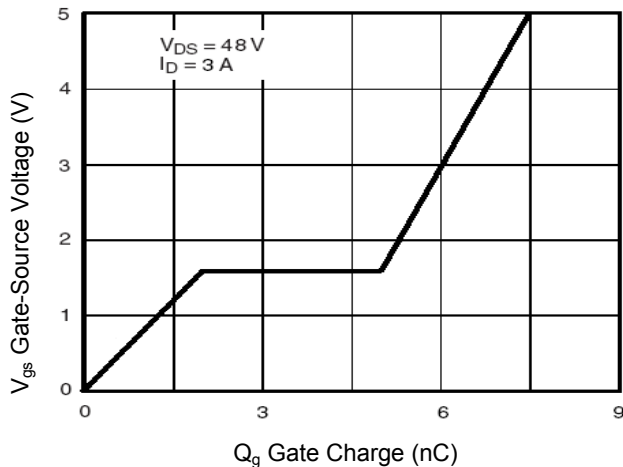
**Figure 8. Drain-Source On-Resistance**



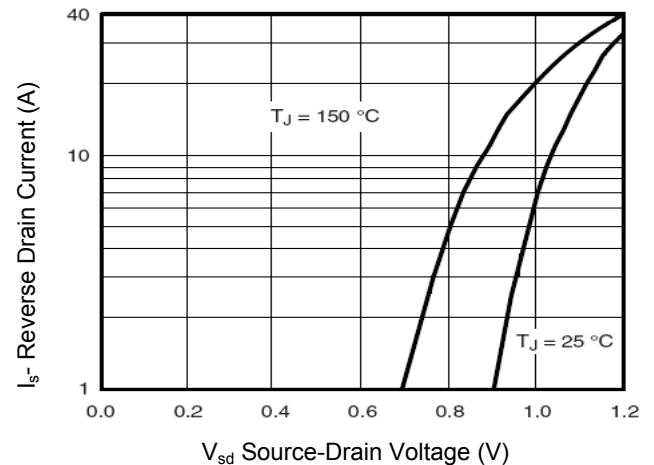
**Figure 9.  $R_{DS(ON)}$  vs  $V_{GS}$**



**Figure 10. Capacitance vs  $V_{DS}$**

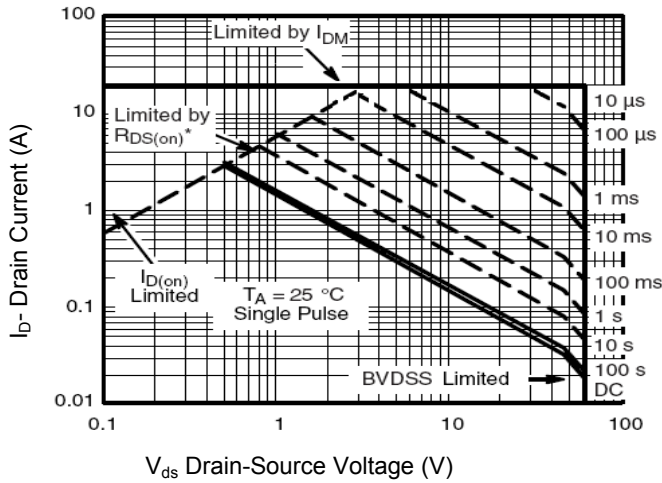


**Figure 11. Gate-Source Voltage vs Gate Charge**

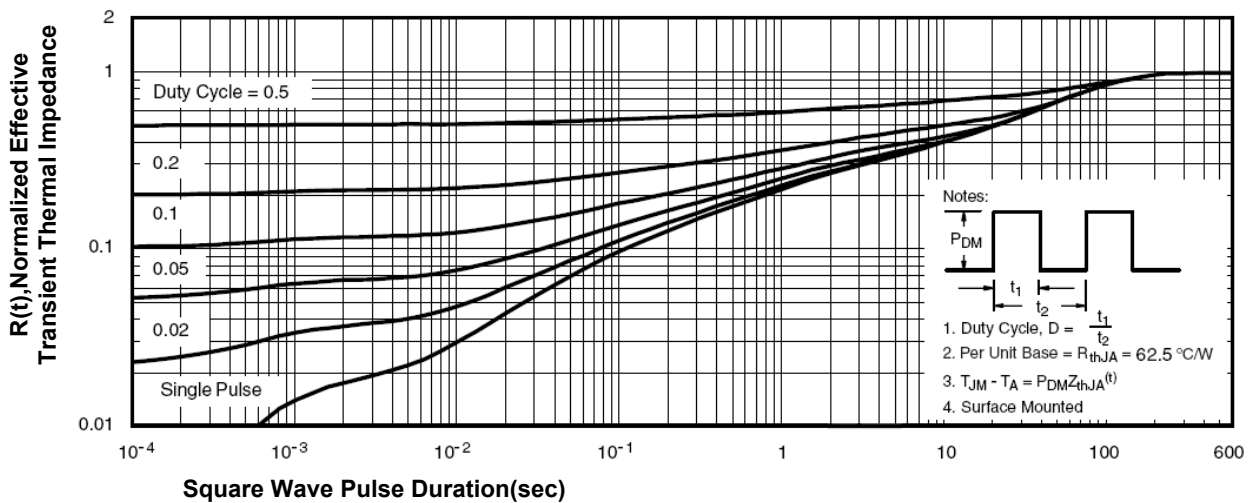


**Figure 12. Source- Drain Diode Forward**

**Typical Electrical and Thermal Characteristic Curves**

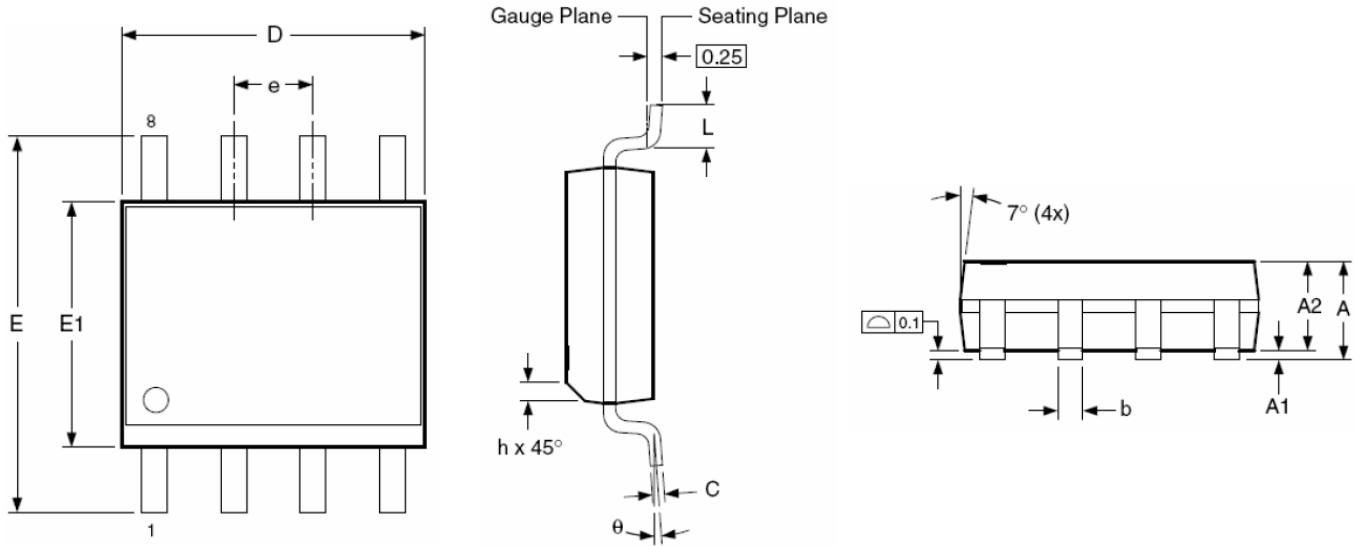


**Figure 13. Safe Operation Area**

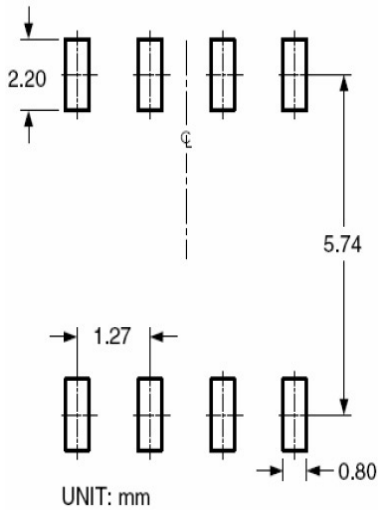


**Figure 14. Normalized Maximum Transient Thermal Impedance**

**Package Outline Dimensions (SOP-8 )**



**Recommended Pad Layout**



**Dimensions in millimeters**

Symbols	Min.	Nom.	Max.
A	1.35	1.65	1.75
A1	0.10	—	0.25
A2	1.25	1.50	1.65
b	0.31	—	0.51
c	0.17	—	0.25
D	4.80	4.90	5.00
E1	3.80	3.90	4.00
e	1.27 BSC		
E	5.80	6.00	6.20
h	0.25	—	0.50
L	0.40	—	1.27
θ	0°	—	8°

**Dimensions in inches**

Symbols	Min.	Nom.	Max.
A	0.053	0.065	0.069
A1	0.004	—	0.010
A2	0.049	0.059	0.065
b	0.012	—	0.020
c	0.007	—	0.010
D	0.189	0.193	0.197
E1	0.150	0.154	0.157
e	0.050 BSC		
E	0.228	0.236	0.244
h	0.010	—	0.020
L	0.016	—	0.050
θ	0°	—	8°

**NOTES:**

1. Dimensions are inclusive of plating
2. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 6 mils.
3. Dimension L is measured in gauge plane.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.