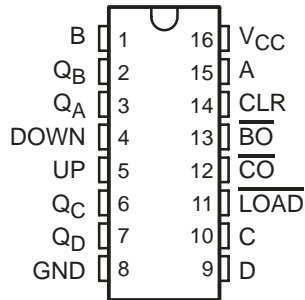


SN54HC193, SN74HC193 4-BIT SYNCHRONOUS UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

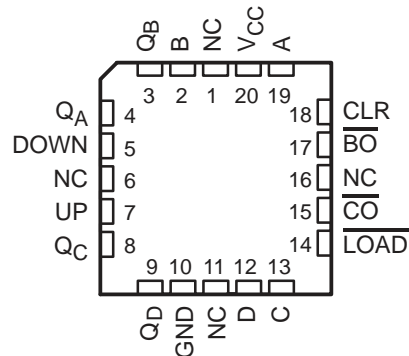
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- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 20$ ns
- ± 4 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- Look-Ahead Circuitry Enhances Cascaded Counters
- Fully Synchronous in Count Modes
- Parallel Asynchronous Load for Modulo-N Count Lengths
- Asynchronous Clear

SN54HC193 . . . J OR W PACKAGE
SN74HC193 . . . D, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC193 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The 'HC193 devices are 4-bit synchronous, reversible, up/down binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

ORDERING INFORMATION

| TA | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------|--------------|-----------------------|------------------|
| -40°C to 85°C | PDIP – N | Tube of 25 | SN74HC193N | SN74HC193N |
| | SOIC – D | Tube of 40 | SN74HC193D | HC193 |
| | | Reel of 2500 | SN74HC193DR | |
| | | Reel of 250 | SN74HC193DT | |
| | SOP – NS | Reel of 2000 | SN74HC193NSR | HC193 |
| | TSSOP – PW | Tube of 90 | SN74HC193PW | HC193 |
| Reel of 2000 | | SN74HC193PWR | | |
| Reel of 250 | | SN74HC193PWT | | |
| -55°C to 125°C | CDIP – J | Tube of 25 | SNJ54HC193J | SNJ54HC193J |
| | CFP – W | Tube of 150 | SNJ54HC193W | SNJ54HC193W |
| | LCCC – FK | Tube of 55 | SNJ54HC193FK | SNJ54HC193FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54HC193, SN74HC193 4-BIT SYNCHRONOUS UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

SCLS122D – DECEMBER 1982 – REVISED OCTOBER 2003

description/ordering information (continued)

The outputs of the four flip-flops are triggered on a low-to-high-level transition of either count (clock) input (UP or DOWN). The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load ($\overline{\text{LOAD}}$) input and entering the desired data at the data inputs. The output changes to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers simply by modifying the count length with the preset inputs.

A clear (CLR) input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and $\overline{\text{LOAD}}$ inputs.

These counters were designed to be cascaded without the need for external circuitry. The borrow ($\overline{\text{BO}}$) output produces a low-level pulse while the count is zero (all outputs low) and DOWN is low. Similarly, the carry ($\overline{\text{CO}}$) output produces a low-level pulse while the count is maximum (9 or 15), and UP is low. The counters then can be cascaded easily by feeding $\overline{\text{BO}}$ and $\overline{\text{CO}}$ to DOWN and UP, respectively, of the succeeding counter.

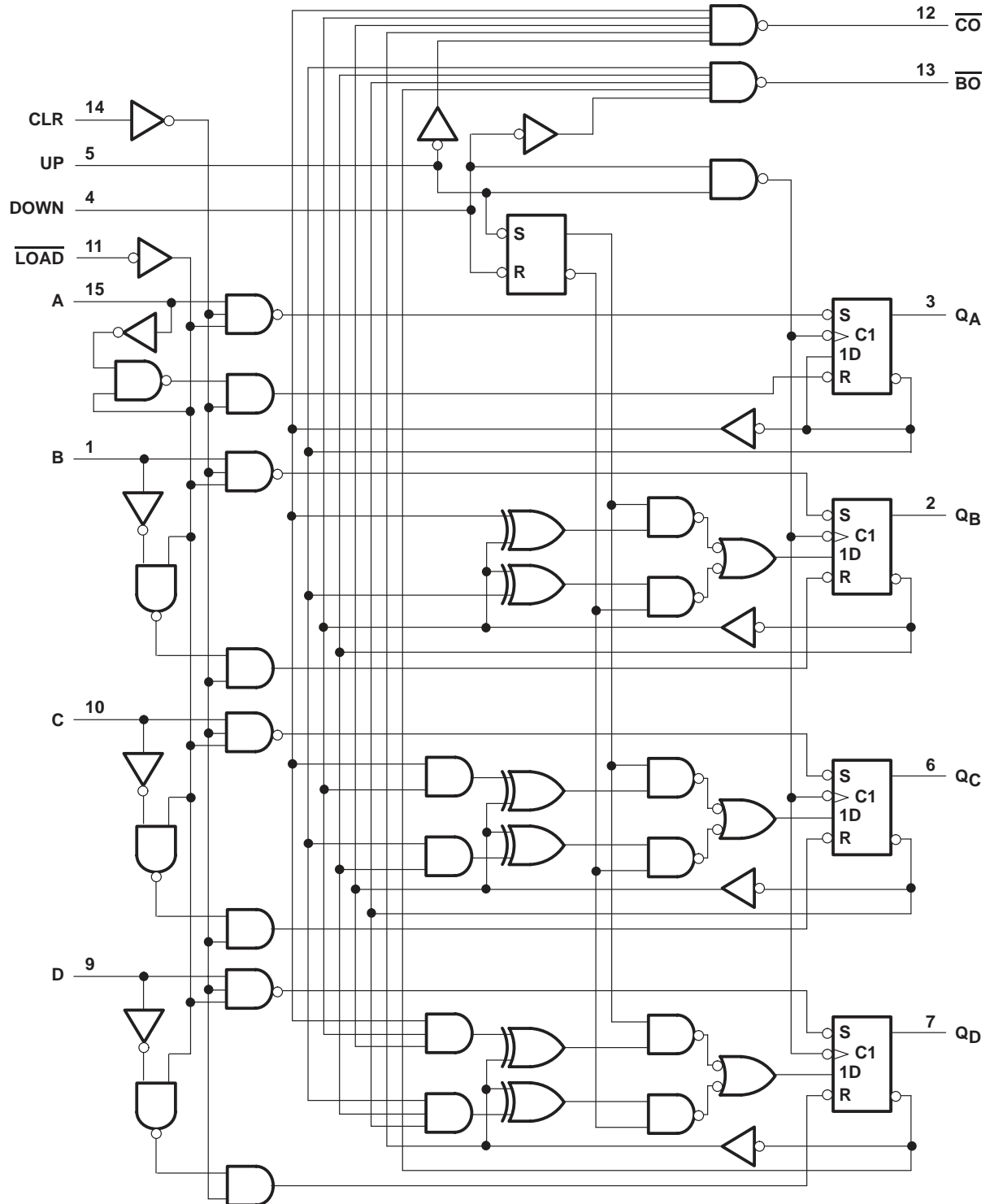


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SN54HC193, SN74HC193 4-BIT SYNCHRONOUS UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

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logic diagram (positive logic)



Pin numbers shown are for the D, J, N, NS, PW, and W packages.

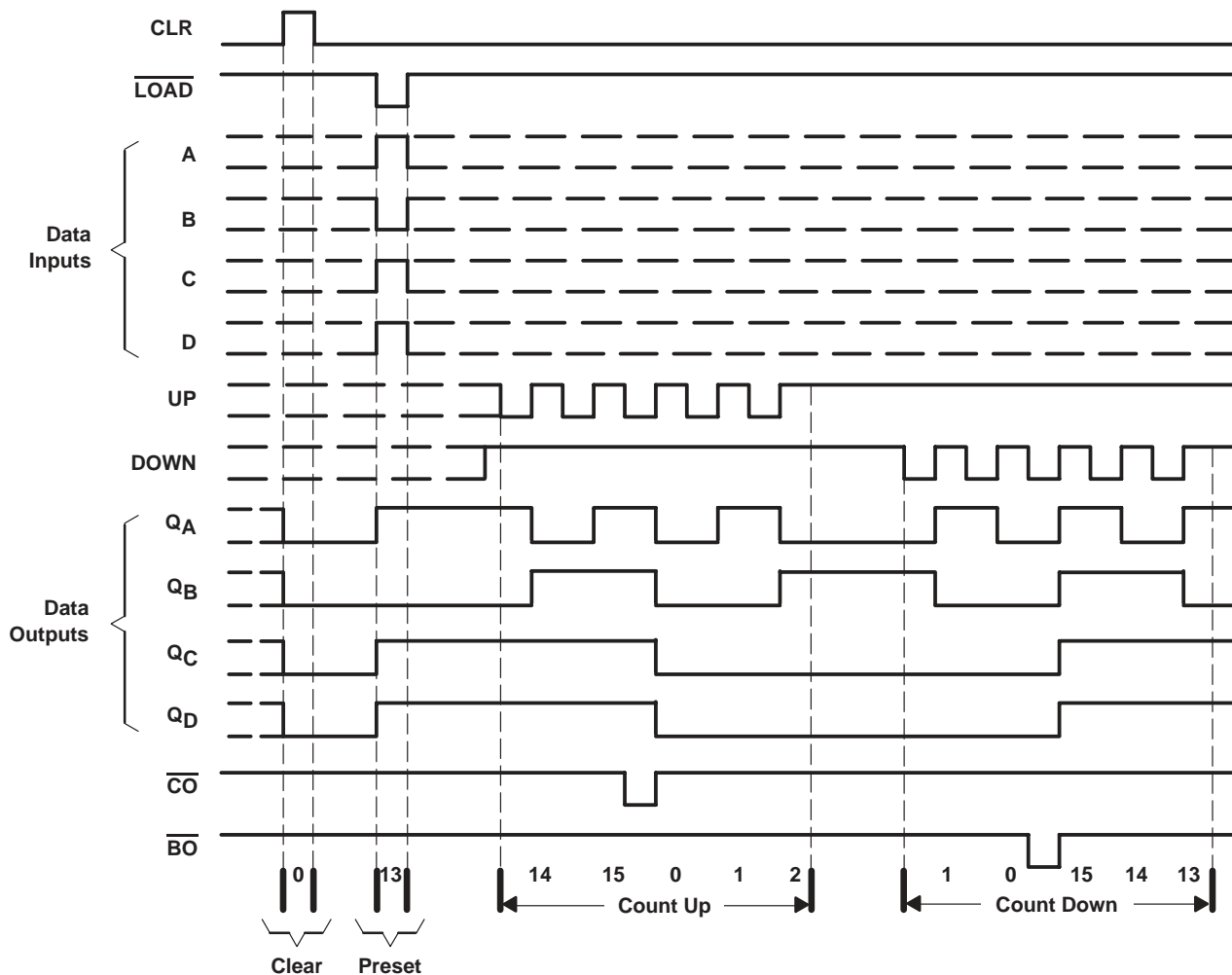
SN54HC193, SN74HC193 4-BIT SYNCHRONOUS UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

SCLS122D – DECEMBER 1982 – REVISED OCTOBER 2003

typical clear, load, and count sequence

The following sequence is illustrated below:

1. Clear outputs to 0
2. Load (preset) to binary 13
3. Count up to 14, 15, carry, 0, 1, and 2
4. Count down to 1, 0, borrow, 15, 14, and 13



- NOTES: A. CLR overrides $\overline{\text{LOAD}}$, data, and count inputs.
 B. When counting up, count-down input must be high; when counting down, count-up input must be high.

SN54HC193, SN74HC193 4-BIT SYNCHRONOUS UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

SCLS122D – DECEMBER 1982 – REVISED OCTOBER 2003

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|----------------|
| Supply voltage range, V_{CC} | –0.5 V to 7 V |
| Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) | ±20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) | ±20 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ±25 mA |
| Continuous current through V_{CC} or GND | ±50 mA |
| Package thermal impedance, θ_{JA} (see Note 2): D package | 73°C/W |
| N package | 67°C/W |
| NS package | 64°C/W |
| PW package | 108°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

| | | SN54HC193 | | | SN74HC193 | | | UNIT |
|-----------------------|---------------------------------|------------------|-----|----------|------------------|-----|----------|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 2 | 5 | 6 | 2 | 5 | 6 | V |
| V_{IH} | High-level input voltage | $V_{CC} = 2$ V | | 1.5 | $V_{CC} = 2$ V | | 1.5 | V |
| | | $V_{CC} = 4.5$ V | | 3.15 | $V_{CC} = 4.5$ V | | 3.15 | |
| | | $V_{CC} = 6$ V | | 4.2 | $V_{CC} = 6$ V | | 4.2 | |
| V_{IL} | Low-level input voltage | $V_{CC} = 2$ V | | | $V_{CC} = 2$ V | | 0.5 | V |
| | | $V_{CC} = 4.5$ V | | | $V_{CC} = 4.5$ V | | 1.35 | |
| | | $V_{CC} = 6$ V | | | $V_{CC} = 6$ V | | 1.8 | |
| V_I | Input voltage | 0 | | V_{CC} | 0 | | V_{CC} | V |
| V_O | Output voltage | 0 | | V_{CC} | 0 | | V_{CC} | V |
| $\Delta t/\Delta v$ ‡ | Input transition rise/fall time | $V_{CC} = 2$ V | | | $V_{CC} = 2$ V | | 1000 | ns |
| | | $V_{CC} = 4.5$ V | | | $V_{CC} = 4.5$ V | | 500 | |
| | | $V_{CC} = 6$ V | | | $V_{CC} = 6$ V | | 400 | |
| T_A | Operating free-air temperature | –55 | | 125 | –40 | | 85 | °C |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

‡ If this device is used in the threshold region (from $V_{ILmax} = 0.5$ V to $V_{IHmin} = 1.5$ V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at $t_f = 1000$ ns and $V_{CC} = 2$ V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.



SN54HC193, SN74HC193
4-BIT SYNCHRONOUS UP/DOWN COUNTERS
(DUAL CLOCK WITH CLEAR)

SCLS122D – DECEMBER 1982 – REVISED OCTOBER 2003

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | V _{CC} | T _A = 25°C | | | SN54HC193 | | SN74HC193 | | UNIT |
|-----------------|---|--------------------------|-----------------|-----------------------|-------|------|-----------|-------|-----------|-------|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | V _I = V _{IH} or V _{IL} | I _{OH} = -20 μA | 2 V | 1.9 | 1.998 | | 1.9 | | 1.9 | V | |
| | | | 4.5 V | 4.4 | 4.499 | | 4.4 | | 4.4 | | |
| | | | 6 V | 5.9 | 5.999 | | 5.9 | | 5.9 | | |
| | | I _{OH} = -4 mA | 4.5 V | 3.98 | 4.3 | | 3.7 | | 3.84 | | |
| | | | 6 V | 5.48 | 5.8 | | 5.2 | | 5.34 | | |
| V _{OL} | V _I = V _{IH} or V _{IL} | I _{OL} = 20 μA | 2 V | | 0.002 | 0.1 | | 0.1 | | V | |
| | | | 4.5 V | | 0.001 | 0.1 | | 0.1 | | | 0.1 |
| | | | 6 V | | 0.001 | 0.1 | | 0.1 | | | 0.1 |
| | | I _{OL} = 4 mA | 4.5 V | | 0.17 | 0.26 | | 0.4 | | | 0.33 |
| | | | 6 V | | 0.15 | 0.26 | | 0.4 | | | 0.33 |
| I _I | V _I = V _{CC} or 0 | | 6 V | | ±0.1 | ±100 | | ±1000 | | ±1000 | nA |
| I _{CC} | V _I = V _{CC} or 0, I _O = 0 | | 6 V | | | 8 | | 160 | | 80 | μA |
| C _i | | | 2 V to 6 V | | 3 | 10 | | 10 | | 10 | pF |

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

| | | V _{CC} | T _A = 25°C | | SN54HC193 | | SN74HC193 | | UNIT |
|--------------------|-----------------------------------|-----------------|-----------------------|-----|-----------|-----|-----------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| f _{clock} | Clock frequency | 2 V | | 4.2 | | 2.8 | | 3.3 | MHz |
| | | 4.5 V | | 21 | | 14 | | 17 | |
| | | 6 V | | 24 | | 16 | | 19 | |
| t _w | CLR high | 2 V | | 120 | | 180 | | 150 | ns |
| | | 4.5 V | | 24 | | 36 | | 30 | |
| | | 6 V | | 21 | | 31 | | 26 | |
| | LOAD low | 2 V | | 120 | | 180 | | 150 | |
| | | 4.5 V | | 24 | | 36 | | 30 | |
| | | 6 V | | 21 | | 31 | | 26 | |
| | UP or DOWN high or low | 2 V | | 120 | | 180 | | 150 | |
| | | 4.5 V | | 24 | | 36 | | 30 | |
| | | 6 V | | 21 | | 31 | | 26 | |
| t _{su} | Data before LOAD inactive | 2 V | | 110 | | 165 | | 140 | ns |
| | | 4.5 V | | 22 | | 33 | | 28 | |
| | | 6 V | | 19 | | 28 | | 24 | |
| | CLR inactive before UP↑ or DOWN↑ | 2 V | | 110 | | 165 | | 140 | |
| | | 4.5 V | | 22 | | 33 | | 28 | |
| | | 6 V | | 19 | | 28 | | 24 | |
| | LOAD inactive before UP↑ or DOWN↑ | 2 V | | 110 | | 165 | | 140 | |
| | | 4.5 V | | 22 | | 33 | | 28 | |
| | | 6 V | | 19 | | 28 | | 24 | |
| t _h | Data after LOAD inactive | 2 V | | 5 | | 5 | | 5 | ns |
| | | 4.5 V | | 5 | | 5 | | 5 | |
| | | 6 V | | 5 | | 5 | | 5 | |



SN54HC193, SN74HC193
4-BIT SYNCHRONOUS UP/DOWN COUNTERS
(DUAL CLOCK WITH CLEAR)

SCLS122D – DECEMBER 1982 – REVISED OCTOBER 2003

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} | T _A = 25°C | | | SN54HC193 | | SN74HC193 | | UNIT |
|------------------|-------------------|-----------------|-----------------|-----------------------|-----|-----|-----------|-----|-----------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| f _{max} | | | 2 V | 4.2 | 8 | | 2.8 | | 3.3 | MHz | |
| | | | 4.5 V | 21 | 55 | | 14 | | 17 | | |
| | | | 6 V | 24 | 60 | | 16 | | 19 | | |
| t _{pd} | UP | \overline{CO} | 2 V | | 75 | 165 | | 250 | | 205 | ns |
| | | | 4.5 V | | 24 | 33 | | 50 | | 41 | |
| | | | 6 V | | 20 | 28 | | 43 | | 35 | |
| | DOWN | \overline{BO} | 2 V | | 75 | 165 | | 250 | | 205 | |
| | | | 4.5 V | | 24 | 33 | | 50 | | 41 | |
| | | | 6 V | | 20 | 28 | | 43 | | 35 | |
| | UP or DOWN | Any Q | 2 V | | 190 | 250 | | 375 | | 315 | |
| | | | 4.5 V | | 40 | 50 | | 75 | | 63 | |
| | | | 6 V | | 35 | 43 | | 64 | | 54 | |
| | \overline{LOAD} | Any Q | 2 V | | 190 | 260 | | 390 | | 325 | |
| | | | 4.5 V | | 40 | 52 | | 78 | | 65 | |
| | | | 6 V | | 35 | 44 | | 66 | | 55 | |
| t _{PHL} | CLR | Any Q | 2 V | | 170 | 240 | | 360 | | 300 | ns |
| | | | 4.5 V | | 36 | 48 | | 72 | | 60 | |
| | | | 6 V | | 31 | 41 | | 61 | | 51 | |
| t _t | | Any | 2 V | | 38 | 75 | | 110 | | 95 | ns |
| | | | 4.5 V | | 8 | 15 | | 22 | | 19 | |
| | | | 6 V | | 6 | 13 | | 19 | | 16 | |

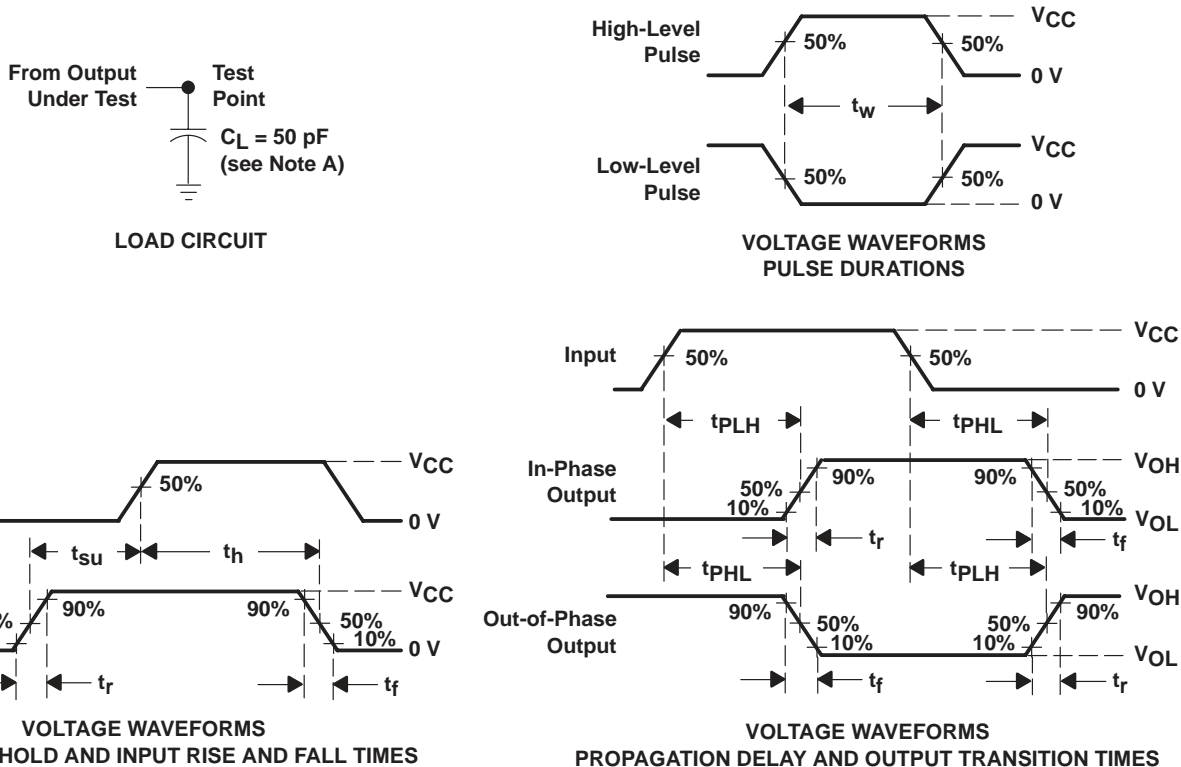
operating characteristics, T_A = 25°C

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|---|-----------------|-----|------|
| C _{pd} Power dissipation capacitance | No load | 50 | pF |

SN54HC193, SN74HC193 4-BIT SYNCHRONOUS UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

SCLS122D – DECEMBER 1982 – REVISED OCTOBER 2003

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
 - C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|-------------------------------|-------------------------|
| 5962-8772401EA | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8772401EA SNJ54HC193J | Samples |
| SN54HC193J | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SN54HC193J | Samples |
| SN74HC193D | ACTIVE | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC193 | Samples |
| SN74HC193DR | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC193 | Samples |
| SN74HC193N | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | SN74HC193N | Samples |
| SN74HC193NE4 | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | SN74HC193N | Samples |
| SN74HC193NSR | ACTIVE | SO | NS | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC193 | Samples |
| SN74HC193PW | ACTIVE | TSSOP | PW | 16 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC193 | Samples |
| SN74HC193PWR | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC193 | Samples |
| SNJ54HC193J | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8772401EA SNJ54HC193J | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54HC193, SN74HC193 :

- Catalog : [SN74HC193](#)
- Automotive : [SN74HC193-Q1](#), [SN74HC193-Q1](#)
- Military : [SN54HC193](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

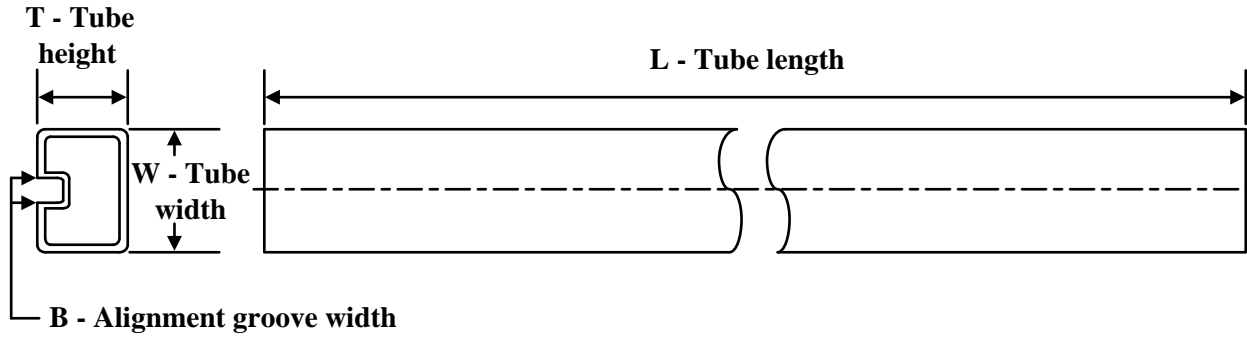
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74HC193DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC193NSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74HC193PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HC193DR | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |
| SN74HC193NSR | SO | NS | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74HC193PWR | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|--------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74HC193D | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| SN74HC193N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC193N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC193NE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC193NE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC193PW | PW | TSSOP | 16 | 90 | 530 | 10.2 | 3600 | 3.5 |

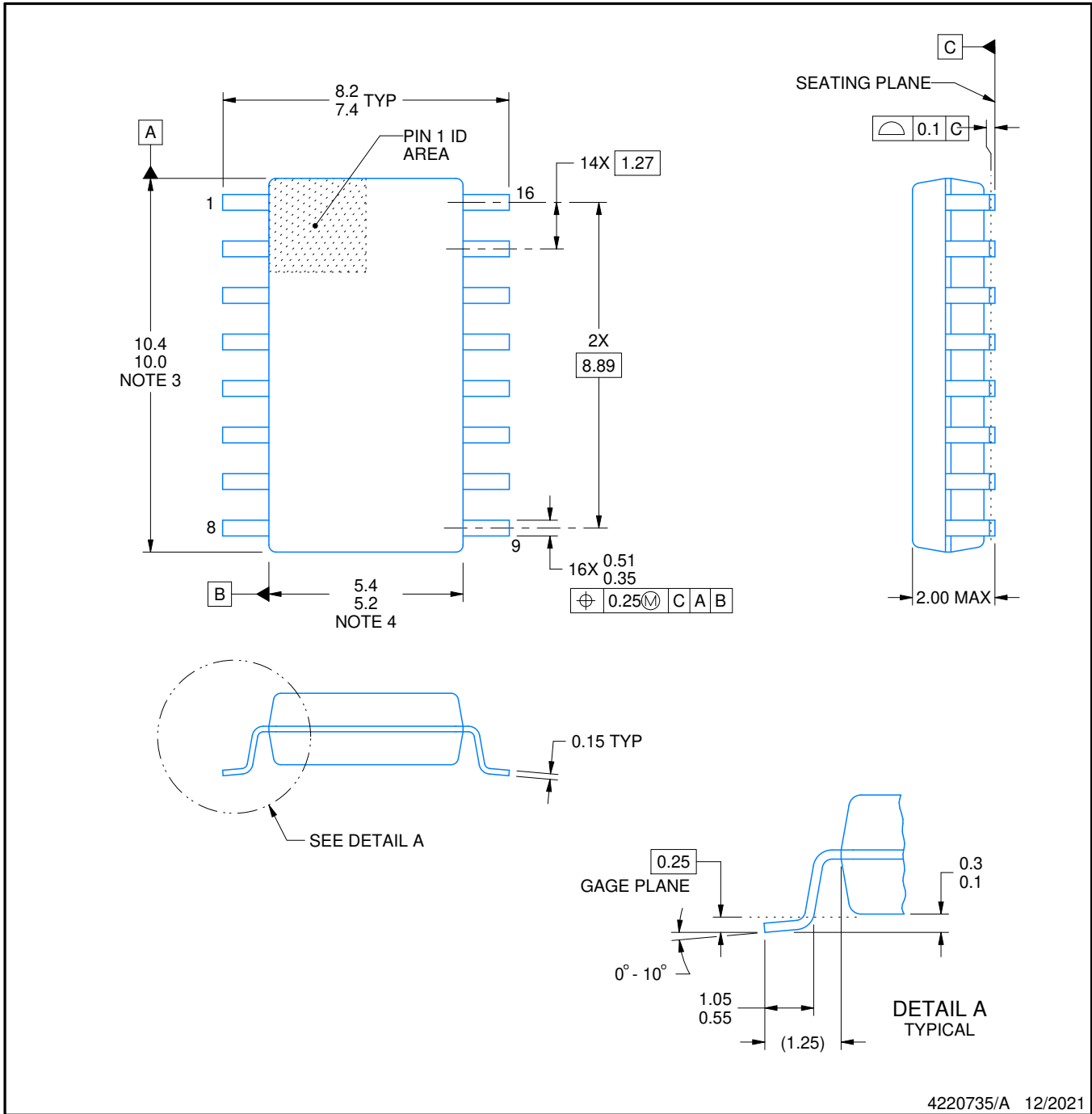


PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



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NOTES:

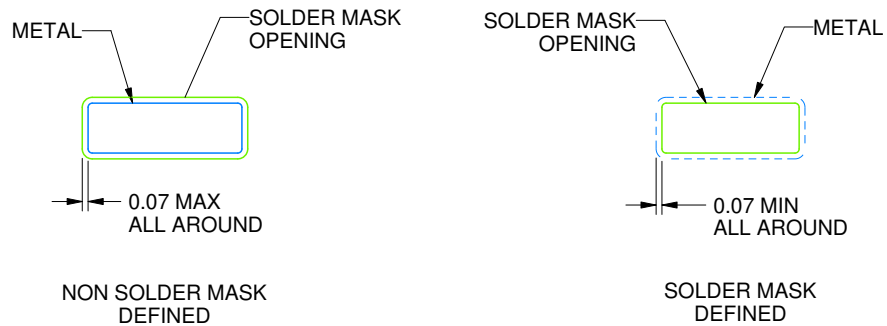
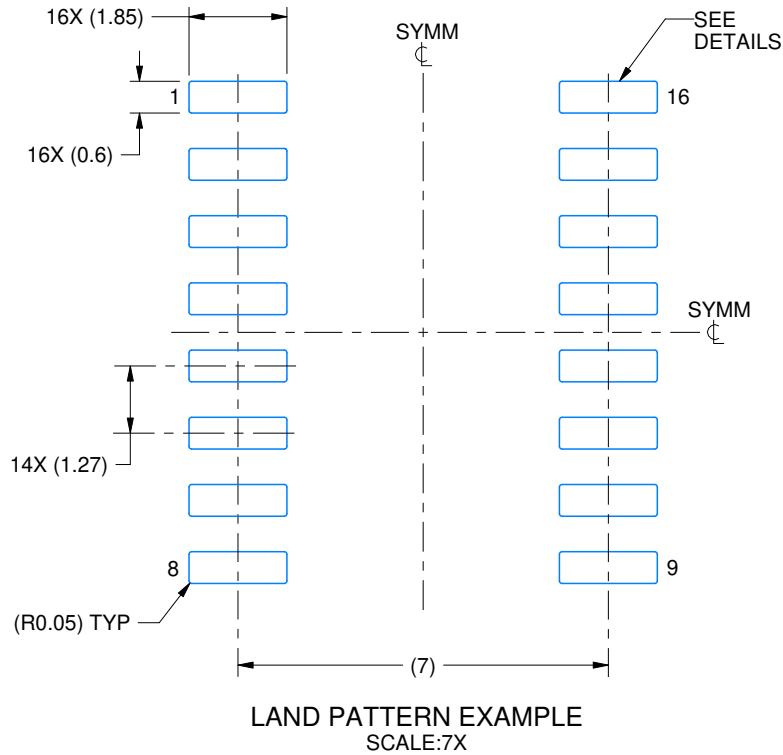
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER MASK DETAILS

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NOTES: (continued)

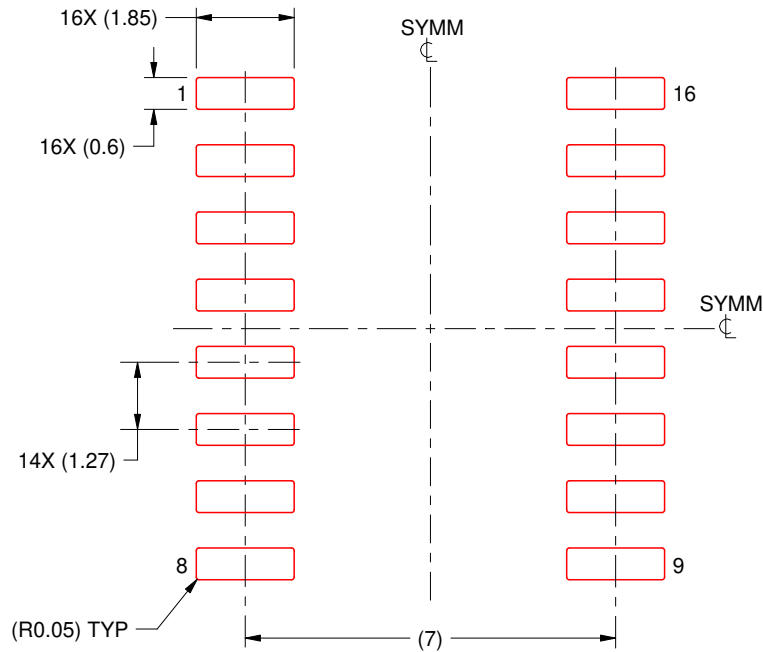
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

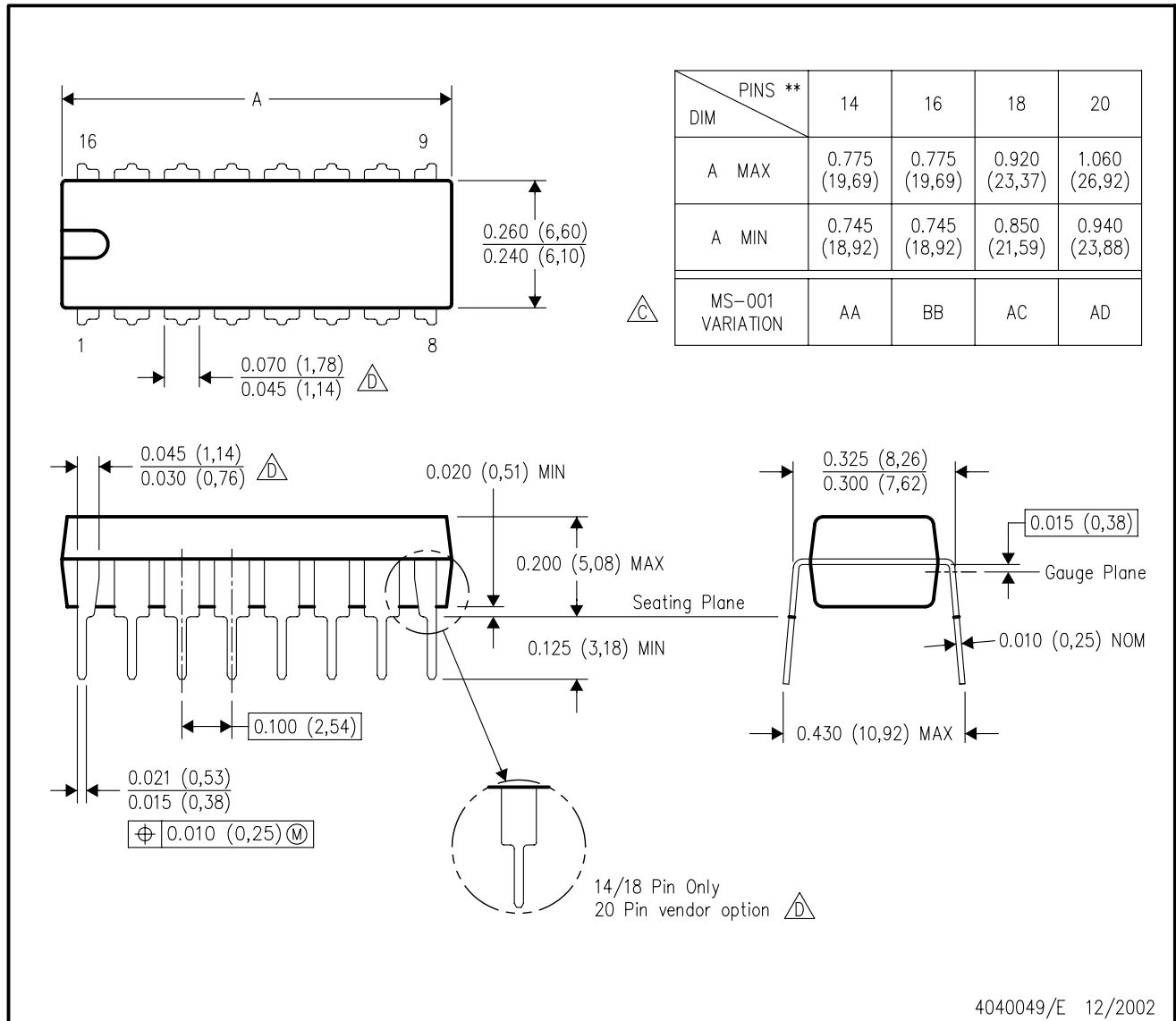
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

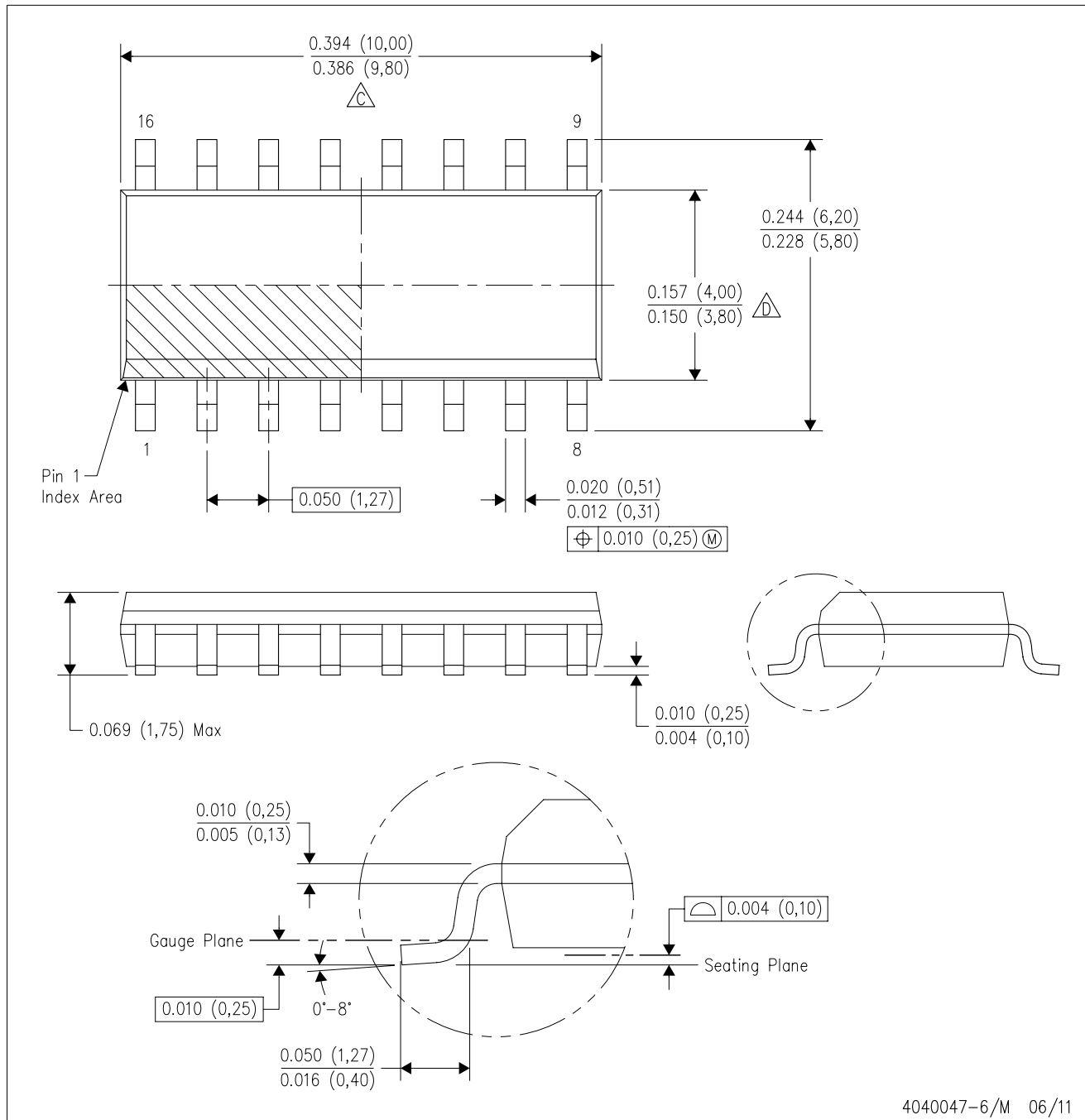
16 PINS SHOWN



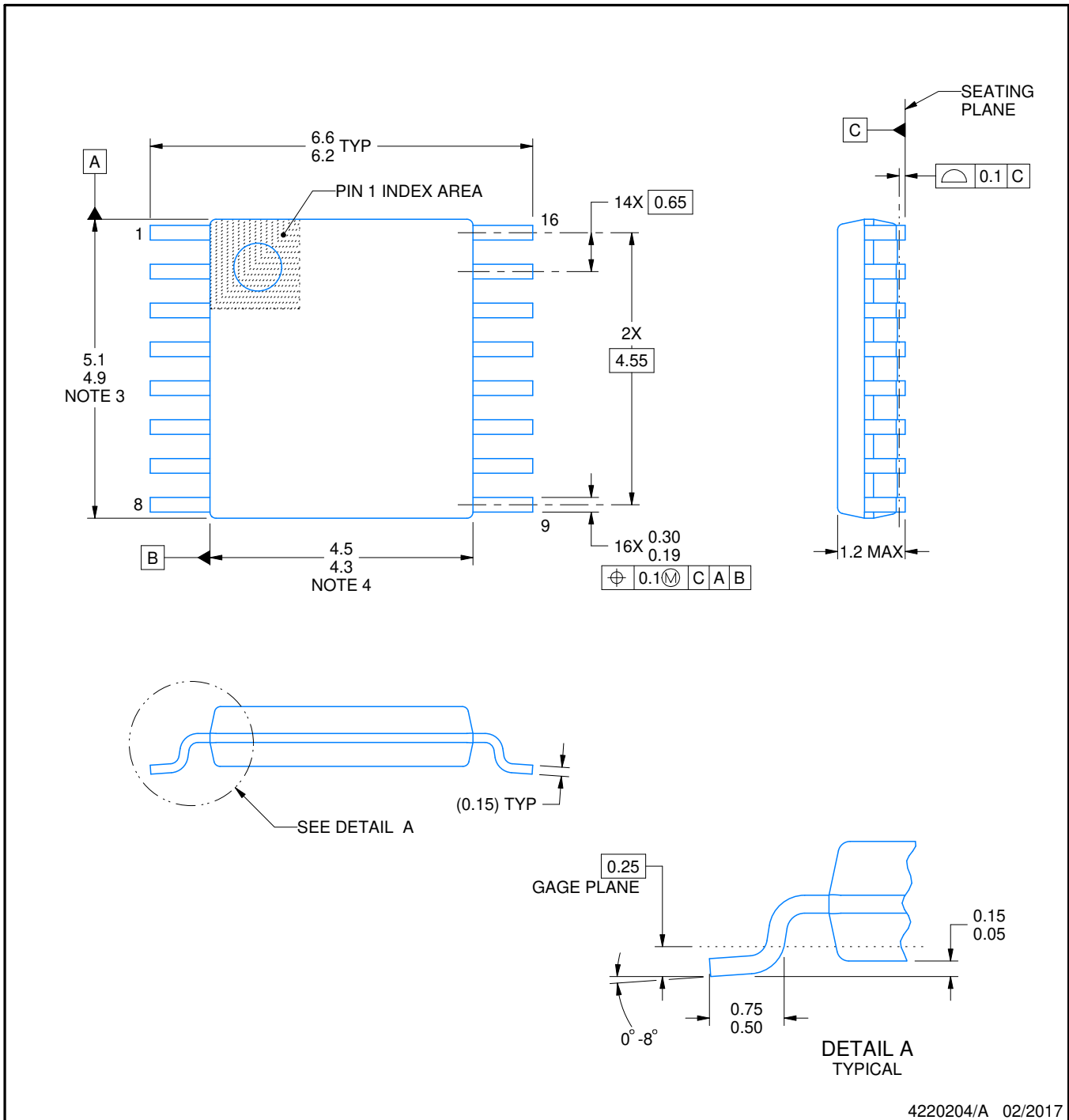
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

NOTES:

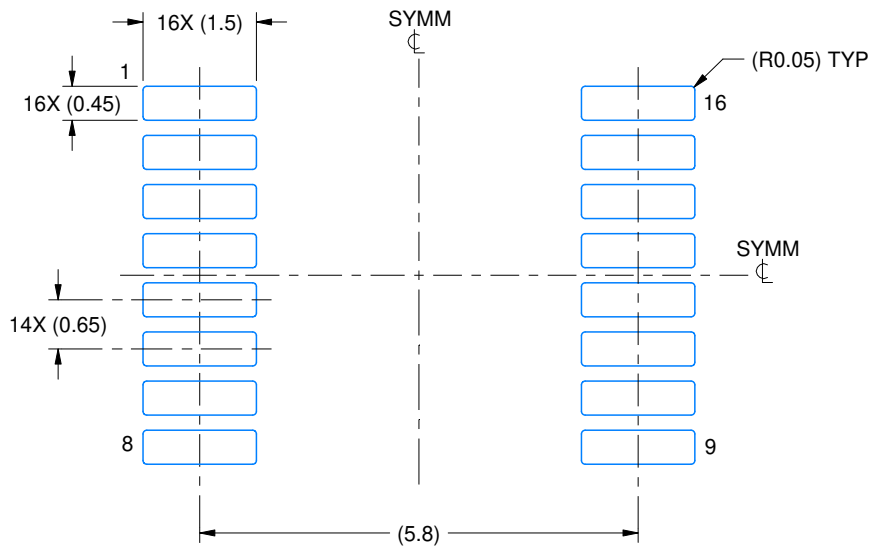
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

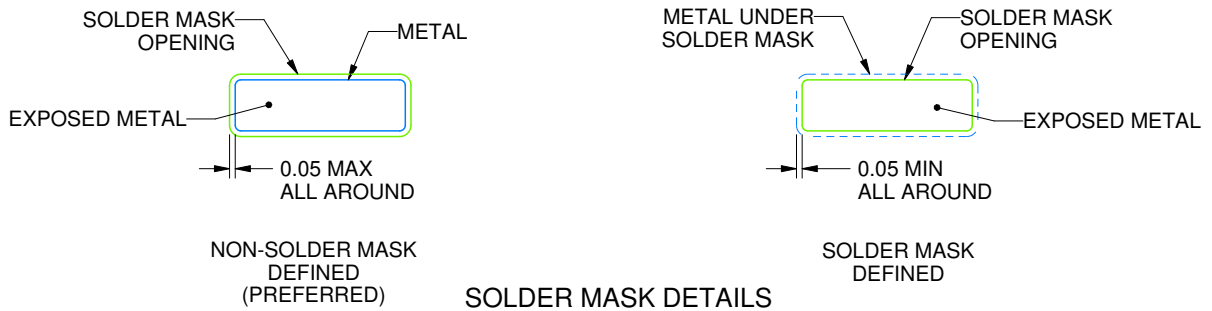
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

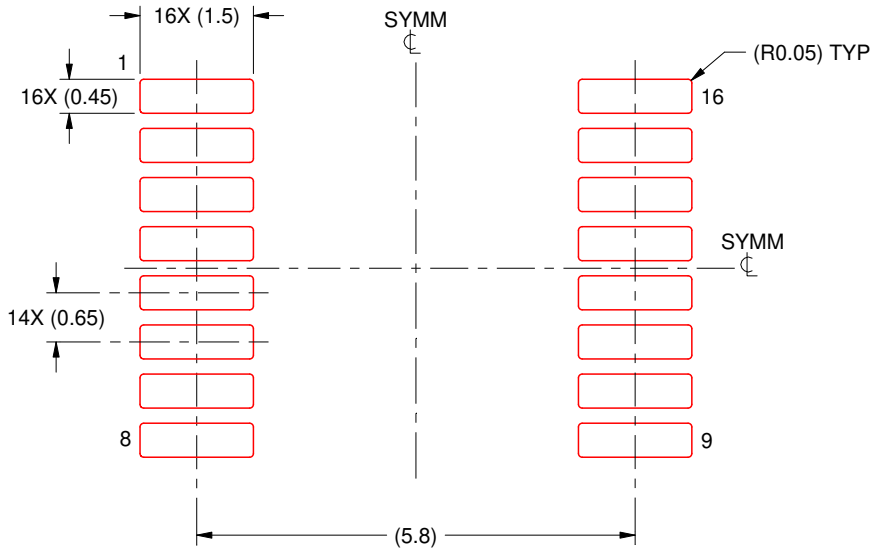
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

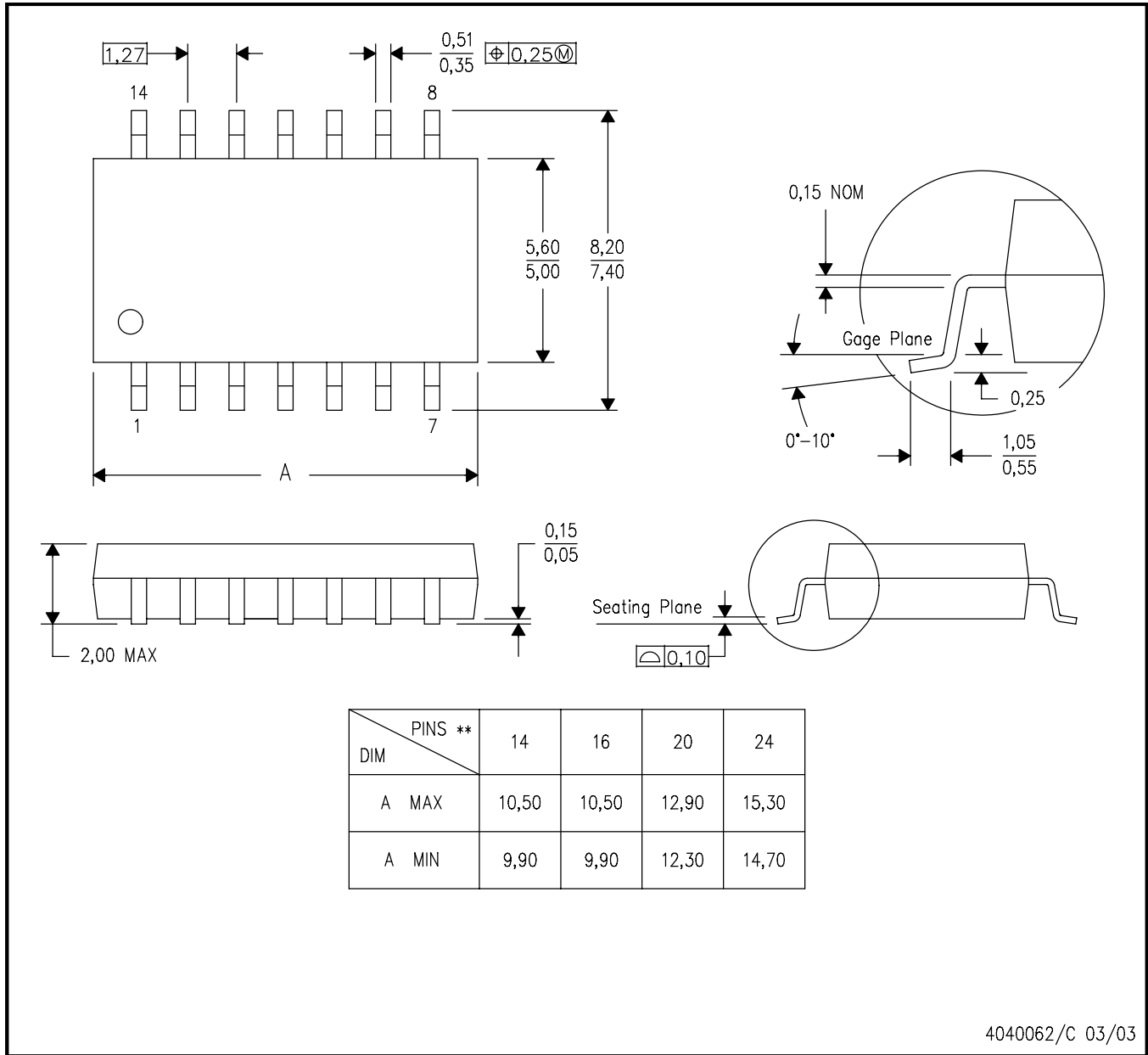
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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