

## Features

- ESD/Surge protection for two lines with bi-directional
- Provide transient protection for each line to  
**IEC 61000-4-2 (ESD)  $\pm 30\text{kV}$  (air),  $\pm 30\text{kV}$  (contact)**  
**IEC 61000-4-4 (EFT) 80A (5/50ns)**  
**IEC 61000-4-5 (Lightning) 6.5A (8/20 $\mu\text{s}$ )**
- Suitable for, 24V and below, operating voltage applications
- Fast turn-on and low clamping voltage
- Array of ESD rated equivalent TVS diodes
- Small package saves board space
- Solid-state silicon-avalanche and active circuit triggering technology
- **Green part**

## Applications

- CAN bus protection
- Industrial control
- Power management system
- Set-top box
- Notebooks, desktops, and servers
- Portable instrumentation
- Peripherals

## Description

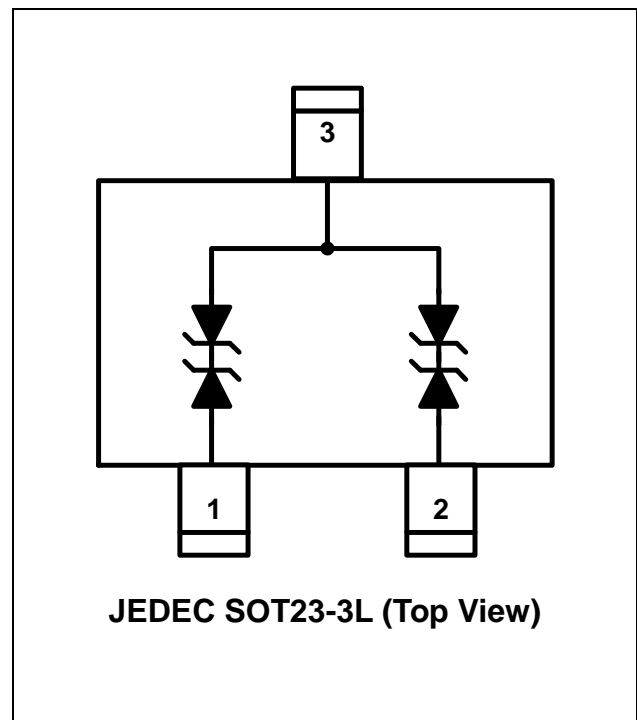
AZ4824-02S is a design which includes ESD /EFT/surge rated clamping cell arrays to protect the power lines or control lines in an electronic system. The AZ4824-02S has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT),

Lightning, and Cable Discharge Event (CDE).

AZ4824-02S is a unique design which includes proprietary clamping cells in a single package. During transient conditions, the proprietary clamping cells prevent over-voltage on the power lines or control lines, protecting any downstream components.

AZ4824-02S may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ( $\pm 15\text{kV}$  air,  $\pm 8\text{kV}$  contact discharge).

## Circuit Diagram / Pin Configuration





## SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ , unless otherwise specified)			
PARAMETER	SYMBOL	RATING	UNIT
Peak Pulse Current ( $t_p=8/20\mu\text{s}$ )	$I_{PP}$	6.5	A
Operating Voltage (pin-1, -2 to pin-3)	$V_{DC}$	$\pm 26$	V
ESD per IEC 61000-4-2 (Air)	$V_{ESD-1}$	$\pm 30$	kV
ESD per IEC 61000-4-2 (Contact)	$V_{ESD-2}$	$\pm 30$	
Lead Soldering Temperature	$T_{SOL}$	260 (10 sec.)	$^\circ\text{C}$
Operating Temperature	$T_{OP}$	-55 to +125	$^\circ\text{C}$
Storage Temperature	$T_{STO}$	-55 to +150	$^\circ\text{C}$

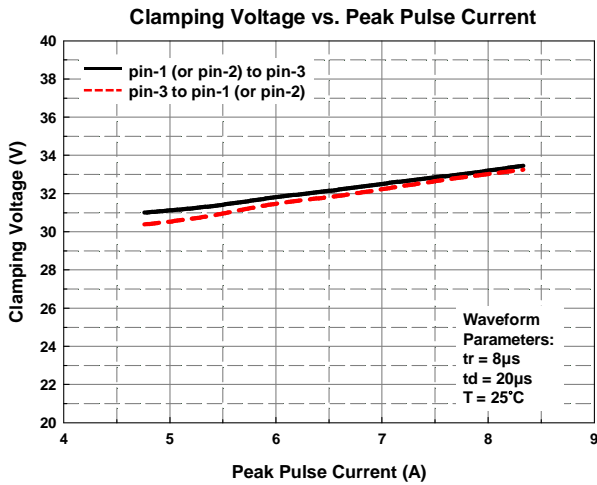
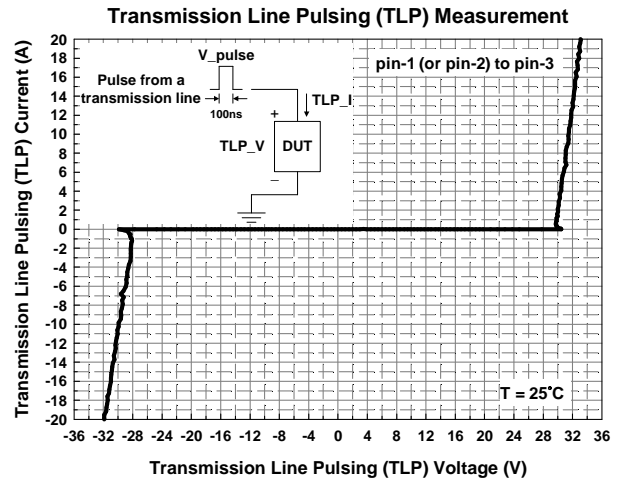
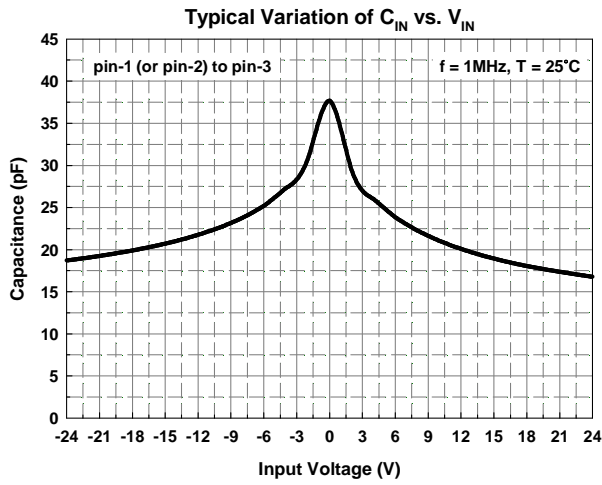
ELECTRICAL CHARACTERISTICS						
PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Reverse Stand-Off Voltage	$V_{RWM}$	Pin-1, -2 to pin-3, $T=25^\circ\text{C}$ .	-24		24	V
Reverse Leakage Current	$I_{Leak}$	$V_{RWM} = \pm 24\text{V}$ , pin-1, -2 to pin-3, $T=25^\circ\text{C}$ .			100	nA
Reverse Breakdown Voltage	$V_{BV}$	$I_{BV} = 1\text{mA}$ , pin-1, -2 to pin-3, $T=25^\circ\text{C}$ .	26.2		33.5	V
Surge Clamping Voltage	$V_{CL-surge}$	$I_{PP} = 5\text{A}$ , $t_p = 8/20\mu\text{s}$ , pin-1, -2 to pin-3, $T=25^\circ\text{C}$ .		32		V
ESD Clamping Voltage (Note 1)	$V_{CL-ESD}$	IEC 61000-4-2 +8kV ( $I_{TLP} = 16\text{A}$ ), contact mode, pin-1, -2 to pin-3, $T=25^\circ\text{C}$ .		32		V
ESD Dynamic Turn-on Resistance	$R_{dynamic}$	IEC 61000-4-2 0~+8kV, contact mode, pin-1, -2 to pin-3, $T=25^\circ\text{C}$ .		0.2		$\Omega$
Channel Input Capacitance	$C_{IN}$	$V_R = 0\text{V}$ , $f = 1\text{MHz}$ , pin-1, -2 to pin-3, $T=25^\circ\text{C}$ .		38	45	pF

Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

TLP conditions:  $Z_0 = 50\Omega$ ,  $t_p = 100\text{ns}$ ,  $t_r = 1\text{ns}$ .



## Typical Characteristics



## Application Information

The AZ4824-02S is designed to protect two lines against system ESD/EFT/Lightning pulses by clamping it to an acceptable reference. It provides bi-directional protection.

The usage of the AZ4824-02S is shown in Fig. 1. Protected lines, such as data lines, control lines, or power lines, are connected at pin 1 and pin 2, respectively. The pin 3 is connected to a ground plane on the board. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ4824-02S should be kept as short as possible.

In order to obtain enough suppression of

ESD induced transient, a good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ4824-02S.
- Place the AZ4824-02S near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

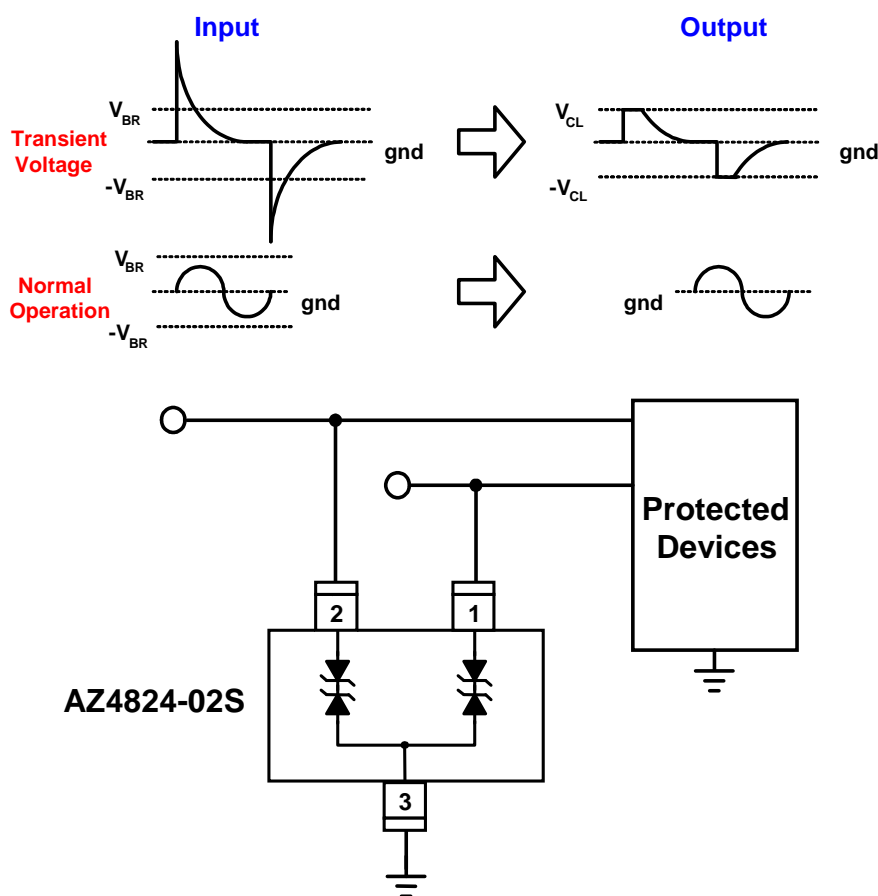
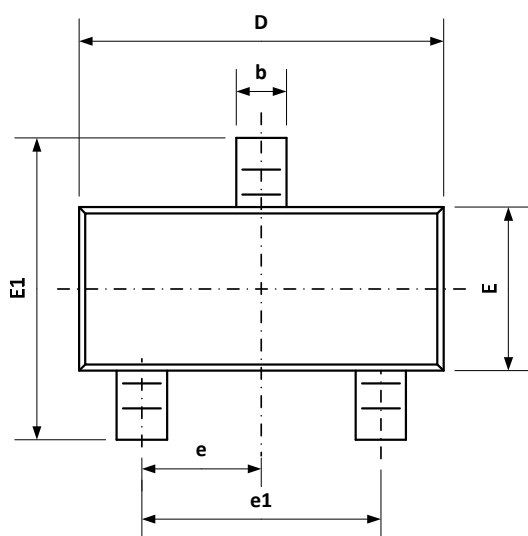


Fig. 1 ESD protection scheme by using AZ4824-02S.

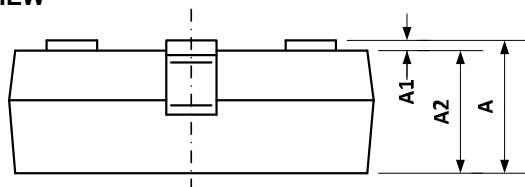
## Mechanical Details

### SOT23-3L PACKAGE DIAGRAMS

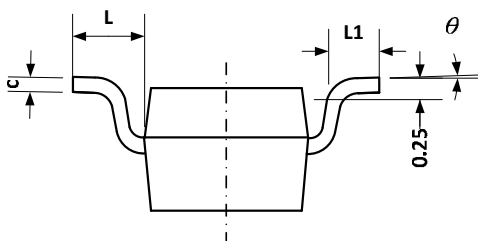
TOP VIEW



SIDE VIEW



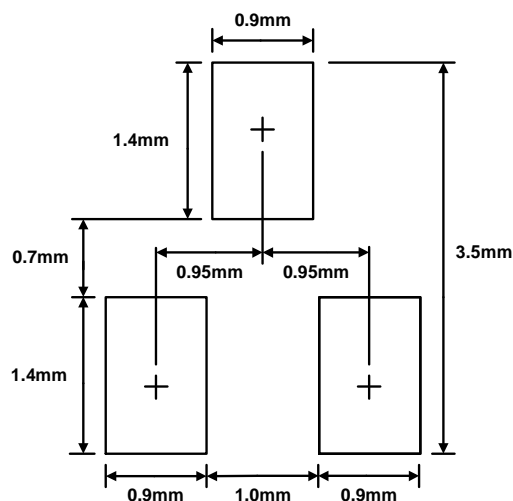
END VIEW



### PACKAGE DIMENSIONS

SYMBOL	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.15
A1	0.00	0.10
A2	0.90	1.05
b	0.30	0.50
c	0.08	0.15
D	2.80	3.00
E	1.20	1.40
E1	2.25	2.55
e	0.95 TYP	
e1	1.80	2.00
L	0.55 REF	
L1	0.30	0.50
$\theta$	0	8

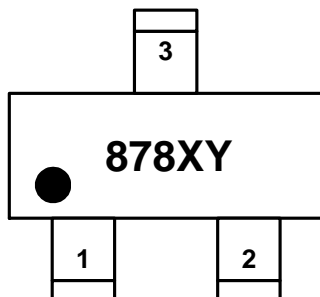
### LAND LAYOUT



#### Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

## MARKING CODE



878 = Device Code  
X = Date Code  
Y = Control Code

Part Number	Marking Code
AZ4824-02S.R7G (Green Part)	<b>878XY</b>

Note. Green means Pb-free, RoHS, and Halogen free compliant.

## Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ4824-02S.R7G	Green	T/R	7 inch	3,000/reel	4 reels=12,000/box	6 boxes=72,000/carton

## Revision History

Revision	Modification Description
Revision 2019/02/15	Formal Release.