Converter Evaluation and Development (CED) Board

Preliminary Technical Data

EVAL-CED1Z

FEATURES

Interfaces to multiple serial and parallel precision converter evaluation boards
Supports high-speed LVDS interface
32MB SDRAM
4MB SRAM
USB 2.0 connection to PC
User reprogrammable Altera Cyclone FPGA
Provides 8 separate power supplies
Connects directly to Blackfin Ez-Kit

APPLICATIONS

Evaluating Precision Converters
Creation of demonstration systems
Prototyping of end-user systems

GENERAL DESCRIPTION

The CED1 board is part of a next generation platform from Analog Devices Inc., intended for use in evaluation, demonstration and development of systems using Analog Devices precision converters. It provides the necessary communications between the converter and the PC, programming or controlling the device, transmitting or receiving data over a USB link.

PACKAGE CONTENTS

- CED Board
- USB A to Mini-B cable
- 7 Volt 15W Power Supply

.

FUNCTIONAL BLOCK DIAGRAM

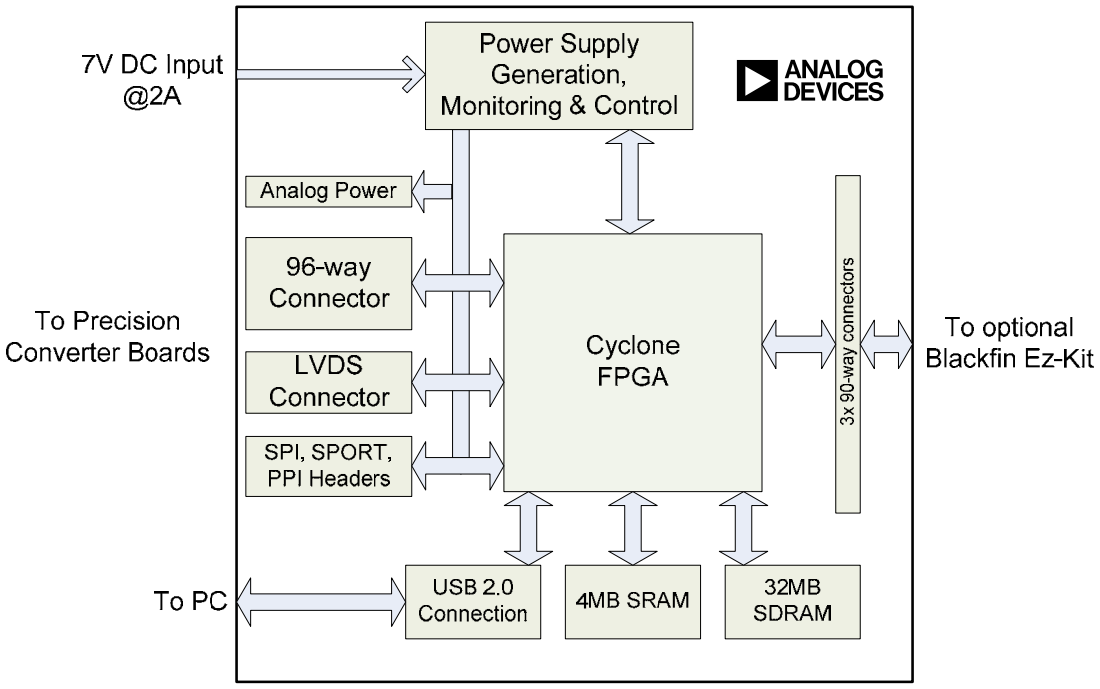

Figure 1.

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Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

7/07—Revision 0: Initial Revision

GENERAL DESCRIPTION

The Converter Evaluation and Development board is intended to assist system designers evaluate and prototype systems utilizing precision converter components from Analog Devices. It provides a means to read and write data, control and program devices from a PC via a high-speed USB 2.0 connection.

Due to its design, the CED1 can handle interfacing to multiple devices simultaneously for users who may wish to prototype their system utilizing proven hardware components from Analog Devices.

The reconfigurable FPGA-based architecture of the board allows the FPGA to be reprogrammed at any time via the USB connection. This allows the user to develop and run their own code to accomplish their desired task.

The many interfacing options accommodate connection to a wide range of precision converter evaluation boards in different form factors. Three standard 0.1-inch pitch headers are available, supporting SPI, SPORT and parallel functionality. A 96-way connector provides links to multiple interfaces and power supplies simultaneously. LVDS is supported through a dedicated connector designed for data pairs with individual grounds.

For developments that require a processor as well as an FPGA, the CED1 board provides the means to connect directly to a Blackfin EZ-Kit. Three 90-way connectors present on the board mate directly with the Blackfin Ez-Kit allowing the development of very powerful systems and demonstrations.

To help minimize the amount of external equipment needed to run a system successfully, the CED board provides eight separate power supplies made available for external connection. The details of these supplies and their current ratings are contained in the Power Supply section of this document.

The CED board requires a single 7V, 15W supply which ships with the board. The user may also connect a bench-top supply providing it can source a minimum current of 2A.

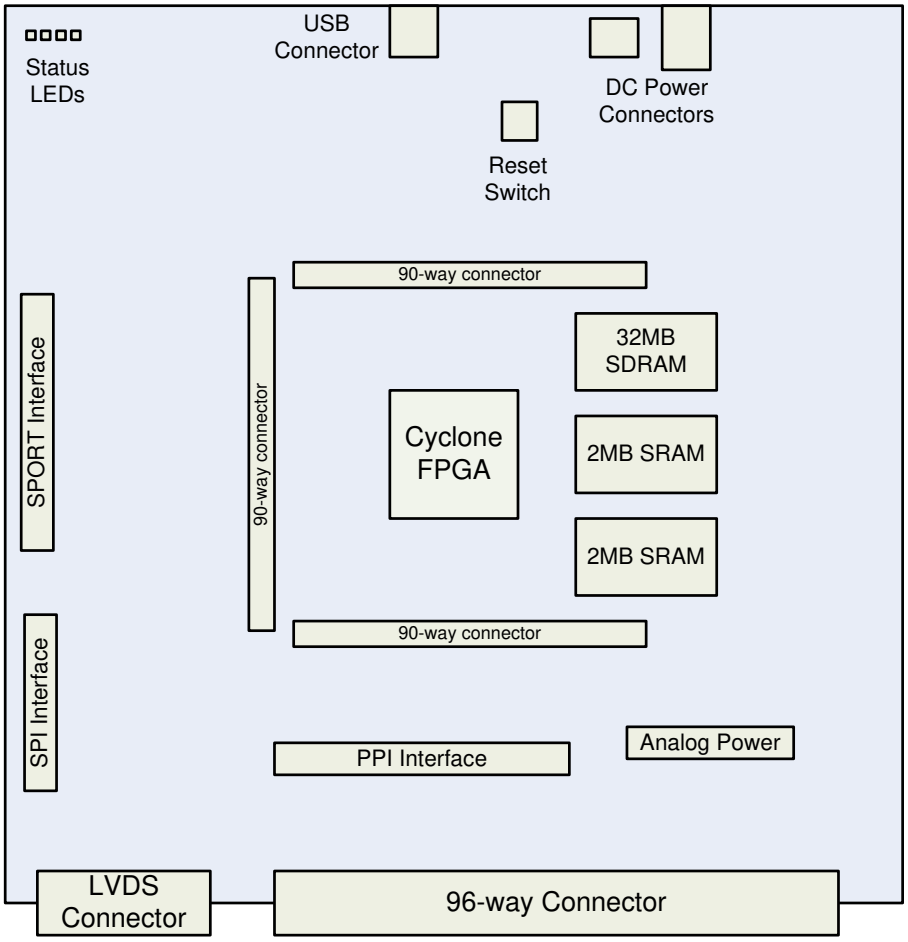


Figure 2. Major Component Locations

CONNECTORS

Many connectors are provided on the CED board to facilitate design and attachment of a range of different form factor converter boards. Due to the number of connections available on the FPGA, certain signals on different connectors are shared and replicated across different connectors.

All signals have been named to assist the user in identifying the shared signals and to which group they belong. SPI signals begin with SPI_xxx, SPORT signals begin with SPORT_xxx and parallel/PPI signals begin with PAR_xxx/PPI_xxx. More details of these signals are given in the relevant connector sections.

J5 – LVDS CONNECTOR

If connecting the CED1 to a high-speed LVDS converter evaluation board, this connector should be used. The connector provides for four differential receive and four differential transmit data pairs in addition to separate differential receive and transmit clocks. Control of any high-speed device is normally achieved over an interface separate to the data. For this purpose, the SPI and some parallel control signals are also routed over this connector. With the inclusion of three power supplies, this connector provides the flexibility to interface to many LVDS converters. Details of the pin-out of this connector are given in Table 1.

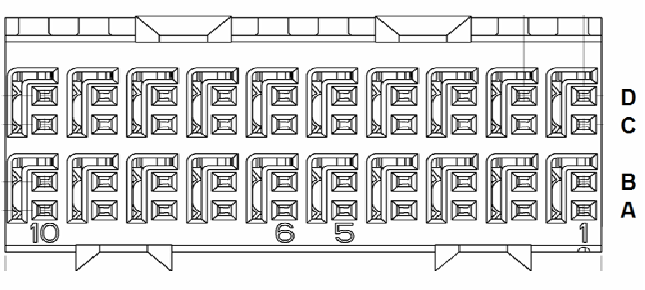


Figure 3. LVDS Connector pin locations

Table 1. LVDS Connector pin out

Pin Num	Pin Name	Description
1A, 1B	+VarA	Variable voltage analog power supply. See power supply section for more details.
1C, 1D	CLKOUT+/-	Differential Clock Output
2A	$\overline{\text{PAR\_CS0}}$	Parallel Chip Select 0
2B	$\overline{\text{PAR\_RD}}$	Parallel Read Strobe
C2-9, D2-7	Dx+/-	Differential Data Receive or Transmit Pair. By default the CED board is configured for 4 receive pairs (D0-3) and 4 transmit pairs (D4-7). These can be reconfigured by changing the termination resistors on the CED board. See schematics for more details.
A3-6	SPI_SELx	SPI Peripheral Chip Select
B3	$\overline{\text{PAR\_WR}}$	Parallel Write Strobe
B4	SPI_MISO	SPI Master In, Slave Out Data line
B5	SPI_MOSI	SPI Master Out, Slave In Data line
B6	SPI_CLK	SPI Clock
A7	TMR0/PPI_FS2	Timer 0 or Frame Sync 2 for PPI usage
B7	GPIO3/TMR1/PPI_FS1	General Purpose I/O, Timer 1 or Frame Sync 2 for PPI usage
A8	RXINT/GPIO2/PPI_FS3	Receive Interrupt, General Purpose I/O or Frame Sync 3 for PPI usage
B8	GPIO4/PAR_A0	General Purpose I/0 or parallel address LSb
A9, B9	+3.3VD_Edge	+3.3V Digital power supply
A10, B10	+VarD	Variable voltage digital power supply. See power supply section for more details.
C10, D10	CLKIN+/-	Differential Clock Input pair

J1 – MINI USB 'B' CONNECTOR

This is used to connect the CED1 to the PC for control and data transfer

J2 – 2-PIN SCREW TERMINAL POWER CONNECTOR

This connector is used when powering the CED board with a lab supply. Care must be taken to ensure the external supply is connected with the correct polarity.

J4 – DC POWER CONNECTOR

When using the CED1 with the supplied power supply, the DC plug should be connected here. The polarity for this connector is centre positive.

J6 – FPGA JTAG CONNECTOR

This can be used with Altera SignalTap Logic Analyzer and appropriate hardware to assist with FPGA development and debug.

J8, 9, 10 – 3× 90-WAY BLACKFIN EZ-KIT CONNECTORS

These three connectors bring across most of the peripheral signals from the Blackfin Ez-Kit directly into the FPGA where they can be used directly or rerouted to the other connectors. Additional processor or microcontroller boards could be designed and connected here if the user wished to add a processor to the design. See the Blackfin Ez-Kit manual for details of these connectors.

J3 – 96-WAY DIN41612 CONNECTOR

This connector has traditionally appeared on most precision ADC evaluation boards. It contains SPI, SPORT and Parallel signals as well as programmable digital and 5 separate analog power supplies. Pin out for this connector is shown in Table 2.

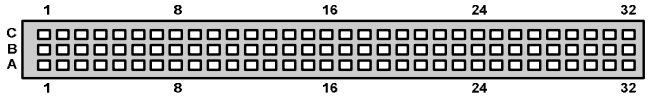


Figure 4. 96-way connector pin locations

Table 2. 96-way connector pin-out

Pin Num	Pin Name	Description
A1	SPORT_DT1PRI/ SPI_MOSI/PAR_D16	Sport1 Data Transmit Primary. SPI Master Out, Slave In data line. Parallel Data bit 16.
B1	GPIO3/TMR1/ PPI_FS1	General Purpose I/O bit 3. Timer 1. Parallel Peripheral Interface Frame Sync 1.
C1	SPORT_DR1PRI/ SPI_MISO/PAR_D19	Sport 1 Data Receive Primary. SPI Master In, Slave Out data line. Parallel Data bit 19.
A2	SPORT_TFS1/ SPI_SEL0/PAR_D17	Sport 1 Transmit Frame Sync. SPI Peripheral Chip Select 0. Parallel Data bit 17.
B2	PAR_D0	Parallel Data bit 0 (LSb)
C2	SPORT_RFS1/ SPI_SEL1/PAR_D20	Sport 1 Receive Frame Sync. SPI Peripheral Chip Select 1. Parallel Data bit 20.
A3	SPORT_TSCLK1/ SPI_CLK/PAR_D18	Sport 1 Transmit Serial Clock. SPI Clock. Parallel Data bit 18.
B3	PAR_D1	Parallel Data bit 1.
C3	SPORT_RSCLK1/ SPI_CLK/PAR_D21	Sport 1 Receive Clock. SPI Clock. Parallel Data bit 21.
A4, B4, C4	DGND	Digital Ground
A5	SPORT_DT0PRI/ SPI_SEL7	Sport 0 Data Transmit Primary. SPI Peripheral Chip Select 7
B5	PAR_D2	Parallel Data bit 2

C5	SPORT_DR0PRI/ SPI_SEL4	Sport 0 Data Receive Primary. SPI Peripheral Chip Select 4
A6	SPORT_TFS0/ SPI_SEL6	Sport 0 Transmit Frame Sync. SPI Peripheral Chip Select 6
B6	PAR_D3	Parallel Data bit 3
C6	SPORT_RFS0/ SPI_SEL3	Sport 0 Receive Frame Sync. SPI Peripheral Chip Select 3
A7	SPORT_TSCLK0/ SPI_SEL5	Sport 0 Transmit Serial Clock. SPI Peripheral Chip Select 5
B7	PAR_D4	Parallel Data bit 4
C7	SPORT_RSCLK0/ SPI_SEL2	SPORT 0 Receive Serial Clock. SPI Peripheral Chip Select 2
A8, B8, C8	+VarD (DV_{DD})	Variable Digital Power Supply. See Power Supply section for further details.
A9	PAR_RD	Parallel Read Strobe
B9	PAR_D5	Parallel Data bit 5
C9	PAR_WR	Parallel Write Strobe
A10	PAR_D22/PAR_A7	Parallel Data bit 22. Parallel Address bit 7 (MSb)
B10	PAR_D6	Parallel Data bit 5
C10	PAR_CS0	Parallel Chip Select 0
A11	SPORT_DT0SEC/ PAR_CS1/PAR_A5	Sport 0 Data Transmit Secondary. Parallel Chip Select 1. Parallel Address bit 5
B11	PAR_D7	Parallel Data bit 7
C11	GPIO6/PAR_D23/ PAR_A6	General Purpose I/O bit 6. Parallel Data bit 23. Parallel Address bit 6
A12, B12, C12	DGND	Digital Ground
A13	TWI_SDA/PAR_CS3/ PAR_A3	Two Wire Interface Serial Data. Parallel Chip Select 3. Parallel Address bit 3
B13	PAR_D8	Parallel Data bit 8
C13	SPORT_DR0SEC/ PAR_CS2/PAR_A4	Sport 0 Data Receive Secondary. Parallel Chip Select 2. Parallel Address bit 4
A14	GPIO5/PAR_A1	General Purpose I/O bit 5. Parallel Address bit 1
B14	PAR_D9	Parallel Data bit 9
C14	TWI_SCL/GPIO7/ PAR_A2	Two Wire Interface Serial Clock. General Purpose I/O bit 7 (MSb). Parallel Address bit 2
A15	GPIO0	General Purpose I/O bit 0 (LSb)
B15	PAR_D10	Parallel Data bit 10
C15	GPIO4/PAR_A0	General Purpose I/O bit 4. Parallel Address bit 0 (LSb)
A16, B16, C16	DGND	Digital Ground

A17	TMR0/PPI_FS2	Timer 0. Parallel Peripheral Interface Frame Sync 2
B17	PAR_D11	Parallel Data bit 11
C17	RXINT/GPIO2/ PPI_FS3	Receive Data Interrupt. General Purpose I/O bit 2. Parallel Peripheral Interface Frame Sync 3
A18	PAR_D12	Parallel Data bit 12
B18	PAR_D13	Parallel Data bit 13
C18	PAR_D14	Parallel Data bit 14
A19	CLKOUT	Clock Output
B19	GPIO1	General Purpose I/O bit 1
C19	PAR_D15	Parallel Data bit 15
A20, B20, C20	DGND	Digital Ground
A21-26, B21-26, C21-26	AGND	Analog Ground
A27, C27	+VarA	Variable Analog Power Supply. See Power Supply section for further details.
B27	AGND	Analog Ground
A28	N/C	No Connect. Do not use this pin.
B28	AGND	Analog Ground
C28	N/C	No Connect. Do not use this pin.
A29, B29, C29	AGND	Analog Ground
A30	-12VA	-12V Analog Power Supply. See Power Supply section for further details.
B30	AGND	Analog Ground
C30	+12VA	+12V Analog Power Supply. See Power Supply section for further details.
A31, B31, C31	-5VA (AV_{SS})	-5V Analog Power Supply. See Power Supply section for further details.
A32, B32, C32	+5VA (AV_{DD})	+5V Analog Power Supply. See Power Supply section for further details.

J7 – ANALOG POWER CONNECTOR

If any analog power supplies are required on boards connected to the CED1 via any connector other than the J3 (96-way), they can be taken from this pin header. Pin-out details of this connector are given in Table 3. Further details of the power supplies are given in the following section.

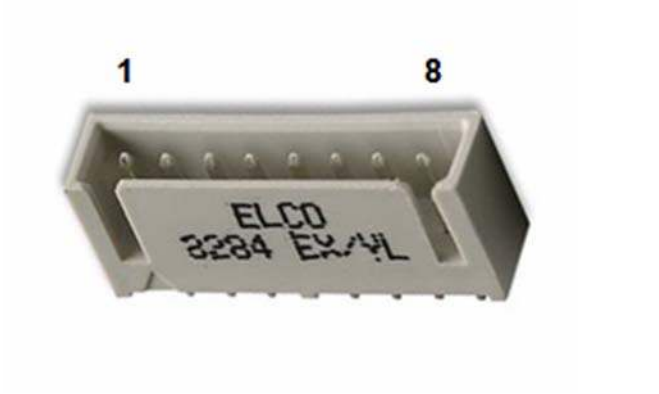


Figure 5. Analog Power Connector Pin Locations

Table 3. Analog Power Connector pin-out

Pin No	Function	Description
1	+12VA_Edge	+12V Analog Supply
2	-12VA_Edge	-12V Analog Supply
3, 6, 8	AGND	Analog Ground
4	+5VA_Edge	+5V Analog Supply
5	-5VA_Edge	-5V Analog Supply
7	+VarA	Variable Voltage Analog Supply. See Power Supply Section for more details.

J12 – SPORT INTERFACE

This standard two row, 0.1-inch connector can be used to connect any daughter board that utilizes the SPORT interface. This connector also contains all the SPI and Two Wire Interface (TWI) signals as well as 5V, 3.3V and the +7V CED board supply. See Table 4 for details. The pin-out of this connector is compatible with the Blackfin Stamp and Ez-Kit SPORT connector. More information on the pin names is given in the section detailing the 96-way connector.

Table 4. SPORT Connector Pin out

+5VD_Edge	**1**	**2**	+7V
DGND	**3**	**4**	N/C (Keying Pin)
$\overline{\text{RESET}}$	**5**	**6**	SPORT_TSCLK0/SPI_SEL5
SPORT_RFS0/SPI_SEL3	**7**	**8**	SPORT_DR0PRI/SPI_SEL4
DGND	**9**	**10**	SPORT_DR0SEC
SPORT_TFS0/SPI_SEL6	**11**	**12**	SPORT_DT0SEC
+3.3VD_Edge	**13**	**14**	SPORT_DT0PRI/SPI_SEL7
+3.3VD_Edge	**15**	**16**	SPORT_RSCLK0/SPI_SEL2
$\overline{\text{SPI\_SS}}$	**17**	**18**	SPI_MOSI
SPI_SEL1	**19**	**20**	SPI_MISO
SPI_SEL2	**21**	**22**	SPI_CLK
SPI_SEL3	**23**	**24**	TWI_SDA
SPI_SEL4	**25**	**26**	TWI_SCK
SPI_SEL5	**27**	**28**	RXINT/GPIO2/PPI_FS3
SPI_SEL6	**29**	**30**	GPIO3/TMR1/PPI_FS1
SPI_SEL7	**31**	**32**	TMR0/PPI_FS2
DGND	**33**	**34**	DGND

J13 – SPI INTERFACE

Using the SPI connector instead of the SPORT should only be considered when the user is satisfied that the device being connected is completely compatible with the SPI specification. This implies that only 8- or 16-bit active low framing is required. See Table 5 for pin-out details of this connector. This connector is compatible with the SPI connector on the Blackfin Stamp and Ez-Kits. More information on the pin names is given in the section detailing the 96-way connector.

Table 5. SPI Connector Pin out

+5VD_Edge	**1**	**2**	+3.3VD_Edge
+5VD_Edge	**3**	**4**	+3.3VD_Edge
SPI_MOSI	**5**	**6**	SPI_MISO
$\overline{\text{RESET}}$	**7**	**8**	SPI_CLK
SPI_SEL1	**9**	**10**	$\overline{\text{SPI\_SS}}$
SPI_SEL3	**11**	**12**	SPI_SEL2
SPI_SEL5	**13**	**14**	SPI_SEL4
SPI_SEL7	**15**	**16**	SPI_SEL6
N/C (Keying Pin)	**17**	**18**	DGND
+7V	**19**	**20**	DGND

J14 – PPI INTERFACE

This connector is intended to allow attachment of daughter boards designed to connect to the PPI Connector on the Blackfin Stamp and Ez-Kit. However, with the signals provided, it should be possible to connect to most parallel interface devices needing up to 16 data bits and multiple control signals.

The inclusion of the SPI signals on this connector allows for separate data and configuration interfaces if required. See Table 6 for details of this connector. More information on the pin names is given in the section detailing the 96-way connector.

Table 6. PPI Connector Pin out

+5VD_Edge	**1**	**2**	+7V
+5VD_Edge	**3**	**4**	N/C (Keying Pin)
+3.3VD_Edge	**5**	**6**	CLKOUTP_EXT
+3.3VD_Edge	**7**	**8**	PAR_D0
PAR_D1	**9**	**10**	PAR_D2
PAR_D3	**11**	**12**	PAR_D4
PAR_D5	**13**	**14**	PAR_D6
PAR_D7	**15**	**16**	PAR_D8
PAR_D9	**17**	**18**	PAR_D10
PAR_D11	**19**	**20**	PAR_D12
PAR_D13	**21**	**22**	PAR_D14
PAR_D15	**23**	**24**	SPI_SEL3
SPI_SEL2	**25**	**26**	SPI_SEL1
$\overline{\text{SPI\_SS}}$	**27**	**28**	$\overline{\text{RESET}}$
RxInt/GPIO2/PPI_FS3	**29**	**30**	SPI_MOSI
GPIO3/TMR1/PPI_FS1	**31**	**32**	SPI_MISO
TMR0/PPI_FS2	**33**	**34**	SPI_CLK
DGND	**35**	**36**	TWI_SDA
DGND	**37**	**38**	TWI_SCK
DGND	**39**	**40**	DGND

CONNECTOR PART NUMBERS

Table 7. Connector Part Numbers

Ref. Des.	Description	Manufacturer	Part Number	Mating Connector
J1	USB Mini-B connector	Molex	565790576	Standard Mini-B USB Cable
J2	2-pin screw terminal	Camden Electronics	CTB5000/2	Cables inserted directly
J3	96-Way 90° DIN41612 socket	Harting	0973 296 6801	0903 196 6921
J4	DC Barrel connector, 2mm centre	Kycon	KLDX-SMT2-0202-A	Cliff - DCPP1 (FC68147)
J5	LVDS connector	Tyco Electronics	1469028-1	1469169-1
J6	10-Pin, 2 row standard 0.1" pitch header	Harwin	M20-8760542	M20-7830546
J8-10	90-way Micro-strip Terminal	Samtec	TFC-145-X2-FD-A	SFC-145-T2-FD-A
J12	34-Pin, 2 row standard 0.1" pitch header	Harwin	M20-8761742	M20-7831746
J13	20-Pin, 2 row standard 0.1" pitch header	Harwin	M20-8761042	M20-7831046
J14	40-Pin, 2 row standard 0.1" pitch header	Harwin	M20-8762042	M20-7832046

POWER SUPPLIES

The CED board provides multiple power supplies that are made available for use with connected boards. A single 7V supply is required for the CED board and this is used to power the board itself and the supplies for boards connected to it. A resettable 2A fuse limits the current that can be drawn from the supply thus limiting the power consumption of the CED and any attached boards.

On it's own without any converter boards attached, the idle current of the CED is approximately 220 mA. When accessing SRAM for example, the current drawn by the CED board itself can increase significantly. Users designing boards to operate with the CED that wish to use the supplies provided must bear in mind the total available power when calculating their power requirements.

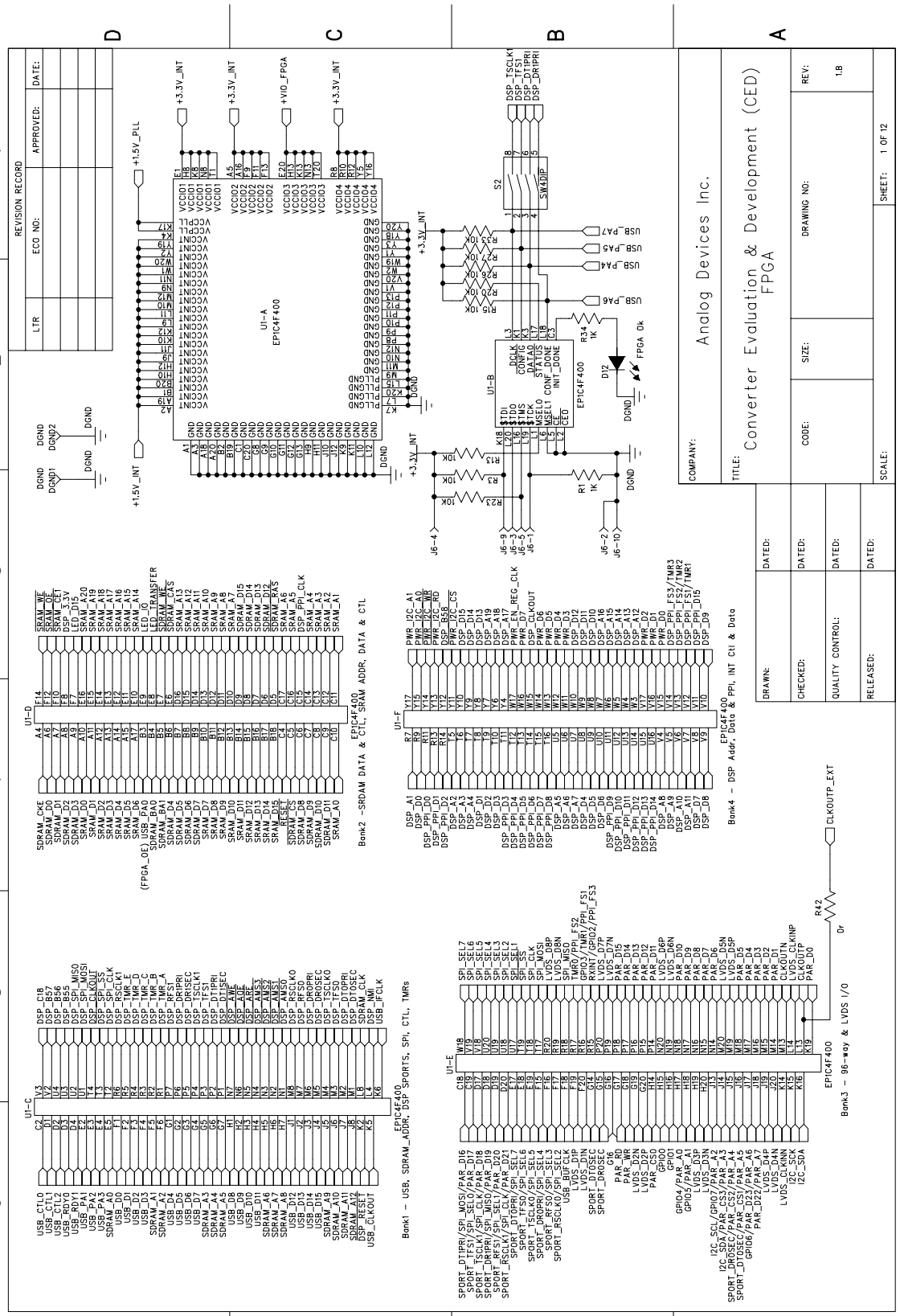
While the supplies generated on the CED are kept as clean as possible, designers of boards connected to the CED must ensure that all devices and supplies are adequately decoupled. This will prevent noise being fed back onto the power supplies of the CED. Excessive noise introduced on to the power supplies may cause the CED or attached boards to malfunction.

The voltage and current ratings of the supplies listed in Table 8 are defined to be absolute maximum limits. While fuses and thermal overload protection have been provided in the power supply circuitry, attempting to draw more current from a particular supply or exceeding the total power available from a combination of supplies may cause damage to the CED board.

Table 8. Power Supplies

Name	Voltage	Max. Current	Test Conditions / Comments
+VarA	+1.5V to +5.5V	300mA	Regulation may suffer at lower voltages.
-12VA	-12V ±5%	100mA	Fuse limited at 100mA.
+12VA	+12V ±5%	100mA	Fuse limited at 100mA.
-5VA	-5V ±5%	100mA	Fuse limited at 100mA.
+5VA	+5V ±5%	500mA	Regulator rated for 500mA but thermally limited.
+5VD	+5V ±5%	500mA	Regulator rated for 500mA but thermally limited.
+3.3VD	+3.3V ±5%	300mA	Thermally limited.
+VarD	+1.5V to +5.5V	300mA	Regulation may suffer at lower voltages.
+7V	+7V ±5%	2A	Total current that can be drawn through board including all other supplies. Fuse limited.

SCHEMATICS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Bank2 -SRDAM DATA & CTL, SRAM ADDR, DATA & CTL
Bank3 - 96-way & LVDS I/O
Bank4 - DSP Addr, Data & PPI, INT Ctl & Data
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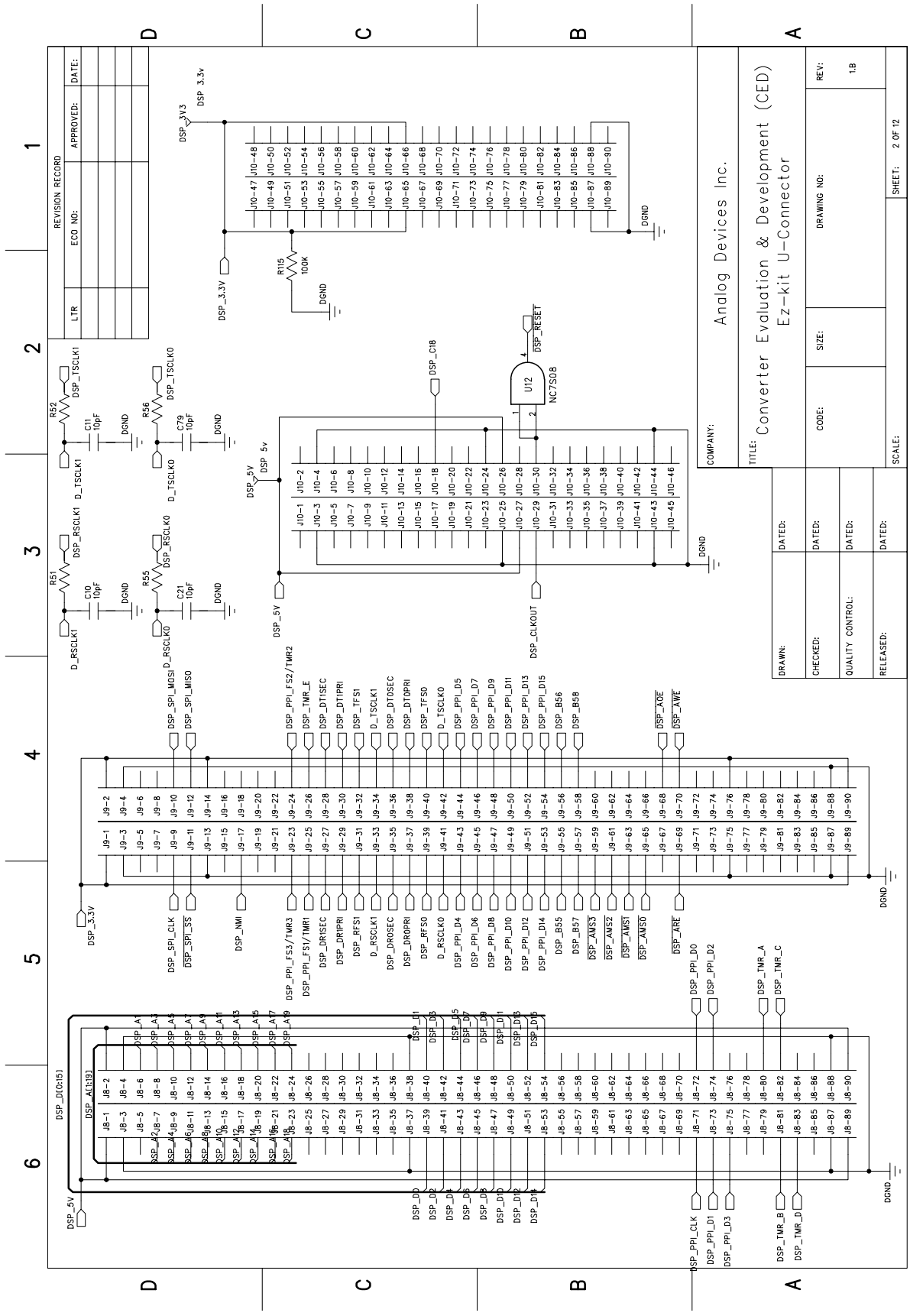
+1.5V_PLL
+VIO_FPGA
DGND
FPGA Ok
CLKOUTP_EXT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DSP_3.3V
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DSP_RSCLK0
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D_TSCLK0
D_RSCLK1
D_RSCLK0
DSP_CLKOUT
DSP_RESET
DSP_CIB
U12
NC7S08
R115 100K
R52
R56
R61
R55
C11 10pF
C79 10pF
C10 10pF
C21 10pF
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DSP_SPI_MISO
DSP_SPI_CLK
DSP_SPI_SS
DSP_NMI
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DSP_TMR_E
DSP_DTISEC
DSP_DTIPRI
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D_TSCLK1
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DSP_DTOPRI
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DSP_PPI_D13
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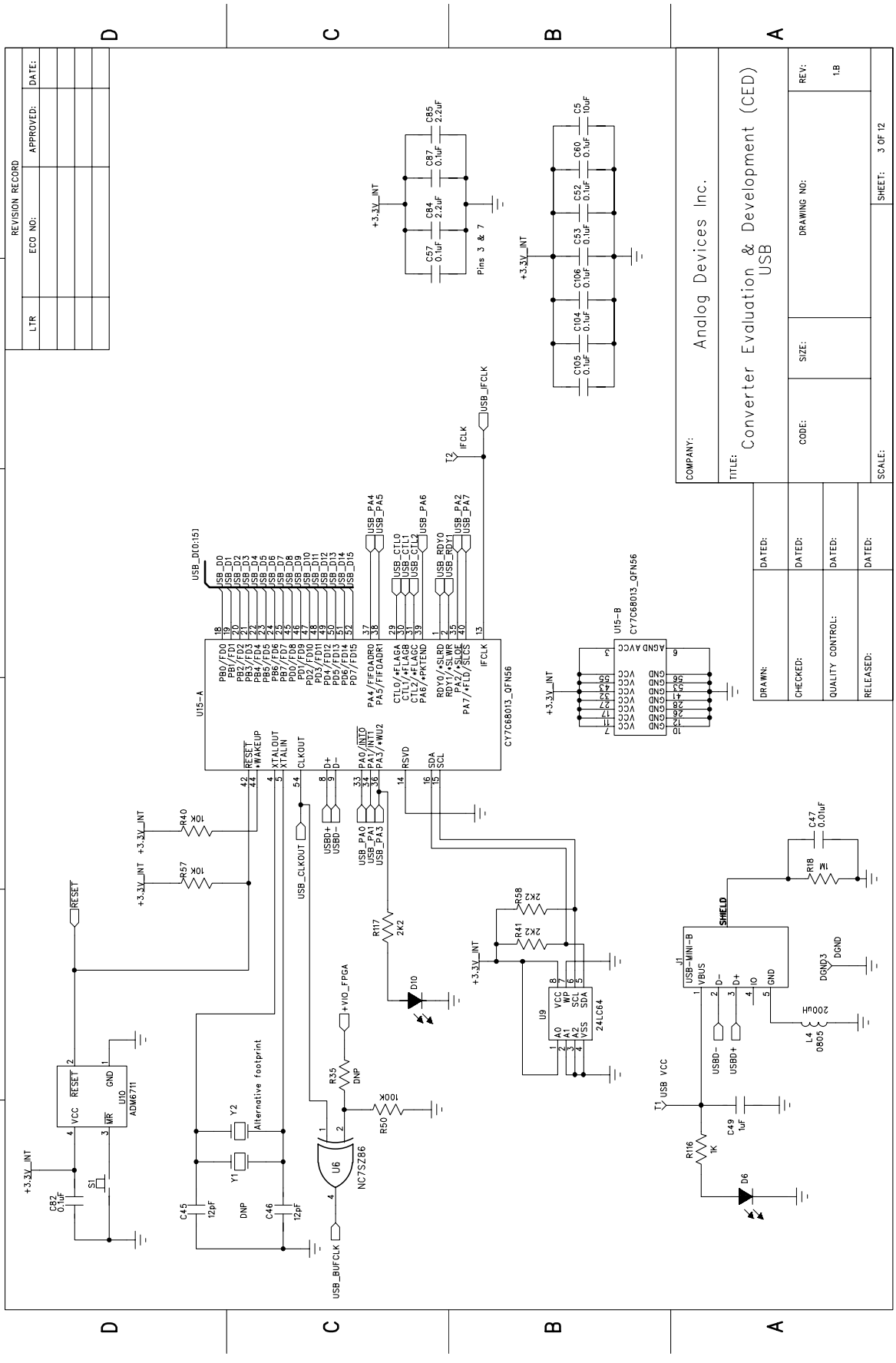
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U6 NC7SZ86
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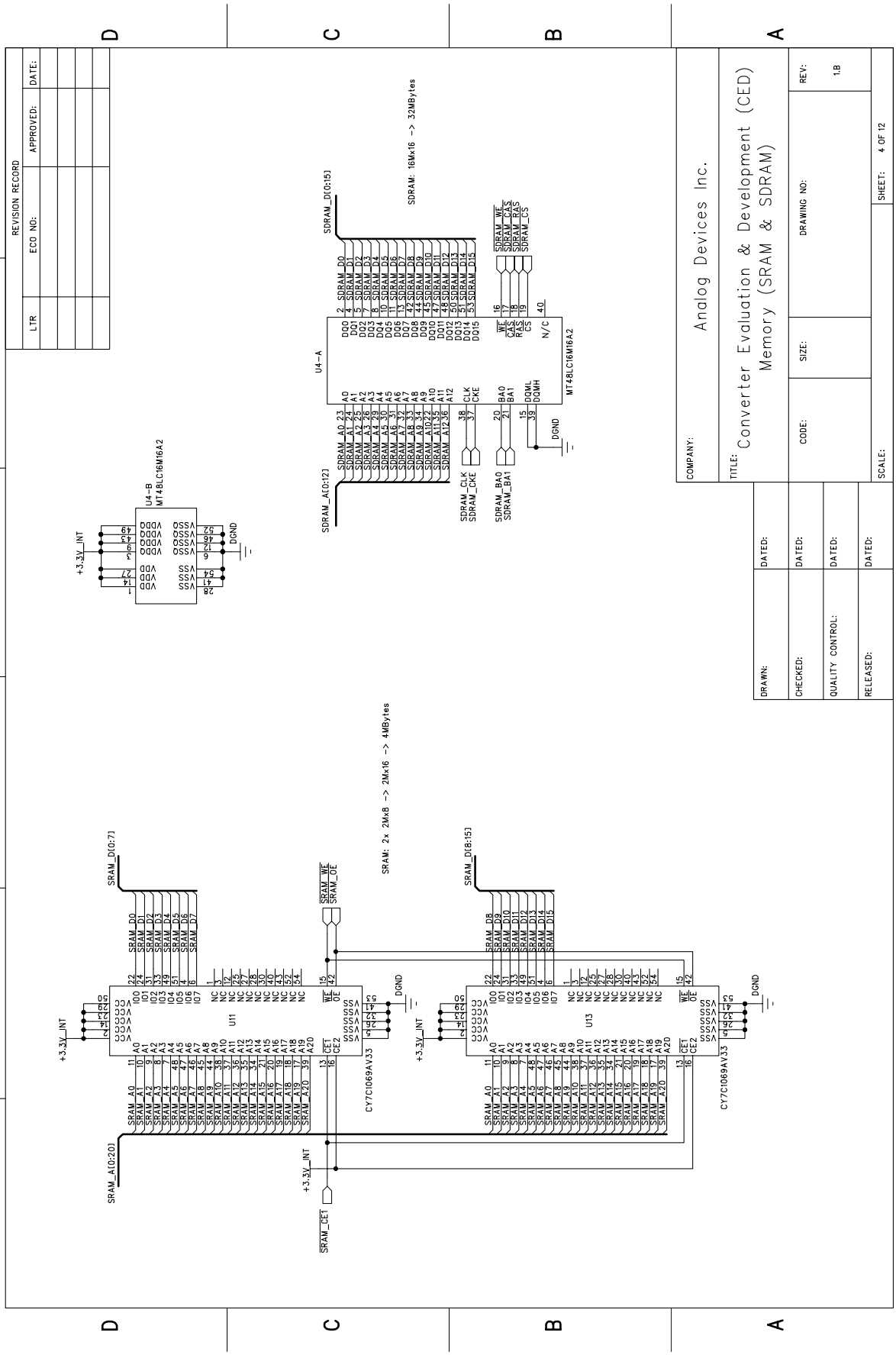
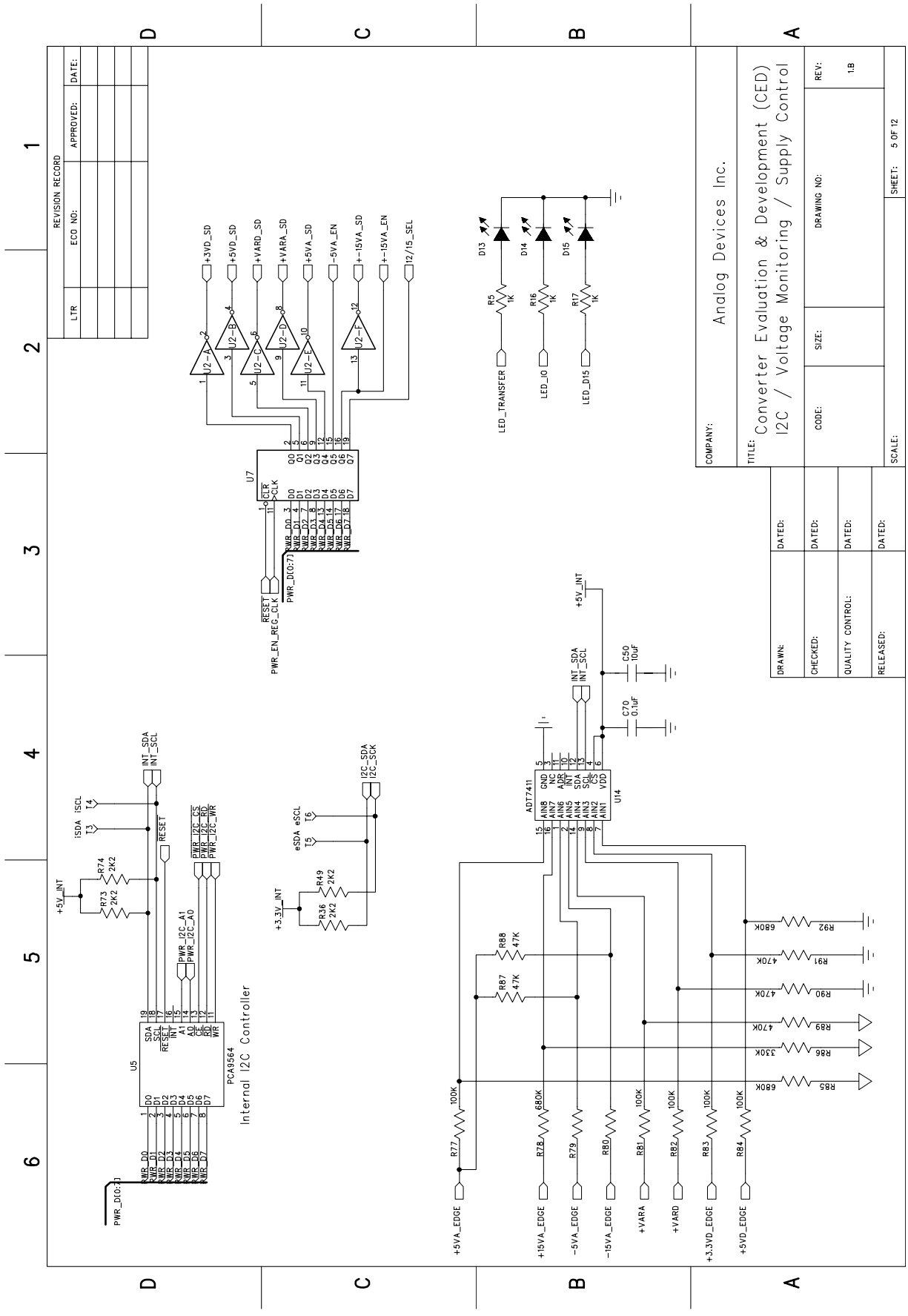
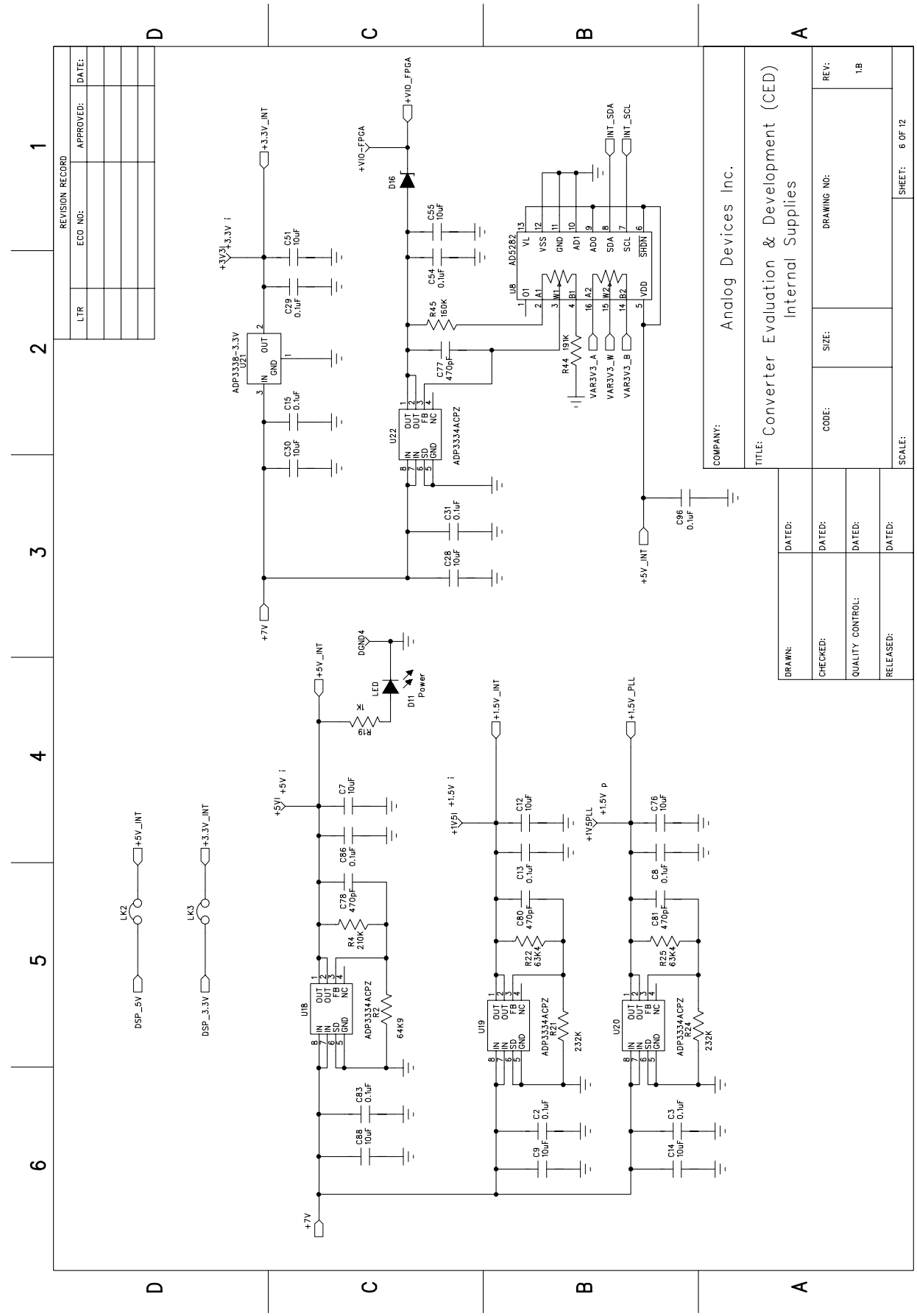
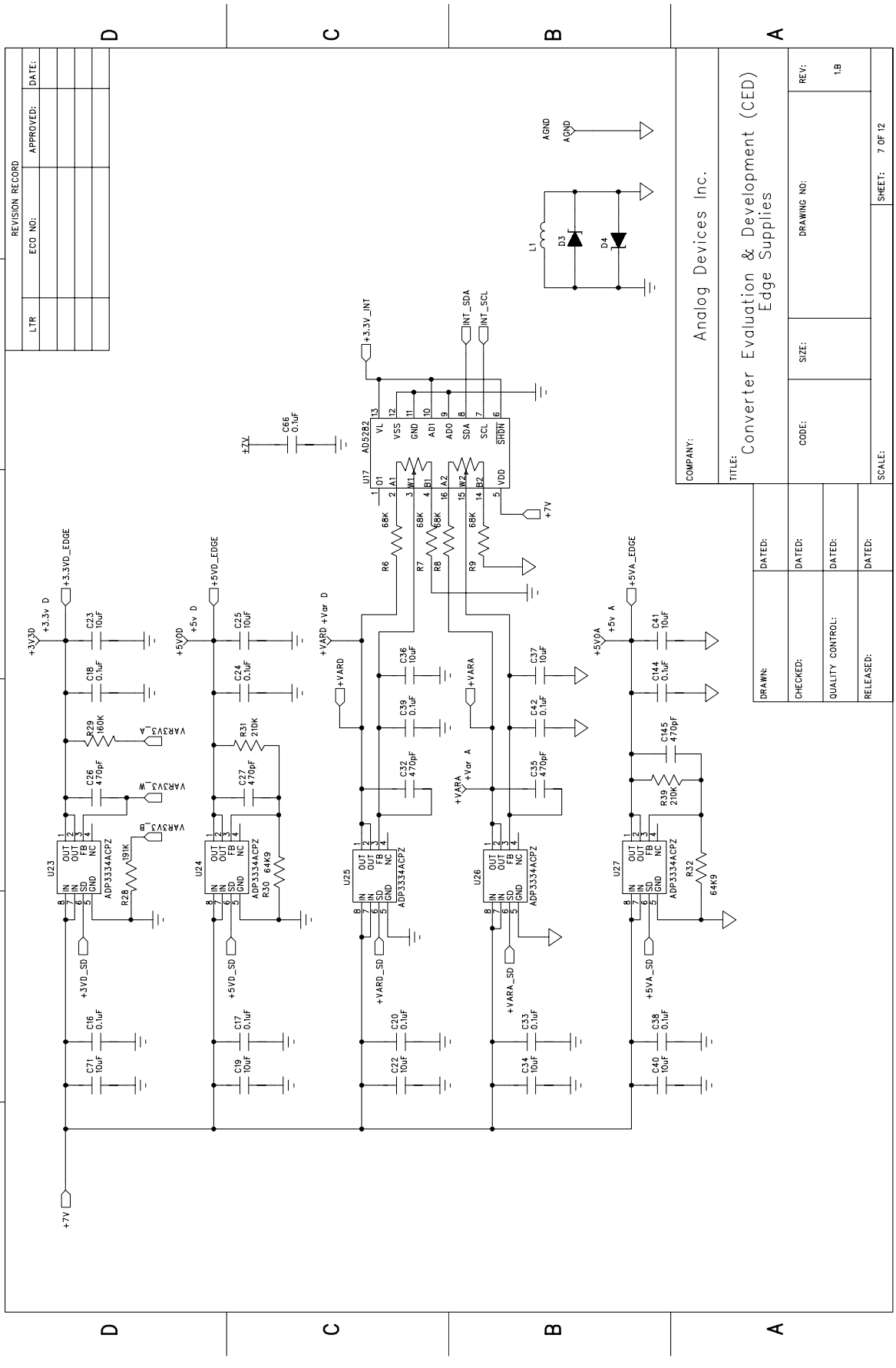
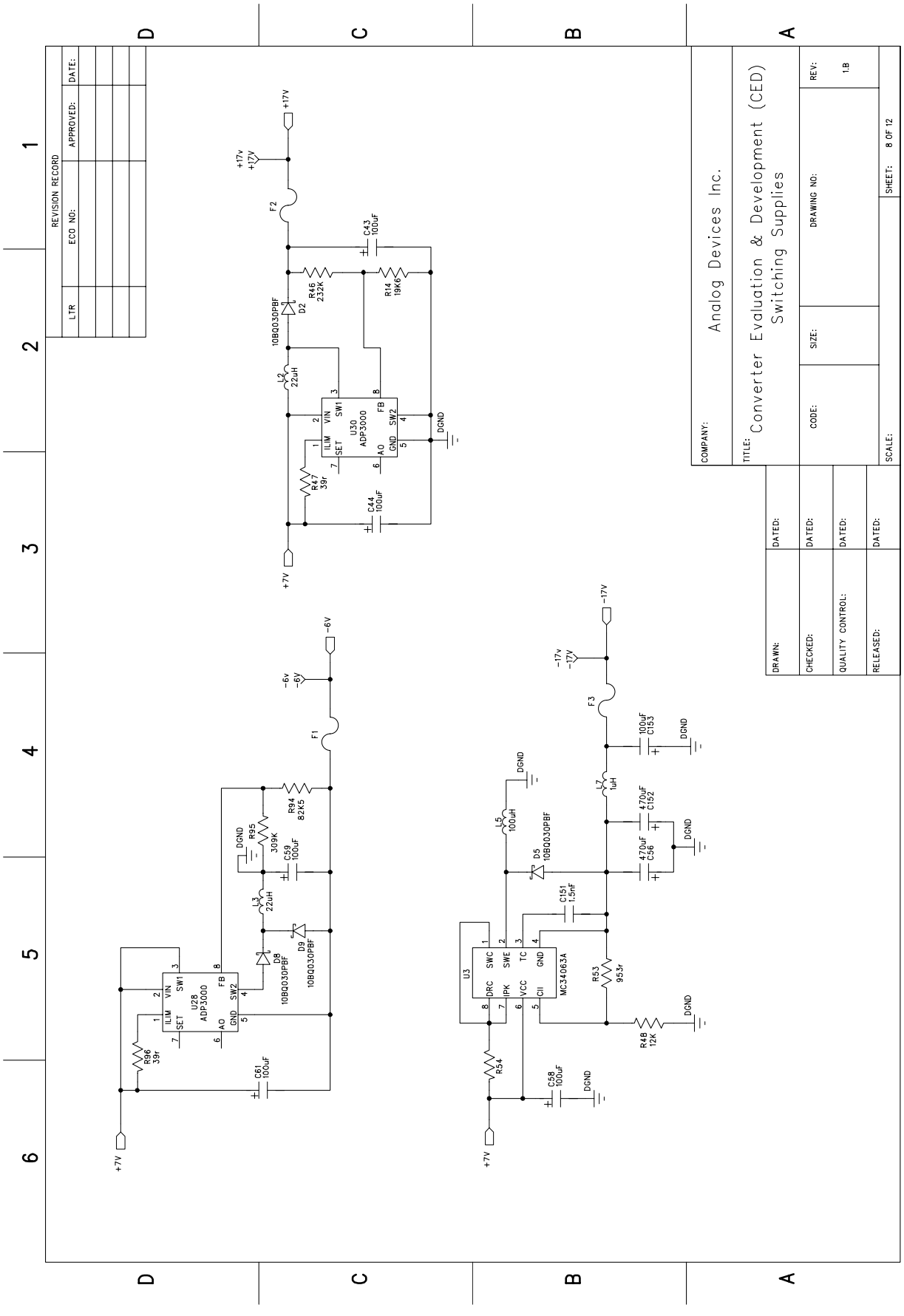
USB_BUFCLK
USB_IFCLK
+3.3V_INT
+VIO_FPGA
RESET
Alternative footprint
Pins 3 & 7
SHIELD
DGND
DGND3

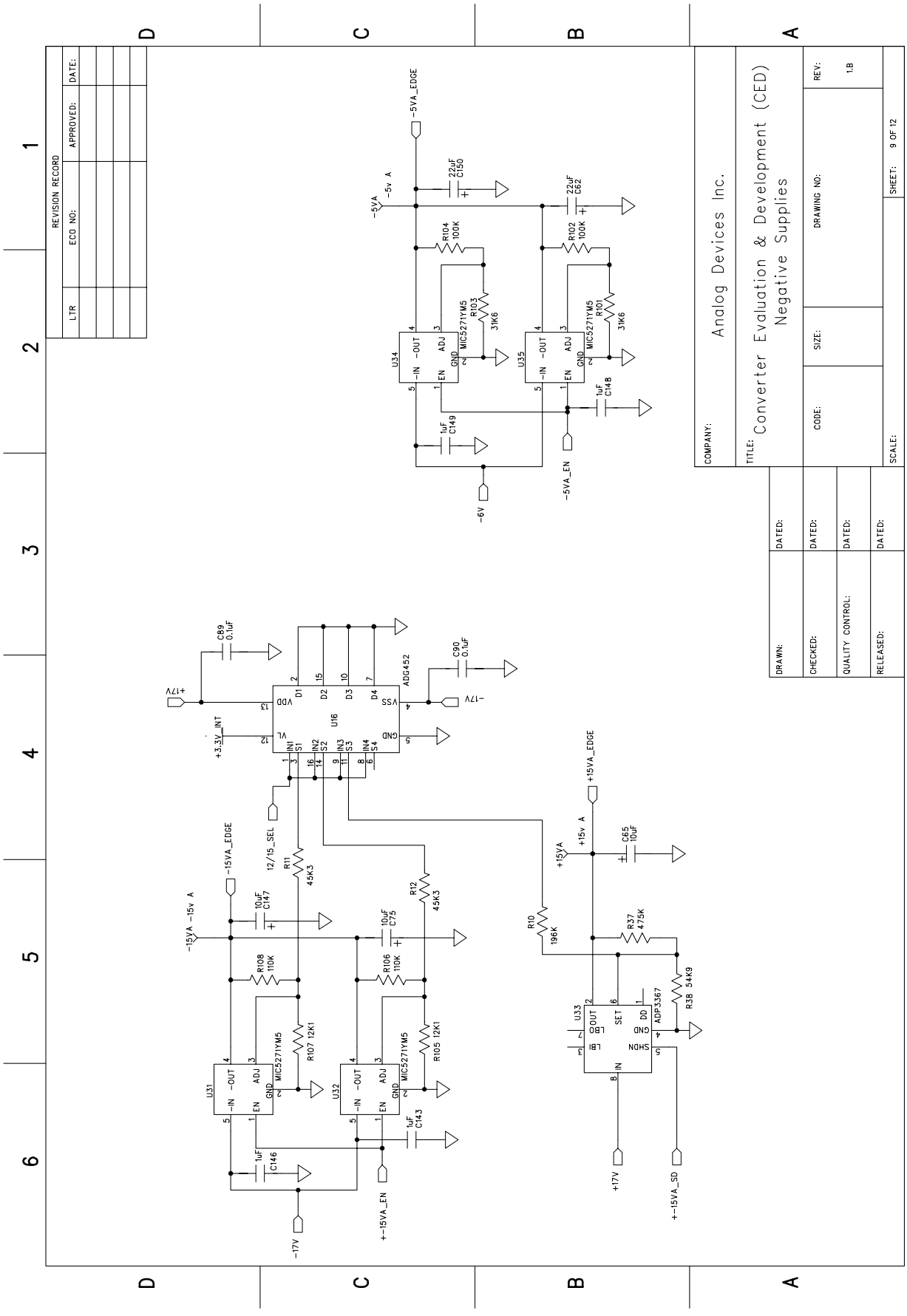

REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
SDRAM: 16Mx16 -> 32MBytes
SRAM: 2x 2Mx8 -> 2Mx16 -> 4MBytes
COMPANY: Analog Devices Inc.
TITLE: Converter Evaluation & Development (CED) Memory (SRAM & SDRAM)
DRAWN:
CHECKED:
QUALITY CONTROL:
RELEASED:
DATED:
CODE:
SIZE:
DRAWING NO:
REV: 1.B
SCALE:
SHEET: 4 OF 12

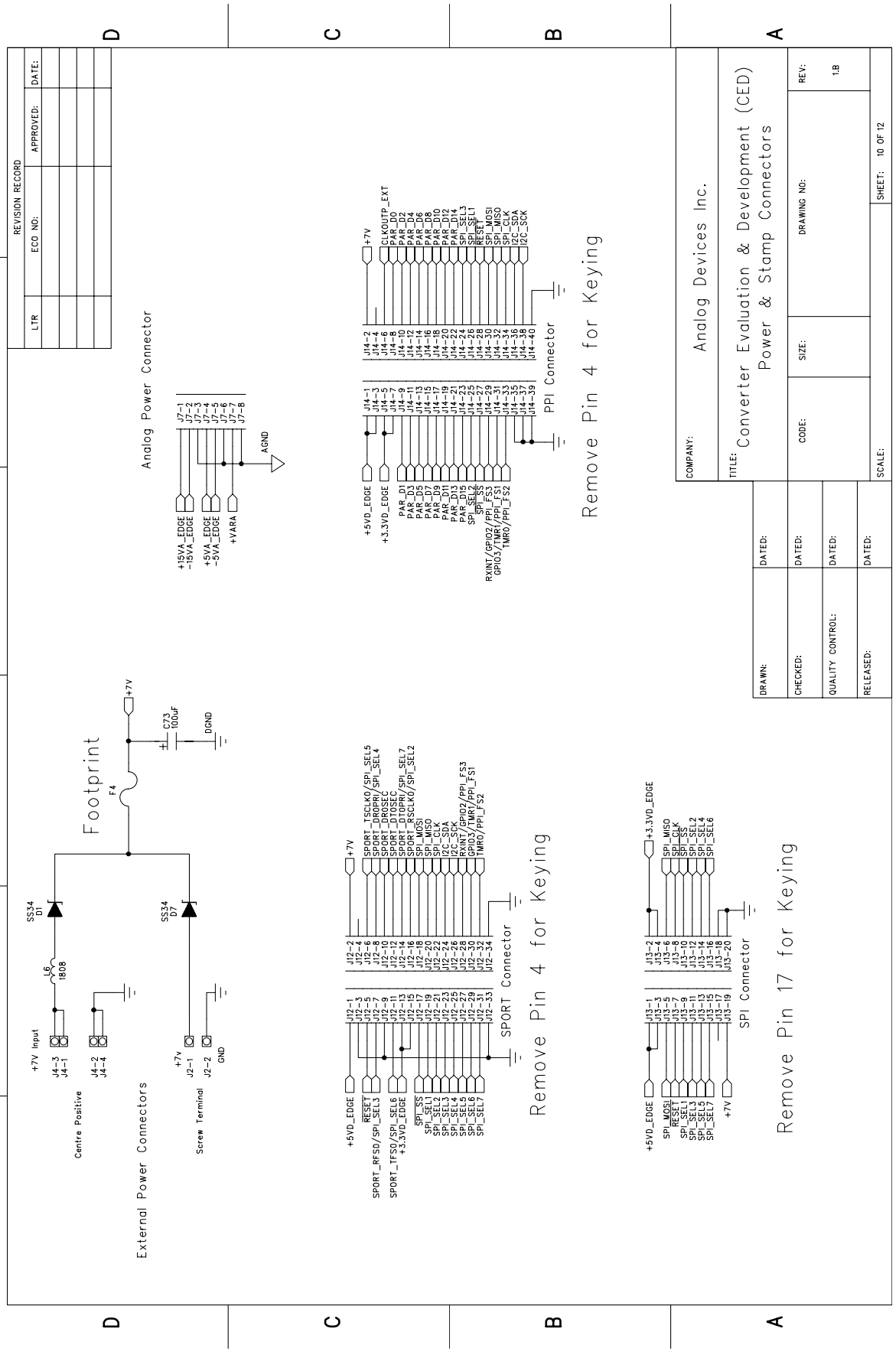

REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
COMPANY: Analog Devices Inc.
TITLE: Converter Evaluation & Development (CED)
I2C / Voltage Monitoring / Supply Control
DRAWN:
CHECKED:
QUALITY CONTROL:
RELEASED:
DATED:
CODE:
SIZE:
DRAWING NO:
REV: 1.B
SCALE:
SHEET: 5 OF 12
PCA9564
Internal I2C Controller
ADT7411
+5V_INT
+3.3V_INT
INT_SDA
INT_SCL
I2C_SDA
I2C_SCK
RESET
PWR_EN_REG_CLK
PWR_DIO:7:1
LED_TRANSFER
LED_IO
LED_D15
+3VD_SD
+5VD_SD
+VARD_SD
+VARA_SD
+5VA_SD
-5VA_EN
+-15VA_SD
+-15VA_EN
12/15_SEL
+5VA_EDGE
+15VA_EDGE
-5VA_EDGE
-15VA_EDGE
+VARA
+VARD
+3.3VD_EDGE
+5VD_EDGE

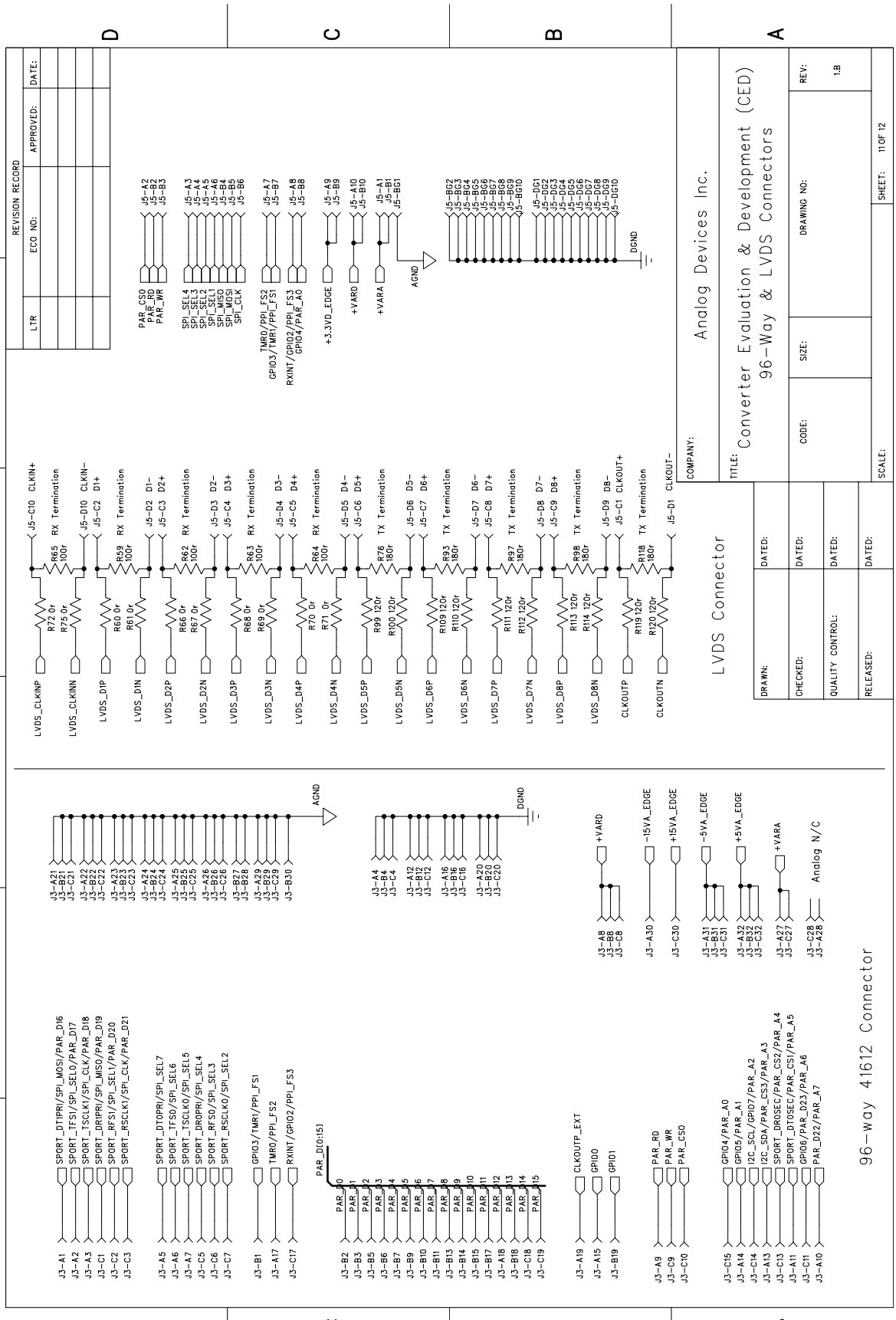

REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
Analog Devices Inc.
COMPANY:
Converter Evaluation & Development (CED)
Internal Supplies
TITLE:
CODE:
SIZE:
DRAWING NO:
REV:
1.B
SCALE:
SHEET: 6 OF 12
DRAWN:
CHECKED:
QUALITY CONTROL:
RELEASED:
DATED:
+VIO_FPGA
+3.3V_INT
+5V_INT
+7V
+1.5V_INT
+1.5V_PLL
+5V_INT
DGND4
LED
Power
D11
D16
U8 AD5282
U21 ADP3338-3.3V
U22 ADP3334ACPZ
U18 ADP3334ACPZ R2 64K9
U19 ADP3334ACPZ R21 232K
U20 ADP3334ACPZ R24 232K
R4 210K
R45 160K
R44 191K
R25 6.3K4
R22 6.3K4
C7 10uF
C86 0.1uF
C78 470pF
C83 0.1uF
C88 10uF
C51 10uF
C29 0.1uF
C15 0.1uF
C30 10uF
C55 10uF
C54 0.1uF
C77 470pF
C31 0.1uF
C28 10uF
C96 0.1uF
C12 10uF
C13 0.1uF
C80 470pF
C2 0.1uF
C9 10uF
C76 10uF
C8 0.1uF
C81 470pF
C3 0.1uF
C14 10uF
INT_SDA
INT_SCL
VAR3V3_A
VAR3V3_W
VAR3V3_B
DSP_5V
DSP_3.3V
LK2
LK3

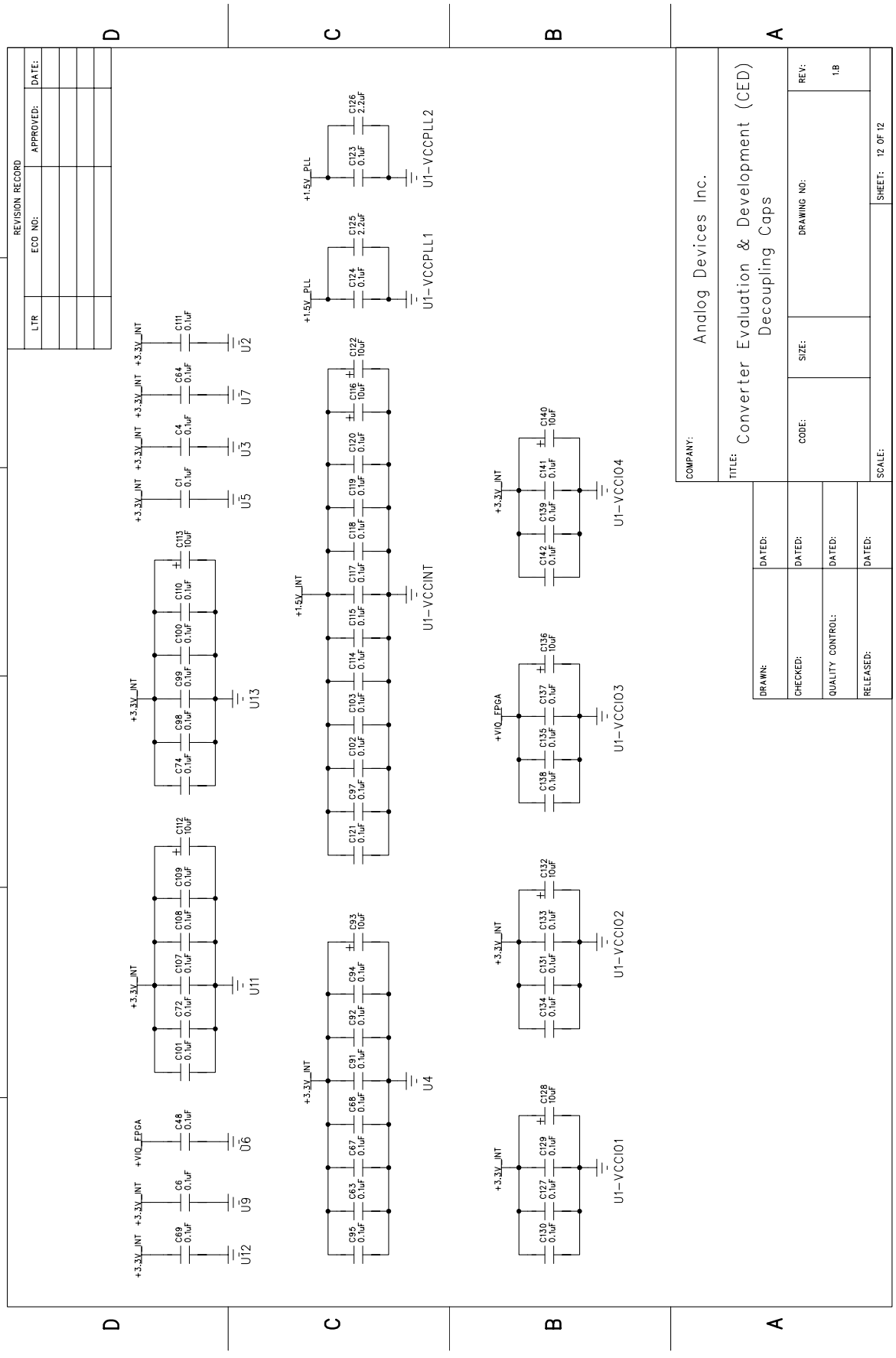

REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
COMPANY: Analog Devices Inc.
TITLE: Converter Evaluation & Development (CED) Edge Supplies
DRAWN:
CHECKED:
QUALITY CONTROL:
RELEASED:
DATED:
CODE:
SIZE:
DRAWING NO:
REV: 1.B
SCALE:
SHEET: 7 OF 12
+3.3V_INT
INT_SDA
INT_SCL
AGND
+7V
U17 AD5282
+3.3VD_EDGE
+5VD_EDGE
+VARD +Var D
+5VA_EDGE
+VARA +Var A
U23 ADP3334ACPZ
U24 ADP3334ACPZ
U25 ADP3334ACPZ
U26 ADP3334ACPZ
U27 ADP3334ACPZ
+3VD_SD
+5VD_SD
+VARD_SD
+VARA_SD
+5VA_SD


REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
COMPANY: Analog Devices Inc.
TITLE: Converter Evaluation & Development (CED) Switching Supplies
CODE:
SIZE:
DRAWING NO:
REV: 1.B
SCALE:
SHEET: 8 OF 12
DRAWN: DATED:
CHECKED: DATED:
QUALITY CONTROL: DATED:
RELEASED: DATED:
+17V
F2
D2 10BQ030PBF
L2 22uH
R46 232K
R14 19K6
C43 100uF
U3D ADP3000
R47 39r
C44 100uF
DGND
+7V
-6V
F1
D8 10BQ030PBF
D9 10BQ030PBF
L3 22uH
R94 82K5
R95 309K
C59 100uF
U2B ADP3000
R96 39r
C61 100uF
-17V
F3
L5 100uH
D5 10BQ030PBF
L7 1uH
C153 100uF
C152 470uF
C56 470uF
C151 1.5nF
U3 MC34063A
R53 953r
R48 12K
R54
C58 100uF


REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
COMPANY: Analog Devices Inc.
TITLE: Converter Evaluation & Development (CED)
Negative Supplies
CODE:
SIZE:
DRAWING NO:
REV: 1.B
SCALE:
SHEET: 9 OF 12
DRAWN: DATED:
CHECKED: DATED:
QUALITY CONTROL: DATED:
RELEASED: DATED:
-5VA_EDGE
-5v A
-5VA
22uF C150
22uF C62
R104 100K
R102 100K
R103 31K6
R101 31K6
MIC5271YM5
U34
U35
1uF C149
1uF C148
-6V
-5VA_EN
C89 0.1uF
C90 0.1uF
+17V
-17V
+3.3V_INT
ADG452
U16
12/15_SEL
+15VA_EDGE
+15v A
+15VA
C65 10uF
-15VA_EDGE
-15v A
-15VA
10uF C147
10uF C75
R11 45K3
R12 45K3
R10 196K
R37 475K
R38 54K9
R108 110K
R106 110K
R107 12K1
R105 12K1
U31
U32
U33
ADP3367
1uF C146
1uF C143
+-15VA_EN
+-15VA_SD


REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
Analog Power Connector
J7-1
J7-2
J7-3
J7-4
J7-5
J7-6
J7-7
J7-8
AGND
+15VA_EDGE
-15VA_EDGE
+5VA_EDGE
-5VA_EDGE
+VARA
+5VD_EDGE
+3.3VD_EDGE
PAR_D1
PAR_D3
PAR_D5
PAR_D7
PAR_D9
PAR_D11
PAR_D13
PAR_D15
SPI_SEL2
SPI_SS
RXINT/GPIO2/PPI_FS3
GPIO3/TMR1/PPI_FS1
TMR0/PPI_FS2
+7V
CLKOUTP_EXT
PAR_D0
PAR_D2
PAR_D4
PAR_D6
PAR_D8
PAR_D10
PAR_D12
PAR_D14
SPI_SEL3
SPI_SEL1
RESET
SPI_MOSI
SPI_MISO
SPI_CLK
I2C_SDA
I2C_SCK
PPI Connector
Remove Pin 4 for Keying
Footprint
F4
+7V
C73
100uF
DGND
SS34
D1
L6
1808
+7V Input
J4-3
J4-1
Centre Positive
J4-2
J4-4
External Power Connectors
SS34
D7
+7V
J2-1
J2-2
GND
Screw Terminal
SPORT_TSCLK0/SPI_SEL5
SPORT_DROPRI/SPI_SEL4
SPORT_DROSEC
SPORT_DTOSEC
SPORT_DTOPRI/SPI_SEL7
SPORT_RSCLK0/SPI_SEL2
SPI_MOSI
SPI_MISO
SPI_CLK
I2C_SDA
I2C_SCK
RXINT/GPIO2/PPI_FS3
GPIO3/TMR1/PPI_FS1
TMR0/PPI_FS2
SPORT_RFSO/SPI_SEL3
SPORT_TFSO/SPI_SEL6
+3.3VD_EDGE
SPI_SS
SPI_SEL1
SPI_SEL2
SPI_SEL3
SPI_SEL4
SPI_SEL5
SPI_SEL6
SPI_SEL7
SPORT Connector
Remove Pin 4 for Keying
SPI_MISO
SPI_CLK
SPI_SS
SPI_SEL2
SPI_SEL4
SPI_SEL6
SPI Connector
Remove Pin 17 for Keying
COMPANY:
Analog Devices Inc.
TITLE:
Converter Evaluation & Development (CED)
Power & Stamp Connectors
DRAWN:
DATED:
CHECKED:
DATED:
QUALITY CONTROL:
DATED:
RELEASED:
DATED:
CODE:
SIZE:
DRAWING NO:
REV:
1.B
SCALE:
SHEET: 10 OF 12


REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
LVDS Connector
96-way 41612 Connector
COMPANY: Analog Devices Inc.
TITLE: Converter Evaluation & Development (CED)
96-Way & LVDS Connectors
DRAWN:
CHECKED:
QUALITY CONTROL:
RELEASED:
DATED:
CODE:
SIZE:
DRAWING NO:
REV: 1.B
SCALE:
SHEET: 11OF 12
LVDS_CLKINP
LVDS_CLKINN
LVDS_D1P
LVDS_D1N
LVDS_D2P
LVDS_D2N
LVDS_D3P
LVDS_D3N
LVDS_D4P
LVDS_D4N
LVDS_D5P
LVDS_D5N
LVDS_D6P
LVDS_D6N
LVDS_D7P
LVDS_D7N
LVDS_D8P
LVDS_D8N
CLKOUTP
CLKOUTN
RX Termination
TX Termination
PAR_CSO
PAR_RD
PAR_WR
SPI_SEL4
SPI_SEL3
SPI_SEL2
SPI_SEL1
SPI_MISO
SPI_MOSI
SPI_CLK
TMR0/PPI_FS2
GPIO3/TMR1/PPI_FS1
RXINT/GPIO2/PPI_FS3
GPIO4/PAR_A0
+3.3VD_EDGE
+VARD
+VARA
AGND
DGND
PAR_DI0:15
CLKOUTP_EXT
GPIO0
GPIO1
-15VA_EDGE
+15VA_EDGE
-5VA_EDGE
+5VA_EDGE
Analog N/C


REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
COMPANY: Analog Devices Inc.
TITLE: Converter Evaluation & Development (CED) Decoupling Caps
DRAWN:
CHECKED:
QUALITY CONTROL:
RELEASED:
DATED:
CODE:
SIZE:
DRAWING NO:
REV: 1.B
SCALE:
SHEET: 12 OF 12
U1-VCCINT
U1-VCCPLL1
U1-VCCPLL2
U1-VCCIO1
U1-VCCIO2
U1-VCCIO3
U1-VCCIO4
+3.3V_INT
+1.5V_INT
+1.5V_PLL
+VIO_FPGA

Ordering Information

ORDERING GUIDE

Model	Description
EVAL-CED1Z[1]	Converter Evaluation and Development Board

[1] Z = RoHS Compliant Part.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PR07072-0-9/07(PrA)