# 1.5V Drive Pch MOSFET

# **RZQ045P01**

#### Structure

Silicon P-channel MOSFET

#### Features

- 1) Low on-resistance.
- 2) High power package.
- 3) Low voltage drive. (1.5V)

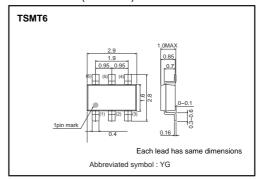
#### Applications

Switching

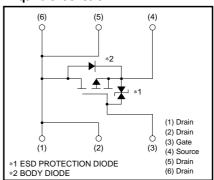
# Packaging specifications

	Package	Taping
Туре	Code	TR
	Basic ordering unit (pieces)	3000
RZQ045P0	0	

# ●Dimensions (Unit:mm)



# ●Equivalent circuit



# ● Absolute maximum ratings (Ta=25°C)

Parameter	Symbol		Limits	Unit	
Drain-source voltage		V <sub>DSS</sub>		-12	V
Gate-source voltage	V <sub>GSS</sub>		±10	V	
Drain augrent	Continuous	I <sub>D</sub>		±4.5	Α
Drain current	Pulsed	IDP	*1	±12	Α
Source current	Continuous	Is		-1	А
(Body diode)	Pulsed	I <sub>SP</sub>	*1	-12	Α
Total power dissipation	PD	*2	1.25	W	
Channel temperature	Tch		150	°C	
Range of Storage temperature		Tstg		-55 to +150	°C

<sup>\*1</sup> Pw≤10µs, Duty cycle≤1% \*2 Mounted on a ceramic board

#### Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to ambient	Rth(ch-a) *	100	°C / W

<sup>\*</sup> Mounted on a ceramic board.

# ●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Gate-source leakage	I <sub>GSS</sub>	-	_	±10	μА	V <sub>GS</sub> =±10V, V <sub>DS</sub> =0V
Drain-source breakdown voltage	V <sub>(BR)</sub> DSS	-12	_	_	V	I <sub>D</sub> = -1mA, V <sub>GS</sub> =0V
Zero gate voltage drain current	I <sub>DSS</sub>	_	_	-1	μΑ	V <sub>DS</sub> = -12V, V <sub>GS</sub> =0V
Gate threshold voltage	VGS (th)	-0.3	-	-1.0	V	VDS= -6V, ID= -1mA
Static drain-source on-state resistance	R <sub>DS</sub> (on)	-	25	35	mΩ	I <sub>D</sub> = -4.5A, V <sub>G</sub> S= -4.5V
		_	31	43	mΩ	I <sub>D</sub> = -2.2A, V <sub>G</sub> S= -2.5V
		_	39	58	mΩ	I <sub>D</sub> = -2.2A, V <sub>G</sub> S= -1.8V
		_	50	100	mΩ	I <sub>D</sub> = -0.9A, V <sub>G</sub> s= -1.5V
Forward transfer admittance	Y <sub>fs</sub>   *	6.5	-	-	S	V <sub>DS</sub> = -6V, I <sub>D</sub> = -4.5A
Input capacitance	Ciss	-	2450	_	pF	V <sub>DS</sub> = -6V
Output capacitance	Coss	_	320	_	pF	V <sub>GS</sub> =0V
Reverse transfer capacitance	Crss	_	290	_	pF	f=1MHz
Turn-on delay time	t <sub>d (on)</sub> *	_	12	_	ns	I <sub>D</sub> = -2.2A
Rise time	tr *	_	75	_	ns	VDD≒ -6V VGS= -4.5V
Turn-off delay time	t <sub>d (off)</sub> *	-	390	_	ns	VGS= −4.5 V Ri≒ 2.7Ω
Fall time	t <sub>f</sub> *	_	215	_	ns	R <sub>G</sub> =10Ω
Total gate charge	Qg *	_	31	_	nC	V <sub>DD</sub> ≒−6V R <sub>L</sub> ≒1.3Ω
Gate-source charge	Q <sub>gs</sub> *	_	4.5	_	nC	V <sub>GS</sub> = -4.5V R <sub>G</sub> =10Ω
Gate-drain charge	Q <sub>gd</sub> *	1	4.0	-	nC	I <sub>D</sub> = -4.5A

<sup>\*</sup>Pulsed

# ●Body diode characteristics (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Forward voltage	Vsp *	_	_	-1.2	V	Is= -4.5A, Vgs=0V

<sup>\*</sup>Pulsed

#### Electrical characteristic curves

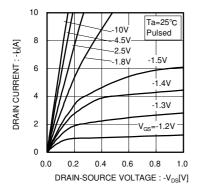


Fig.1 Typical Output Characteristics( I )

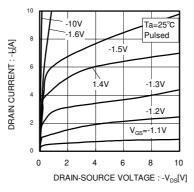


Fig.2 Typical Output Characteristics(  ${\rm I\hspace{-.1em}I}$  )

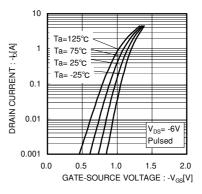


Fig.3 Typical Transfer Characteristics

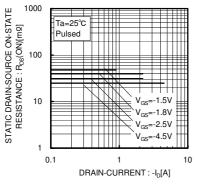


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current( I )

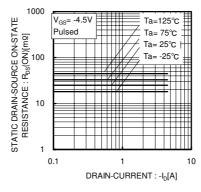


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current( II )

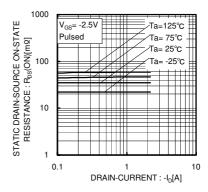


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(Ⅲ)

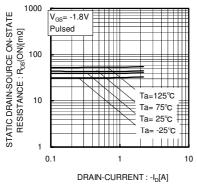


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(IV)

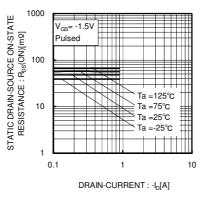


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current(V)

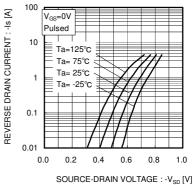


Fig.9 Reverse Drain Current
vs. Sourse-Drain Voltage

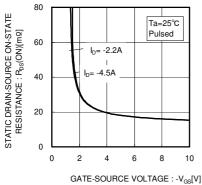


Fig.10 Static Drain-Source On-State
Resistance vs. Gate-Source Voltage

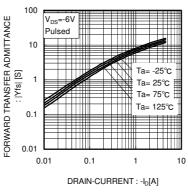


Fig.11 Forward Transfer Admittance vs. Drain Current

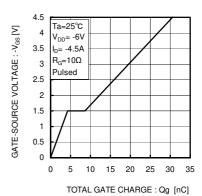
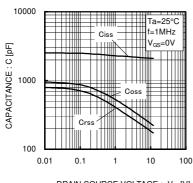


Fig.12 Dynamic Input Characteristics



DRAIN-SOURCE VOLTAGE: -V<sub>DS</sub>[V]
Fig.13 Typical Capacitance
vs. Drain-Source Voltage

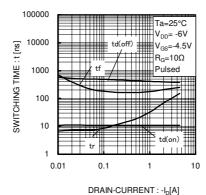


Fig.14 Switching Characteristics

#### Measurement circuits

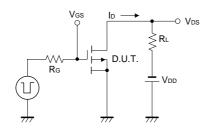


Fig.15 Switching Time Measurement Circuit

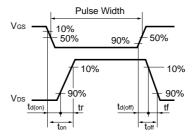


Fig.16 Switching Waveforms

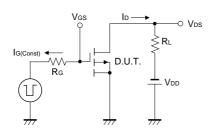


Fig.17 Gate Charge Measurement Circuit

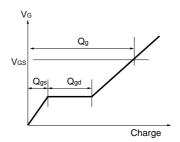


Fig.18 Gate Charge Waveform

# ●Notice

This product might cause chip aging and breakdown under the large electrified environment . Please consider to design ESD protection circuit.

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