



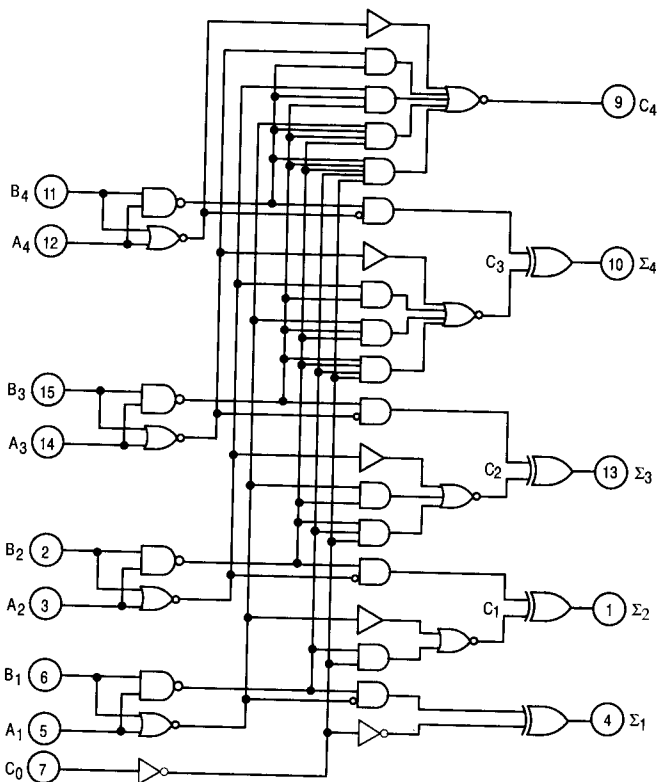
**MOTOROLA**

# 4-Bit Full Adder With Fast Carry

ELECTRICALLY TESTED PER:  
MIL-M-38510/31202

The 54LS283 is a high-speed 4-Bit Binary full adder with internal carry lookahead. It accepts two 4-bit binary words ( $A_1$ - $A_4$ ,  $B_1$ - $B_4$ ) and a Carry input ( $C_0$ ). It generates the binary Sum output ( $\Sigma_1$  -  $\Sigma_4$ ) and the Carry output ( $C_4$ ) from the most significant bit. The 'LS283 will operate with either active-HIGH or active-LOW operands (positive or negative logic).

LOGIC DIAGRAM



## Military 54LS283



### AVAILABLE AS:

- 1) JAN: JM38510/31202BXA
- 2) SMD: 7604301
- 3) 883: 54LS283/BXAJC

X = CASE OUTLINE AS FOLLOWS:  
 PACKAGE: CERDIP: E  
 CERFLAT: F  
 LCC: 2

THE LETTER "M" APPEARS  
 BEFORE THE / ON LCC.

### PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
$\Sigma_2$	1	1	2	VCC
$B_2$	2	2	3	VCC
$A_2$	3	3	4	VCC
$\Sigma_1$	4	4	5	VCC
$A_1$	5	5	7	VCC
$B_1$	6	6	8	VCC
$C_0$	7	7	9	VCC
GND	8	8	10	GND
$C_4$	9	9	12	VCC
$\Sigma_4$	10	10	13	VCC
$B_4$	11	11	14	VCC
$A_4$	12	12	15	VCC
$\Sigma_3$	13	13	17	VCC
$A_3$	14	14	18	VCC
$B_3$	15	15	19	VCC
VCC	16	16	20	VCC

BURN-IN CONDITIONS:  
 VCC = 5.0 V MIN/6.0 V MAX

## FUNCTIONAL DESCRIPTION

The 'LS283 adds two 4-bit binary words (A plus B) plus the incoming carry  $C_0$ . The binary sum appears on the Sum ( $\Sigma_1 - \Sigma_4$ ) and outgoing carry ( $C_4$ ) outputs.

$$C_0 + (A_1 + B_1) + 2(A_2 + B_2) + 4(A_3 + B_3) + 8(A_4 + B_4) = \Sigma_1 + 2\Sigma_2 + 4\Sigma_3 + 8\Sigma_4 + 16C_4$$

Where: (+) = plus

Due to the symmetry of the binary add function the 'LS283 can be used with either all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). Note that with active HIGH inputs, Carry Input can not be left open, but must be held LOW when no carry in is intended.

FUNCTION TABLE				
$C_{(n-1)}$	$A_n$	$B_n$	$\Sigma_n$	$C_n$
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

$C_1 - C_3$  are generated internally

$C_0$  is an external input

$C_4$  is an output generated internally

Pin Name		Loading (Note a)	
		HIGH	LOW
A <sub>1</sub> -A <sub>4</sub>	A Operand Inputs	1.0 U.L.	0.5 U.L.
B <sub>1</sub> -B <sub>4</sub>	B Operand Inputs	1.0 U.L.	0.5 U.L.
C <sub>0</sub>	Carry Output	0.5 U.L.	0.25 U.L.
$\Sigma_1 - \Sigma_4$	Sum Outputs (Note b)	10 U.L.	5(2.5) U.L.
C <sub>4</sub>	Carry Outputs (Note b)	10 U.L.	5(2.5) U.L.

## NOTES:

- One TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/ 1.6 mA LOW.
- The Output LOW drive factor is 2.5 U.L. for Military (54) Temperature Ranges.

	C <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	A <sub>4</sub>	B <sub>1</sub>	B <sub>2</sub>	B <sub>3</sub>	B <sub>4</sub>	$\Sigma_1$	$\Sigma_2$	$\Sigma_3$	$\Sigma_4$	C <sub>4</sub>
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active High	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active Low	1	1	0	1	0	0	1	1	0	0	0	1	1	0

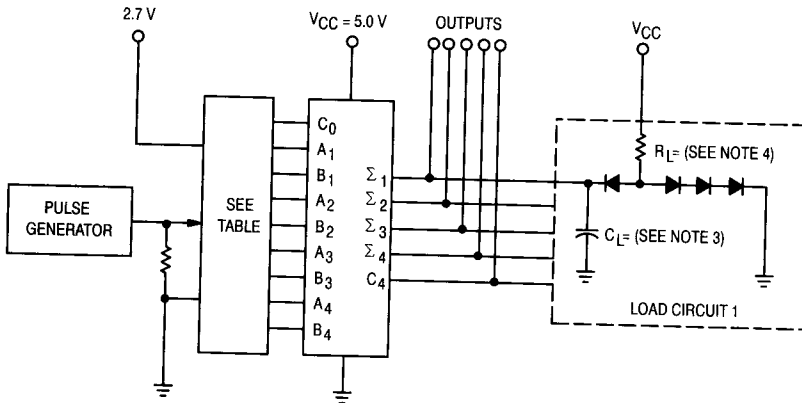
Interchanging inputs of equal weight does not effect the operation, thus C<sub>0</sub>, A<sub>1</sub>, B<sub>1</sub>, can be arbitrarily assigned to pins 7, 5 or 3.

$$(10 + 9 = 19)$$

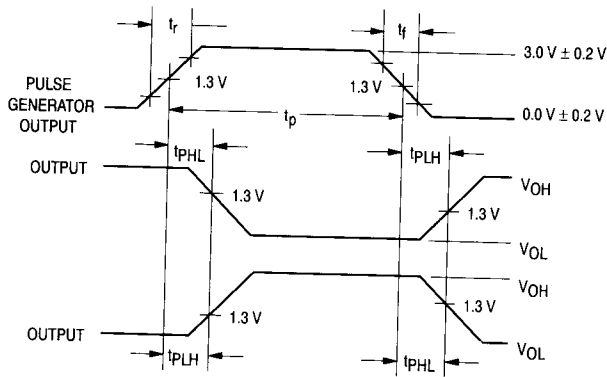
$$(\text{carry} + 5 + 6 = 12)$$

# 54LS283

## AC TEST CIRCUIT



## SWITCHING WAVEFORMS



### NOTES:

1. The pulse generator has the following characteristics:  
 $PRR \leq 1.0$  MHz,  $t_r \leq 15$  ns,  $t_f \leq 6.0$  ns,  $t_p = 200$  ns and  $Z_{OUT} \approx 50 \Omega$ .
2.  $C_L = 50$  pF  $\pm 10\%$ , including scope probe, wiring capacitance without package in test fixture.
3. All diodes are 1N3064 or equivalent.
4.  $R_L = 2.0$  k $\Omega \pm 5.0\%$ .
5. Terminal conditions (pins not designated may be high  $\geq 2.0$  V, or low  $\leq 0.7$  V, or open).

## 54LS283

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V <sub>OH</sub>	Logical "1" Output Voltage	2.5		2.5		2.5		V	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -0.4 mA, V <sub>IH</sub> = 2.0 V (all inputs).
V <sub>OL</sub>	Logical "0" Output Voltage		0.4		0.4		0.4	V	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 4.0 mA, V <sub>IL</sub> = 0.7 V (all inputs).
V <sub>IC</sub>	Input Clamping Voltage		-1.5					V	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA, other inputs are open.
I <sub>IH(C0)</sub>	Logical "1" Input Current		20		20		20	μA	V <sub>CC</sub> = 5.5 V, V <sub>IH</sub> = 2.7 V, other inputs are open.
I <sub>IHH(C0)</sub>	Logical "1" Input Current		100		100		100	μA	V <sub>CC</sub> = 5.5 V, V <sub>IHH</sub> = 5.5 V, other inputs are open.
I <sub>IH</sub>	Logical "1" Input Current		40		40		40	μA	V <sub>CC</sub> = 5.5 V, V <sub>IH</sub> = 2.7 V, other input = GND.
I <sub>IHH</sub>	Logical "1" Input Current		200		200		200	μA	V <sub>CC</sub> = 5.5 V, V <sub>IHH</sub> = 5.5 V, other input = GND.
I <sub>OS</sub>	Output Short Circuit Current	- 15	- 100	- 15	- 100	- 15	- 100	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 5.5 V (all inputs), V <sub>OUT</sub> = GND.
I <sub>IL</sub>	Logical "0" Input Current	- 0.3	- 0.76	- 0.3	- 0.76	- 0.3	- 0.76	mA	V <sub>CC</sub> = 5.5 V, V <sub>IL</sub> = 0.4 V, other input = 5.5 V.
I <sub>IL(C0)</sub>	Logical "0" Input Current	- 0.15	- 0.38	- 0.15	- 0.38	- 0.15	- 0.38	mA	V <sub>CC</sub> = 5.5 V, V <sub>IL</sub> = 0.4 V, other inputs are open.
I <sub>CCL</sub>	Power Supply Current Off		39		39		39	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = GND (all inputs).
I <sub>CCZ</sub>	Power Supply Current Off		34		34		34	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 5.5 V (A inputs only), other inputs = GND
I <sub>CCH</sub>	Power Supply Current Off		34		34		34	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 5.5 V (all inputs).
V <sub>IH</sub>	Logical "1" Input Voltage	2.0		2.0		2.0		V	V <sub>CC</sub> = 4.5 V.
V <sub>IL</sub>	Logical "0" Input Voltage		0.7		0.7		0.7	V	V <sub>CC</sub> = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V <sub>CC</sub> = 5.0 V, V <sub>INL</sub> = 0.4 V, and V <sub>INH</sub> = 2.5 V.

## 54LS283

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t <sub>PHL1</sub> t <sub>PHL1</sub>	Propagation Delay C <sub>0</sub> to Any Σ Output	5.0 —	35 24	5.0 —	40 35	5.0 —	40 35	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF.
t <sub>PLH1</sub> t <sub>PLH1</sub>	Propagation Delay C <sub>0</sub> to Any Σ Output	5.0 —	30 24	5.0 —	39 34	5.0 —	39 34	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF.
t <sub>PHL2</sub> t <sub>PHL2</sub>	Propagation Delay C <sub>0</sub> to Any Σ Output	5.0 —	35 24	5.0 —	40 35	5.0 —	40 35	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF.
t <sub>PLH2</sub> t <sub>PLH2</sub>	Propagation Delay C <sub>0</sub> to Any Σ Output	5.0 —	30 24	5.0 —	39 34	5.0 —	39 34	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF.
t <sub>PHL3</sub> t <sub>PHL3</sub>	Propagation Delay C <sub>0</sub> to Any Σ Output	5.0 —	35 24	5.0 —	40 35	5.0 —	40 35	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF.
t <sub>PLH3</sub> t <sub>PLH3</sub>	Propagation Delay C <sub>0</sub> to Any Σ Output	5.0 —	30 24	5.0 —	39 34	5.0 —	39 34	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF.
t <sub>PHL4</sub> t <sub>PHL4</sub>	Propagation Delay C <sub>0</sub> to Any Σ Output	5.0 —	35 24	5.0 —	40 35	5.0 —	40 35	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF.
t <sub>PLH4</sub> t <sub>PLH4</sub>	Propagation Delay C <sub>0</sub> to Any Σ Output	5.0 —	30 24	5.0 —	39 34	5.0 —	39 34	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF.
t <sub>PHL5</sub>	Propagation Delay /Data-Output C <sub>0</sub> to C <sub>4</sub>	5.0	28	5.0	35	5.0	35	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ.
t <sub>PLH5</sub>	Propagation Delay /Data-Output C <sub>0</sub> to C <sub>4</sub>	5.0	25	5.0	32	5.0	32	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ.
t <sub>PHL6</sub>	Propagation Delay /Data-Output A or B to Σ Output	5.0	35	5.0	40	5.0	40	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ.
t <sub>PLH6</sub>	Propagation Delay /Data-Output A or B to Σ Output	5.0	35	5.0	40	5.0	40	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ.
t <sub>PHL7</sub>	Propagation Delay /Data-Output A or B to Σ Output	5.0	35	5.0	40	5.0	40	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ.
t <sub>PLH7</sub>	Propagation Delay /Data-Output A or B to Σ Output	5.0	35	5.0	40	5.0	40	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ.
t <sub>PHL8</sub>	Propagation Delay /Data-Output A or B to Σ Output	5.0	35	5.0	40	5.0	40	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ.
t <sub>PLH8</sub>	Propagation Delay /Data-Output A or B to Σ Output	5.0	35	5.0	40	5.0	40	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ.
t <sub>PHL9</sub>	Propagation Delay /Data-Output A or B to Σ Output	5.0	35	5.0	40	5.0	40	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ.
t <sub>PLH9</sub>	Propagation Delay /Data-Output A or B to Σ Output	5.0	35	5.0	40	5.0	40	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ.

## NOTE:

1. The limit specified for C<sub>L</sub> = 15 pF is guaranteed but not tested.