

HA1630D04/05/06 Series

Ultra-Small Low Voltage Operation CMOS Dual Operational Amplifier

R03DS0111EJ0100

Rev.1.00

Nov. 30, 2017

Description

The HA1630D04/05/06 are high slew rate dual CMOS Operational Amplifiers realizing low voltage operation, low input offset voltage and low supply current. In addition to a low operating voltage from 1.8V, these device output can achieve full swing output voltage capability extending to either supply. Available in an ultra-small TSSOP-8 and MPAK-8 package that occupy more small area against the SOP-8.

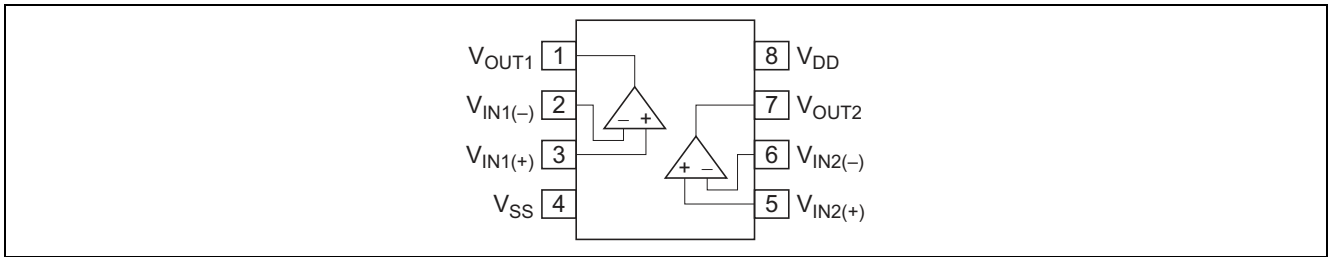
Features

- Low power and single supply operation $V_{DD} = 1.8$ to 5.5 V
- Low input offset voltage $V_{IO} = 4.0$ mV Max
- Low supply current (per channel) $I_{DD} = 200$ μ A Typ (HA1630D04)
 $I_{DD} = 400$ μ A Typ (HA1630D05)
 $I_{DD} = 800$ μ A Typ (HA1630D06)
- High slew rate $SR = 2$ V/ μ s Typ (HA1630D04)
 $SR = 4$ V/ μ s Typ (HA1630D05)
 $SR = 8$ V/ μ s Typ (HA1630D06)
- Maximum output voltage $V_{OH} = 2.9$ V Min (at $V_{DD} = 3.0$ V)
- Low input bias current $I_{IB} = 1$ pA Typ

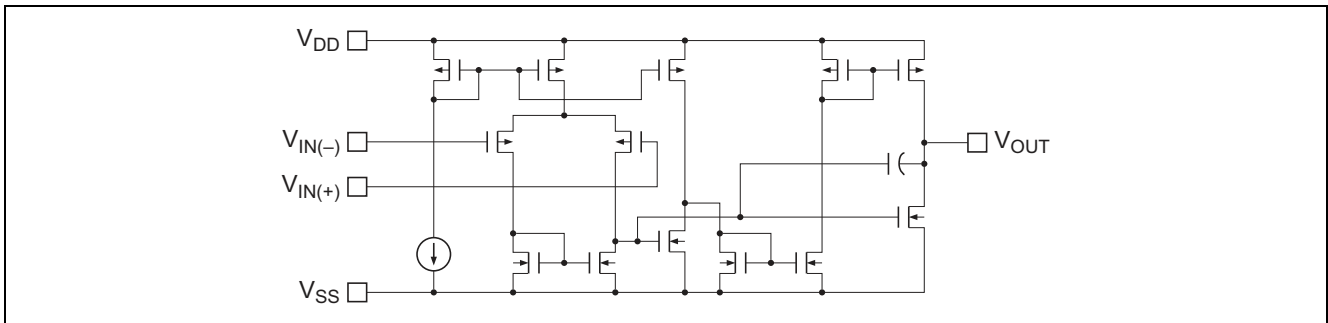
Ordering Information

Type No.	Package Name	Package Code
HA1630D04T	TTP-8DA	PTSP0008JC-B
HA1630D05T		
HA1630D06T		
HA1630D04MM	MPAK-8	PLSP0008JC-A
HA1630D05MM		
HA1630D06MM		

Pin Arrangement



Equivalent Circuit (per one channel)



Absolute Maximum Ratings

(Ta = 25°C)

Items	Symbol	Ratings	Unit	Note
Supply voltage	V _{DD}	7	V	
Differential input voltage	V _{IN(diff)}	-V _{DD} to +V _{DD}	V	
Input voltage	V _{IN}	-0.3 to +V _{DD}	V	*1
Power dissipation	P _T	240/145	mW	TTP-8DA/MMPAK-8 *2
Operating temp. Range	Topr	-40 to +85	°C	
Storage temp. Range	Tstg	-55 to +125	°C	

Notes: 1. Do not apply Input Voltage exceeding V_{DD} or 7 V.2. The value of PTSP0008JC-B (TTP-8DAV) / PLSP0008JC-A (MMPAK-8). It computes from heat resistance $\theta_{ja} = 520^{\circ}\text{C}/\text{W}$, and $690^{\circ}\text{C}/\text{W}$ each other.

Electrical Characteristics

(V_{DD} = 3.0 V, Ta = 25°C)

Items	Symbol	Min	Typ	Max	Unit	Test Condition
Input offset voltage	V _{IO}	—	—	4.0	mV	V _{in} = 1.5 V
Input offset current	I _{IO}	—	(1.0)	—	pA	V _{in} = 1.5 V
Input bias current	I _{IB}	—	(1.0)	—	pA	V _{in} = 1.5 V
Output high voltage	V _{OH}	2.9	—	—	V	R _L = 100 k Ω
Output source current	I _{O SOURCE}	100	200	—	μA	V _{OH} = 2.5 V (HA1630D04)
		200	400	—		V _{OH} = 2.5 V (HA1630D05)
		400	800	—		V _{OH} = 2.5 V (HA1630D06)
Output low voltage	V _{OL}	—	—	0.1	V	R _L = 100 k Ω
Output sink current	I _{O SINK}	—	(5.0)	—	mA	V _{OL} = 0.5 V (HA1630D04)
		—	(6.0)	—		V _{OL} = 0.5 V (HA1630D05)
		—	(6.5)	—		V _{OL} = 0.5 V (HA1630D06)
Common mode input voltage range	V _{CM}	-0.05 to 2.1	—	—	V	(HA1630D04, HA1630D05)
		0 to 1.9	—	—		(HA1630D06)
Slew rate	SR	—	(2.0)	—	V/ μs	C _L = 20 pF (HA1630D04)
		—	(4.0)	—		C _L = 20 pF (HA1630D05)
		—	(8.0)	—		C _L = 20 pF (HA1630D06)
Voltage gain	A _V	60	90	—	dB	
Gain bandwidth product	BW	—	(2100)	—	kHz	C _L = 20 pF (HA1630D04)
		—	(3300)	—		C _L = 20 pF (HA1630D05)
		—	(3600)	—		C _L = 20 pF (HA1630D06)
Power supply rejection ratio	PSRR	50	70	—	dB	
Common mode rejection ratio	CMRR	50	70	—	dB	
Supply current	I _{DD}	—	400	800	μA	R _L = ∞ (HA1630D04)
		—	800	1600		R _L = ∞ (HA1630D05)
		—	1600	3400		R _L = ∞ (HA1630D06)

Notes: 1. In the case of continuous current flow, use a sink current of under 4 mA.

2. () : Design specification

Table of Graphs

Electrical Characteristics			HA1630D04 Figure	HA1630D05 Figure	HA1630D06 Figure	Test Circuit
Supply current	I_{DD}	vs Supply voltage	1-1	2-1	3-1	2
		vs Ambient temperature	1-2	2-2	3-2	
Output high voltage	V_{OH}	vs Output source current	1-3	2-3	3-3	4
		vs Supply voltage	1-4	2-4	3-4	
Output source current	$I_{O\ SOURCE}$	vs Ambient temperature	1-5	2-5	3-5	6
Output low voltage	V_{OL}	vs Output sink current	1-6	2-6	3-6	5
Output sink current	$I_{O\ SINK}$	vs Ambient temperature	1-7	2-7	3-7	6
Input offset voltage	V_{IO}	Distribution	1-8	2-8	3-8	1
		vs Supply voltage	1-9	2-9	3-9	
		vs Ambient temperature	1-10	2-10	3-10	
Common mode input voltage range	V_{CM}	vs Ambient temperature	1-11	2-11	3-11	7
Power supply rejection ratio	PSRR	vs Frequency	1-12	2-12	3-12	1
Common mode rejection ratio	CMRR	vs Frequency	1-13	2-13	3-13	7
Voltage gain & phase angle	A_V	vs Frequency	1-14	2-14	3-14	10
Input bias current	I_{IB}	vs Ambient temperature	1-15	2-15	3-15	3
		vs Input voltage	1-16	2-16	3-16	
Slew Rate (rising)	SRr	vs Ambient temperature	1-17	2-17	3-17	9
Slew Rate (falling)	SRf	vs Ambient temperature	1-18	2-18	3-18	
Slew rate		Large signal transient response	1-19	2-19	3-19	
		Small signal transient response	1-20	2-20	3-20	
Total harmonic distortion + noise	(0 dB)	vs. Output voltage p-p	1-21	2-21	3-21	8
	(40 dB)	vs. Output voltage p-p	1-22	2-22	3-22	
Maximum p-p output voltage		vs Frequency	1-23	2-23	3-23	
Voltage noise density		vs Frequency	1-24	2-24	3-24	
Channel separation		vs Frequency	1-25	2-25	3-25	

Main Characteristics (HA1630D04)

Figure 1-1. HA1630D04
Supply Current vs. Supply Voltage

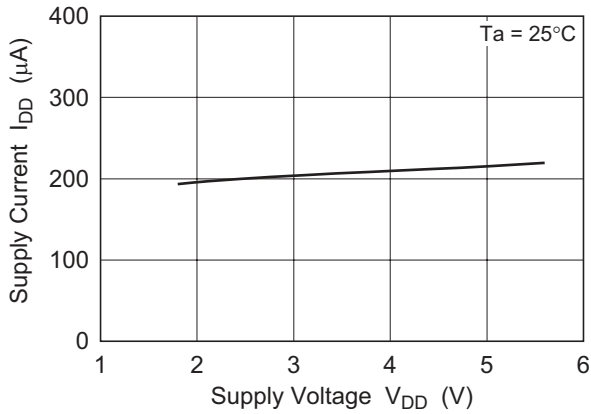


Figure 1-2. HA1630D04
Supply Current vs. Ambient Temperature

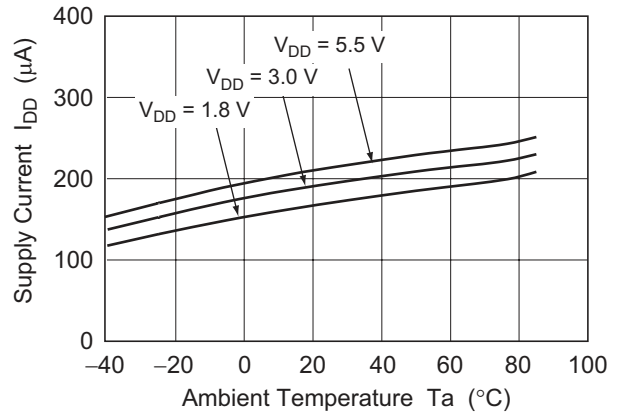


Figure 1-3. HA1630D04
Output High Voltage vs. Output Source Current

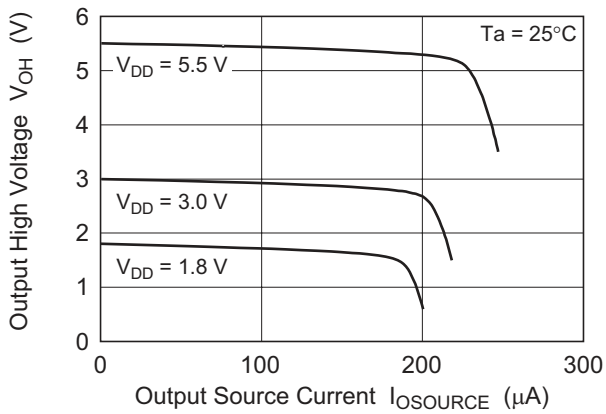


Figure 1-4. HA1630D04
Output High Voltage vs. Supply Voltage

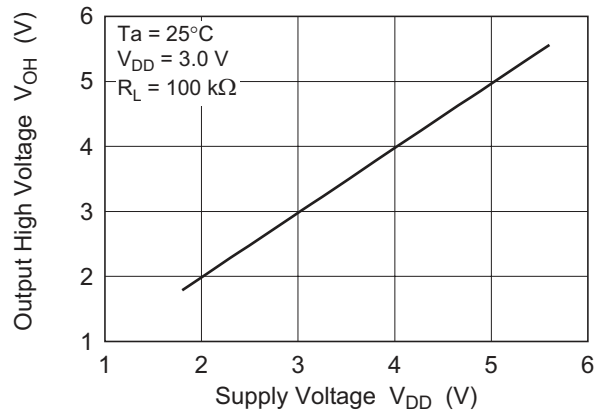
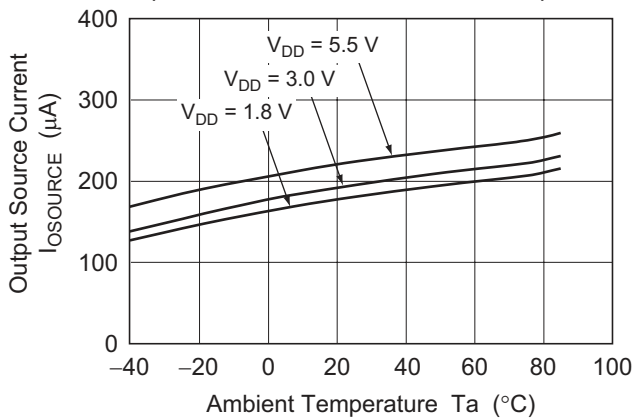


Figure 1-5. HA1630D04
Output Source Current vs. Ambient Temperature



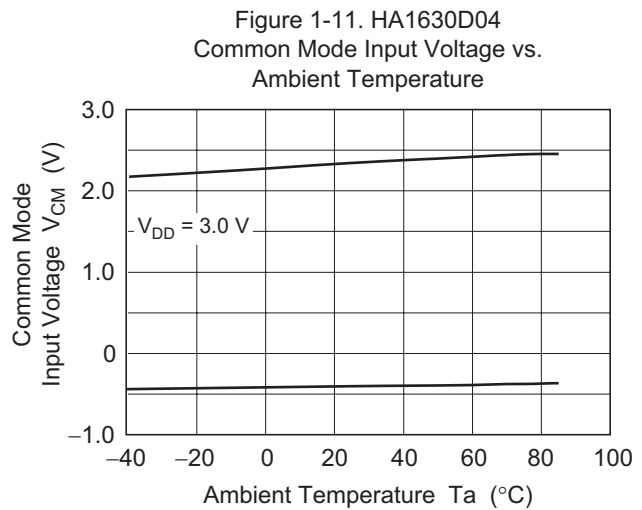
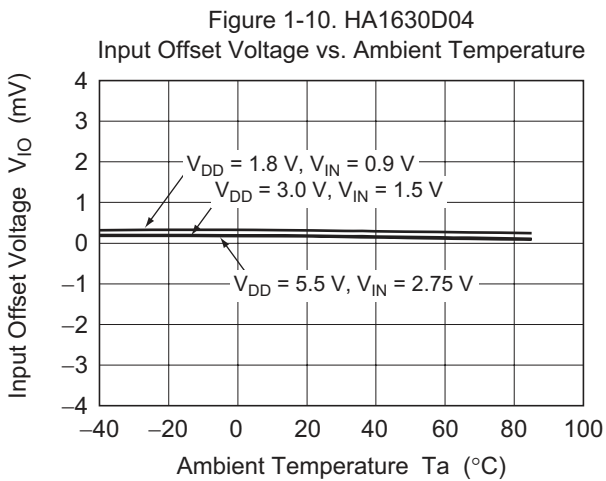
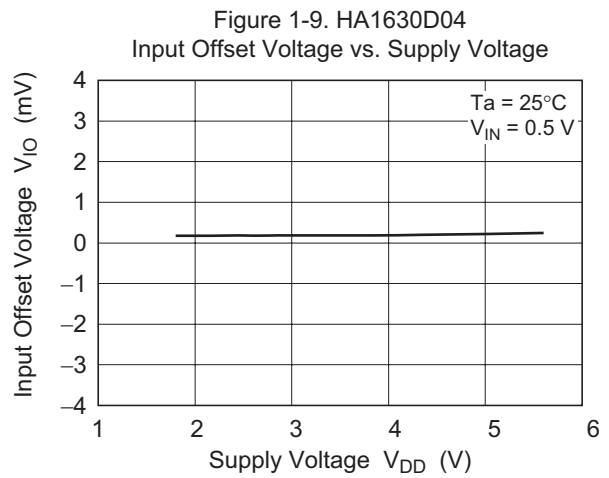
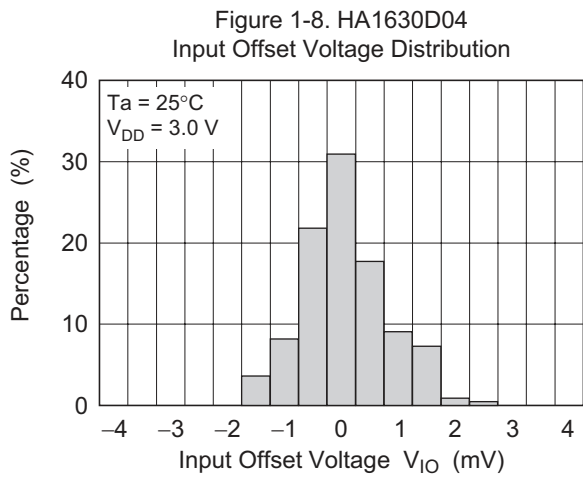
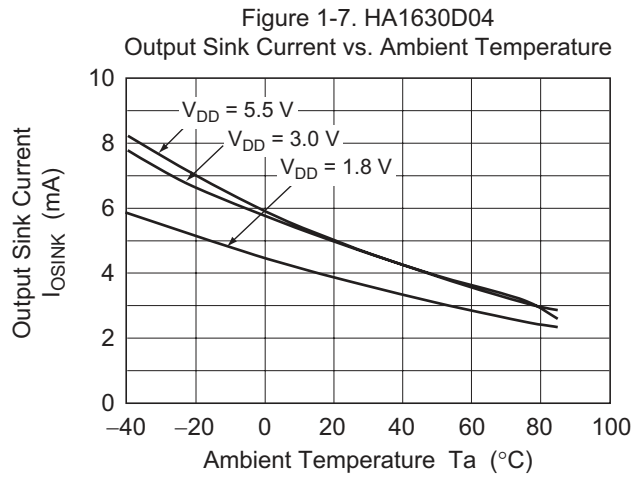
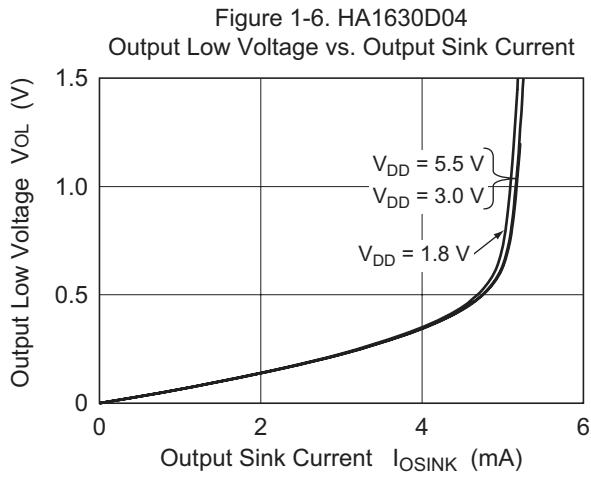


Figure 1-12. HA1630D04
Power Supply Rejection Ratio vs. Frequency

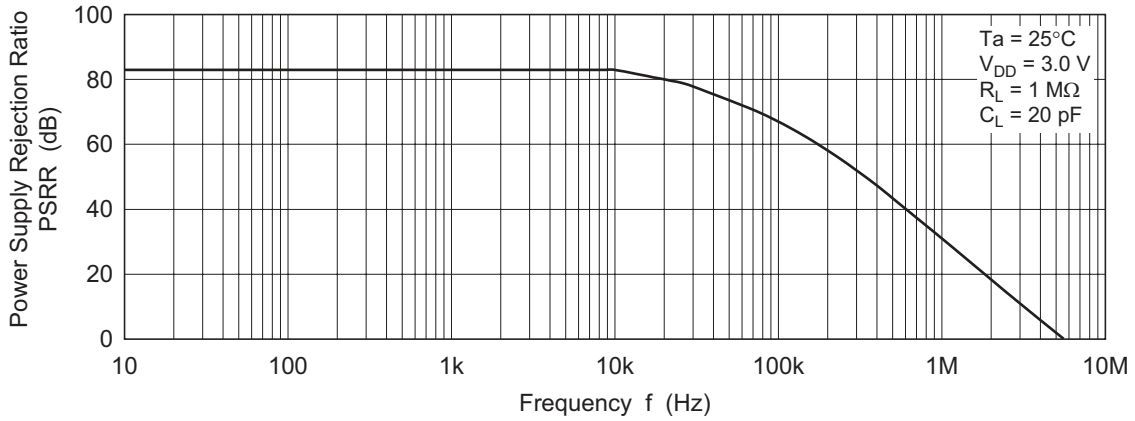


Figure 1-13. HA1630D04
Common Mode Rejection Ratio vs. Frequency

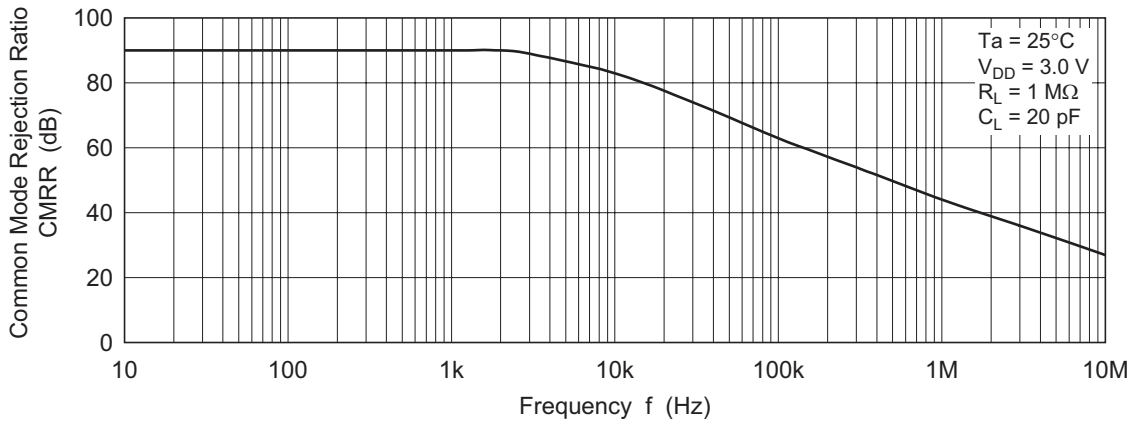
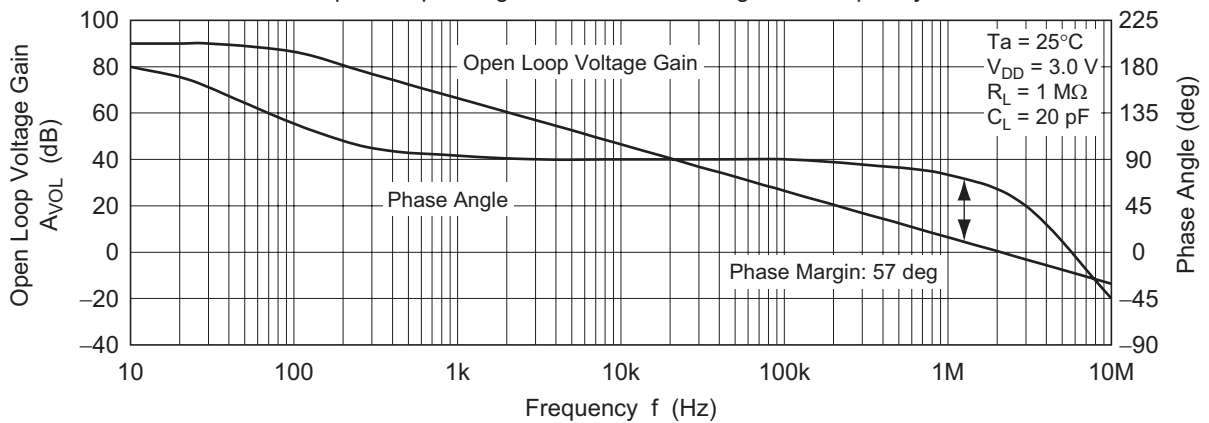


Figure 1-14. HA1630D04
Open Loop Voltage Gain and Phase Angle vs. Frequency



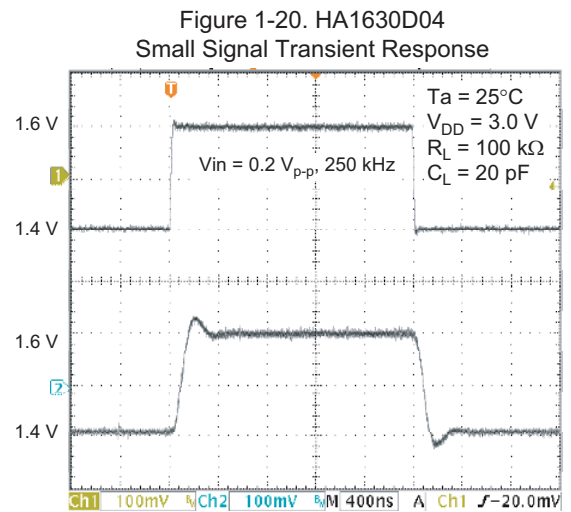
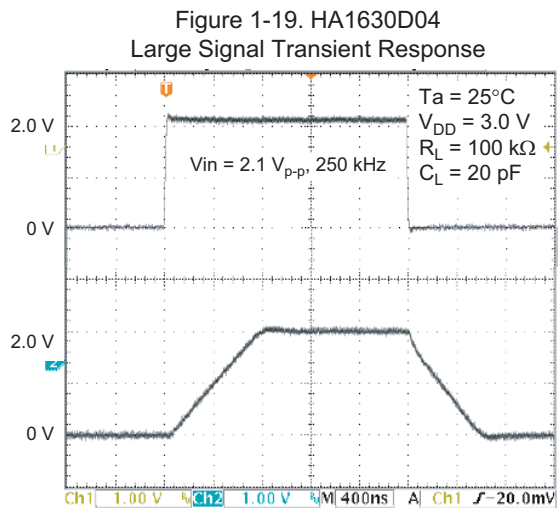
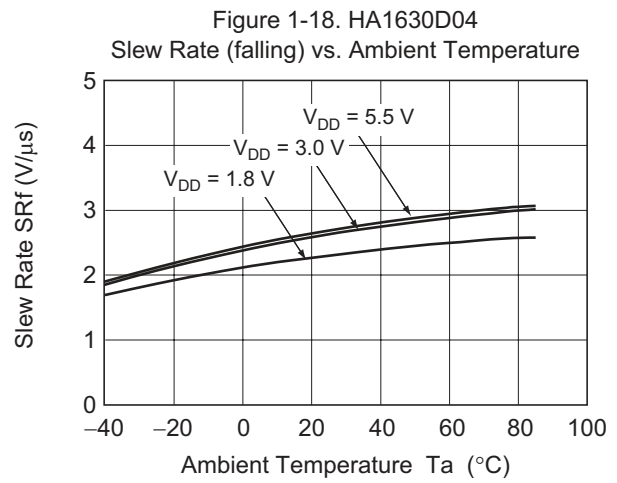
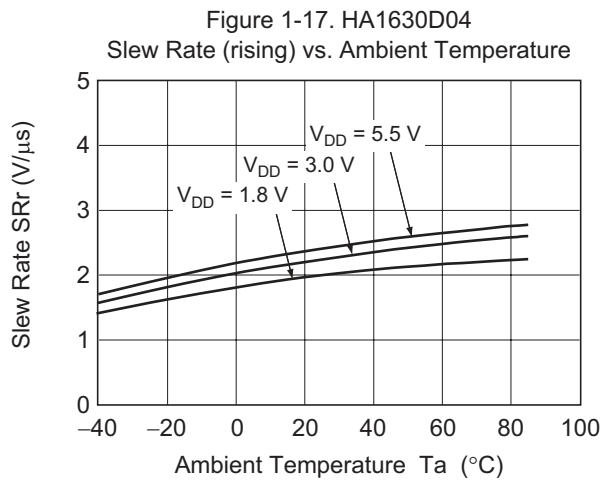
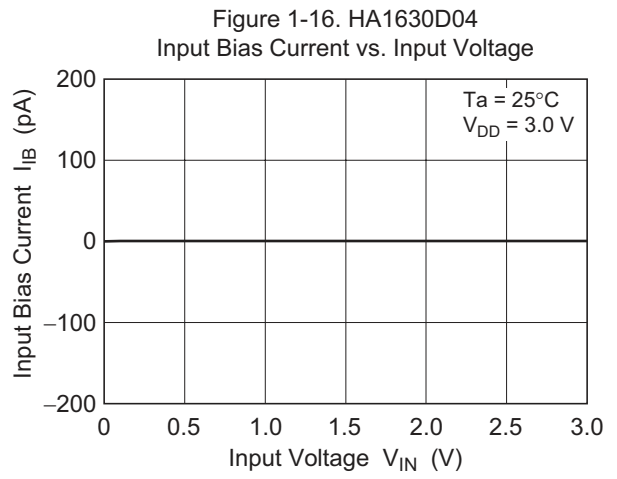
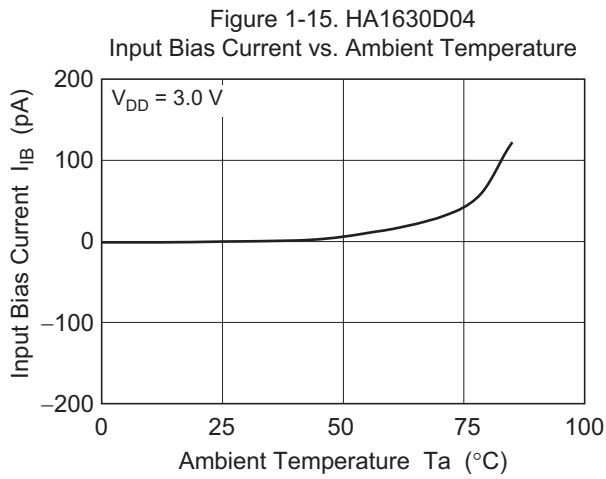


Figure 1-21. HA1630D04
Total Harmonic Distortion + Noise vs.
Output Voltage p-p

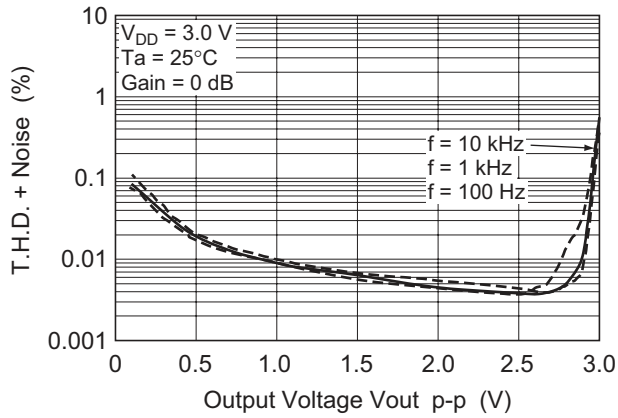


Figure 1-22. HA1630D04
Total Harmonic Distortion + Noise vs.
Output Voltage p-p

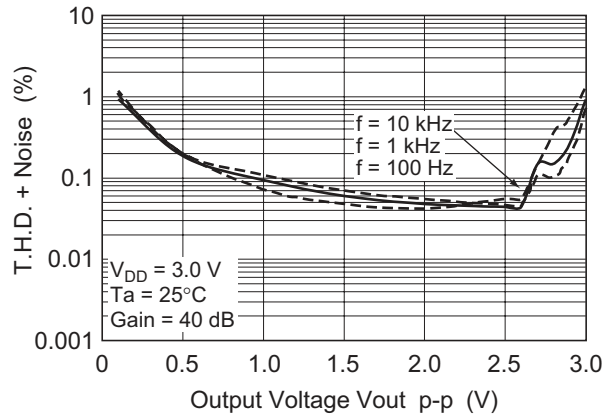


Figure 1-23. HA1630D04
Voltage Output p-p vs. Frequency

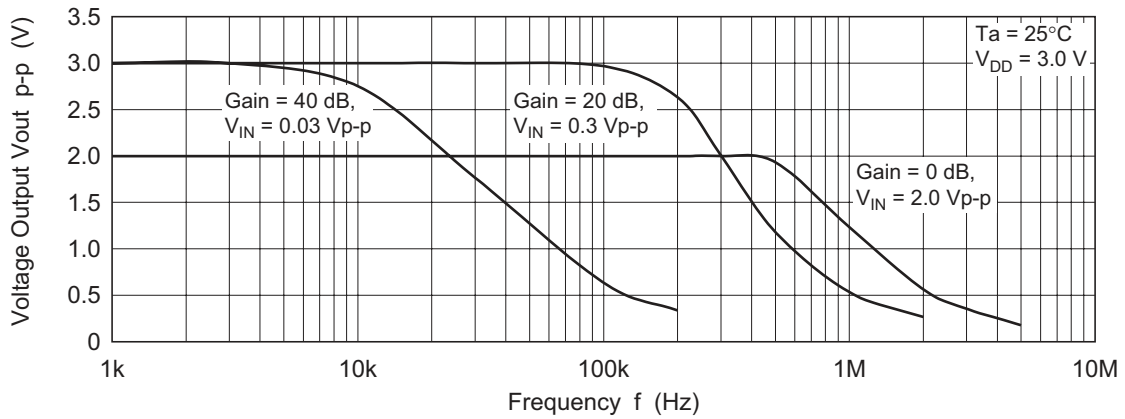


Figure 1-24. HA1630D04
Voltage Noise Density vs. Frequency

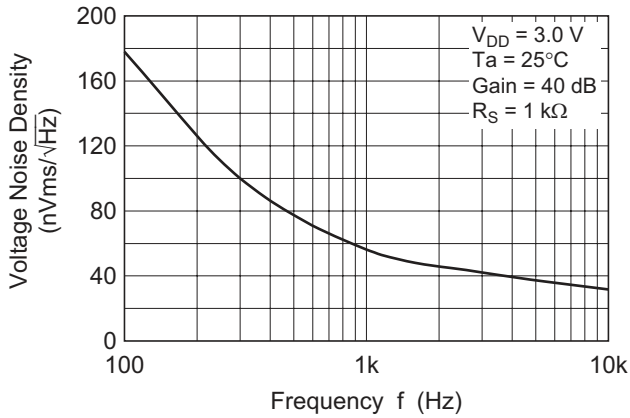
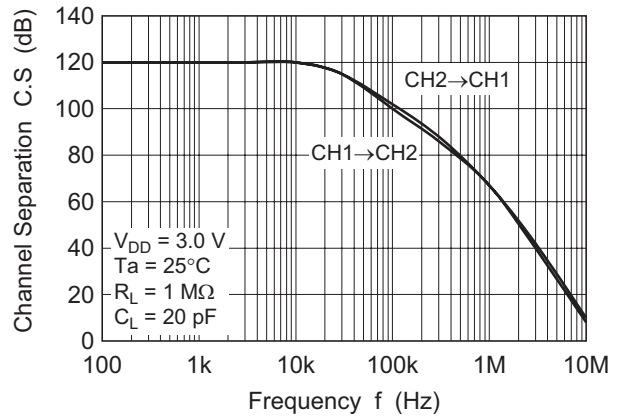
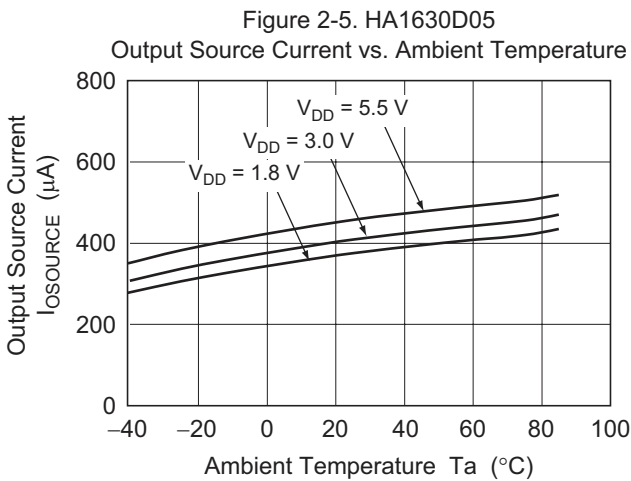
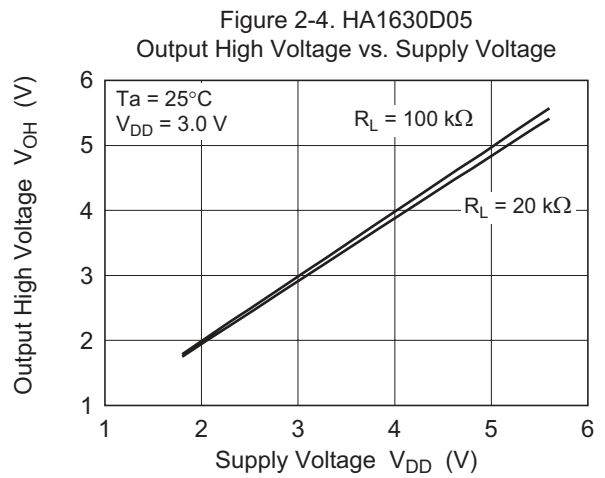
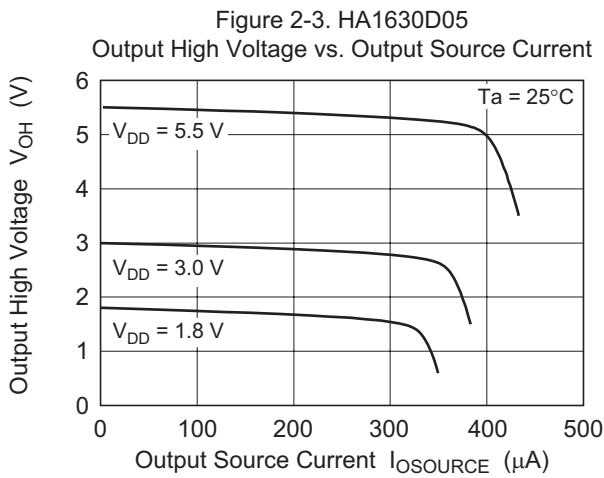
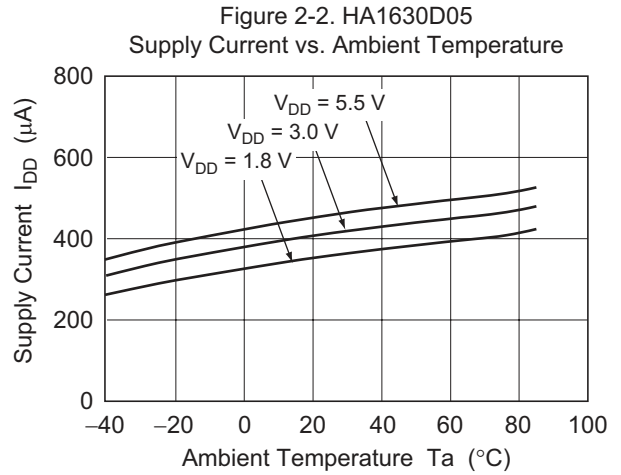
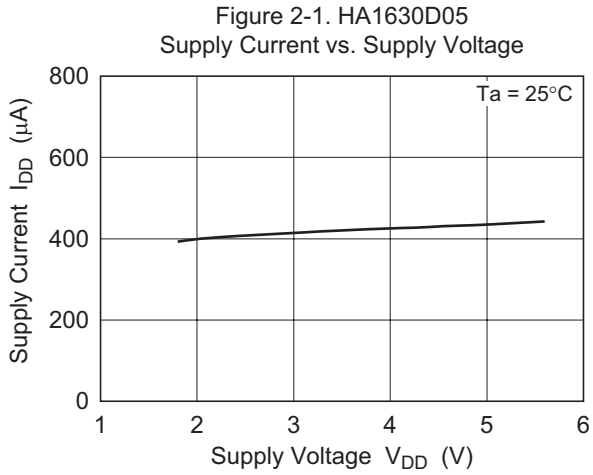


Figure 1-25. HA1630D04
Channel Separation vs. Frequency



Main Characteristics (HA1630D05)



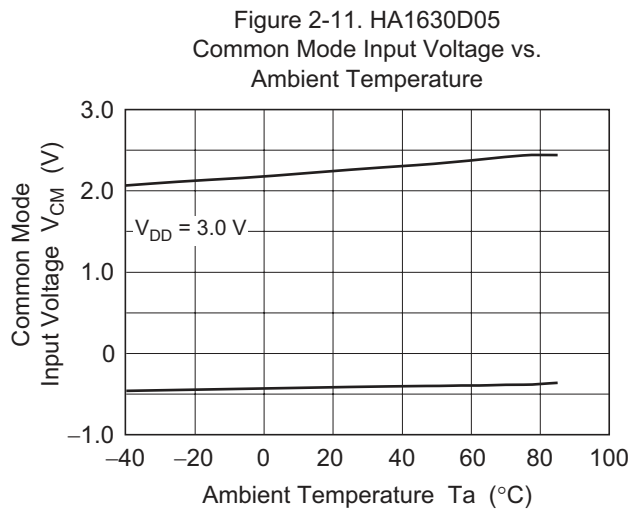
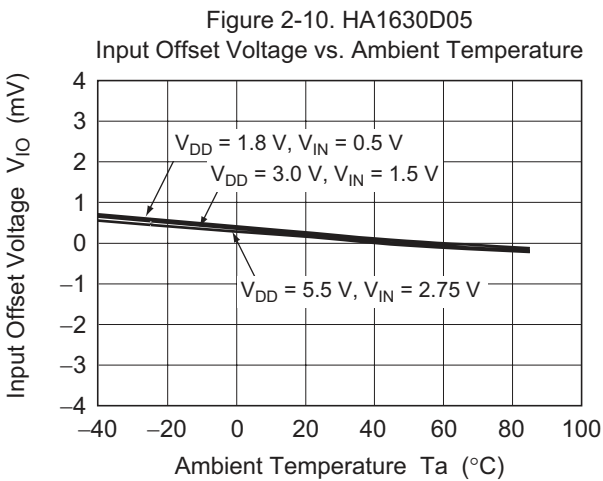
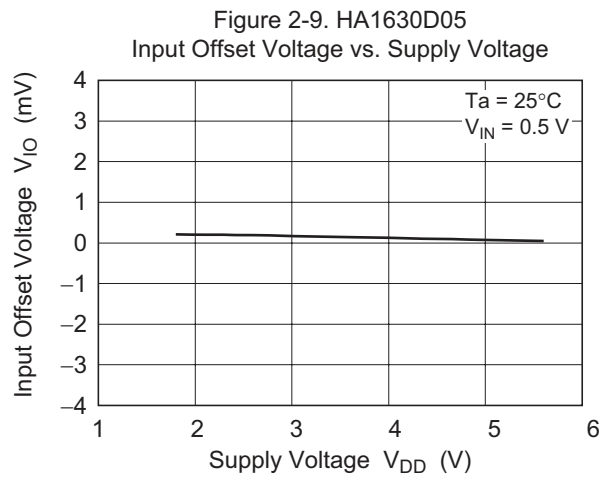
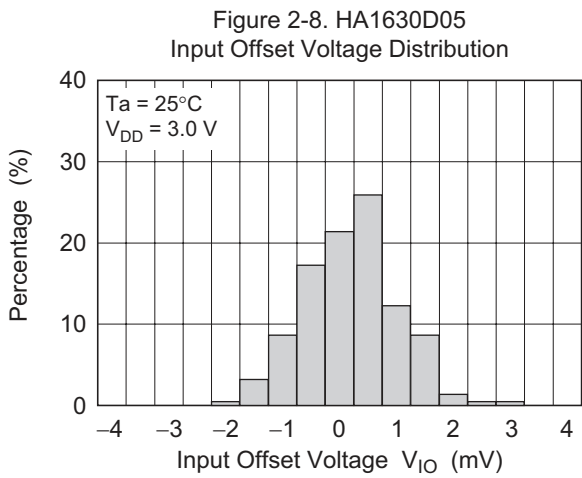
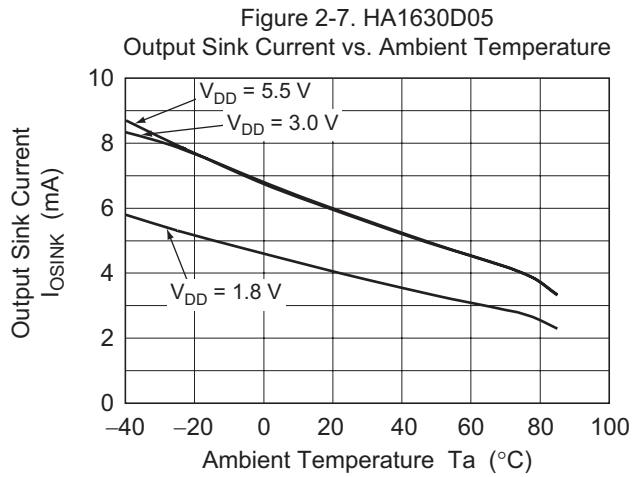
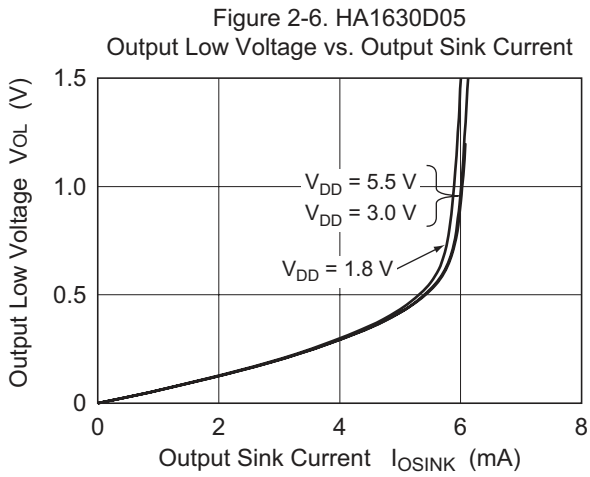


Figure 2-12. HA1630D05
Power Supply Rejection Ratio vs. Frequency

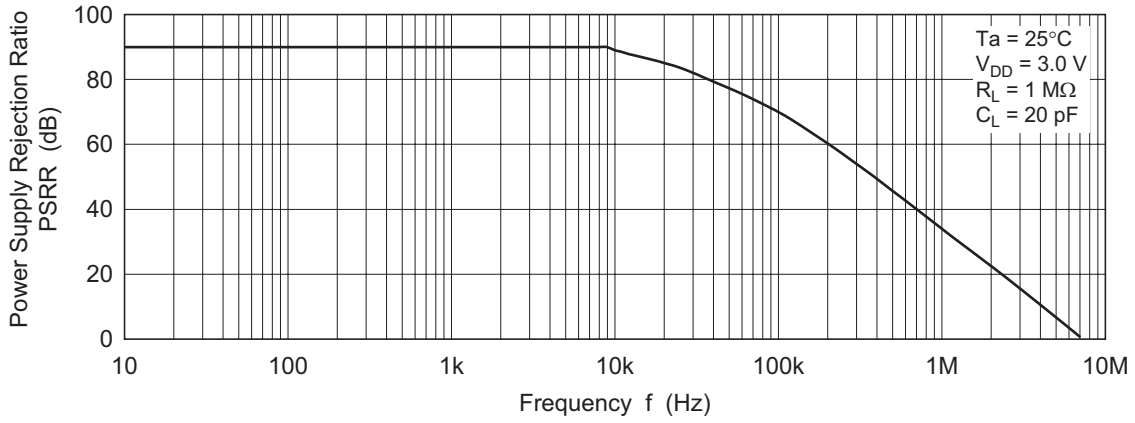


Figure 2-13. HA1630D05
Common Mode Rejection Ratio vs. Frequency

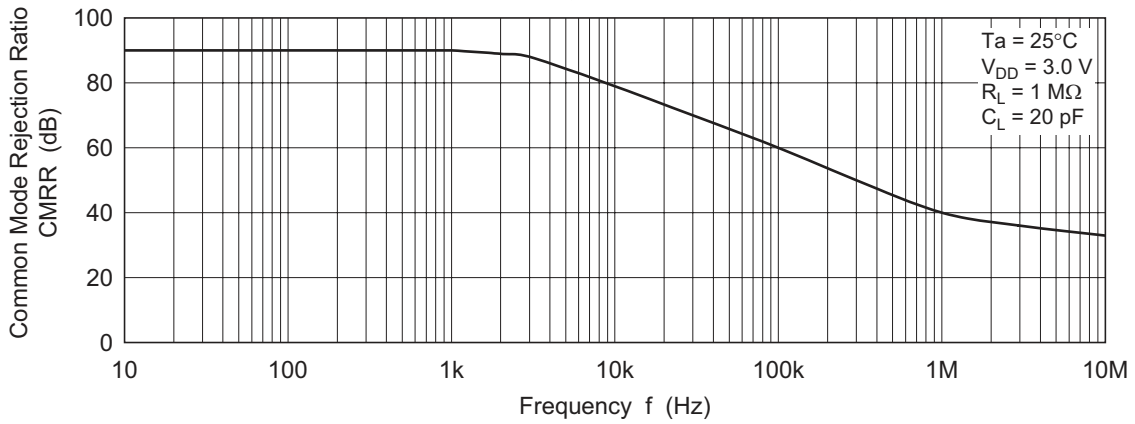
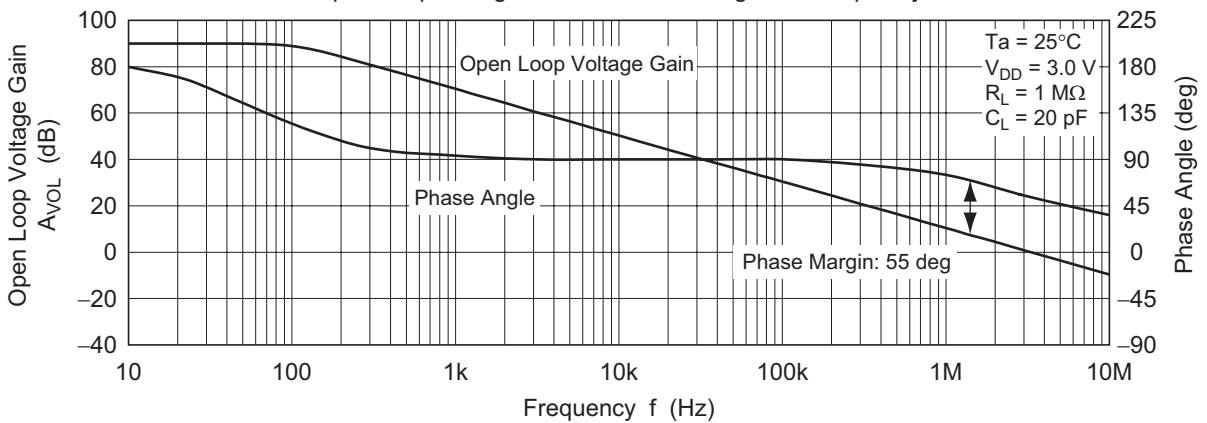


Figure 2-14. HA1630D05
Open Loop Voltage Gain and Phase Angle vs. Frequency



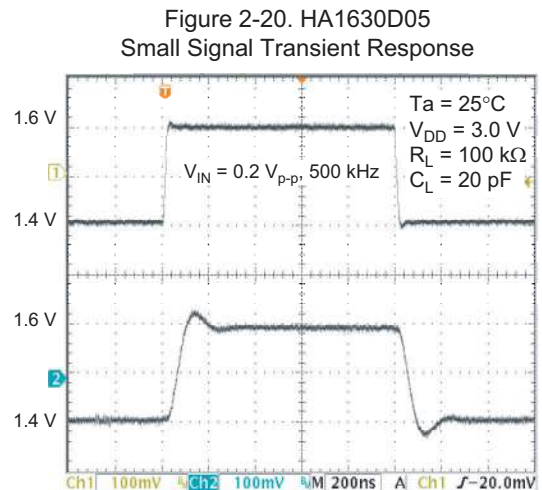
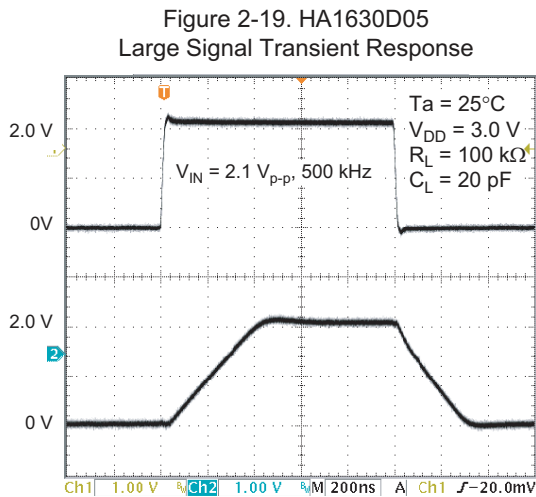
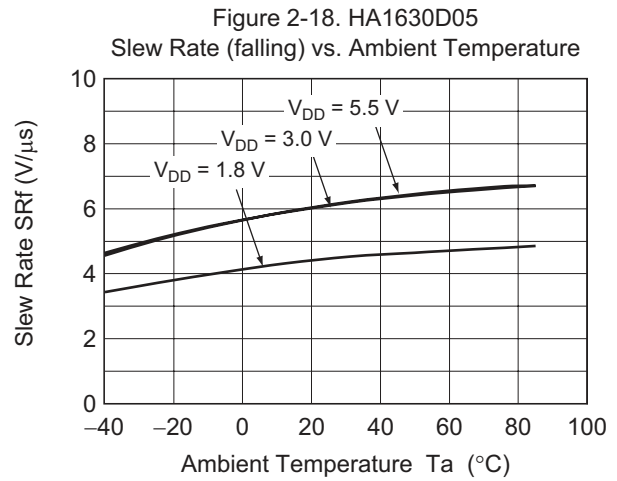
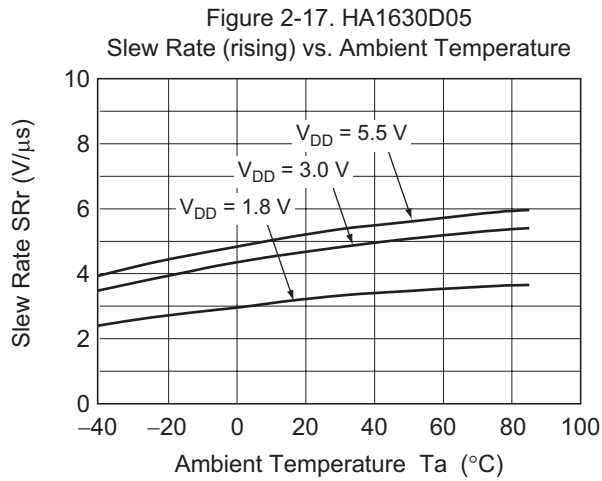
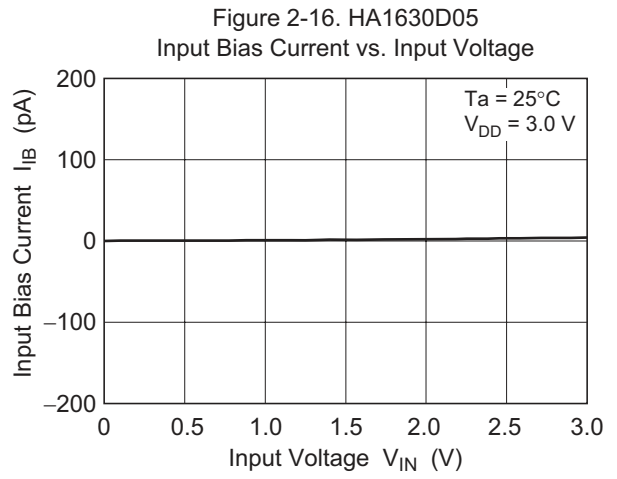
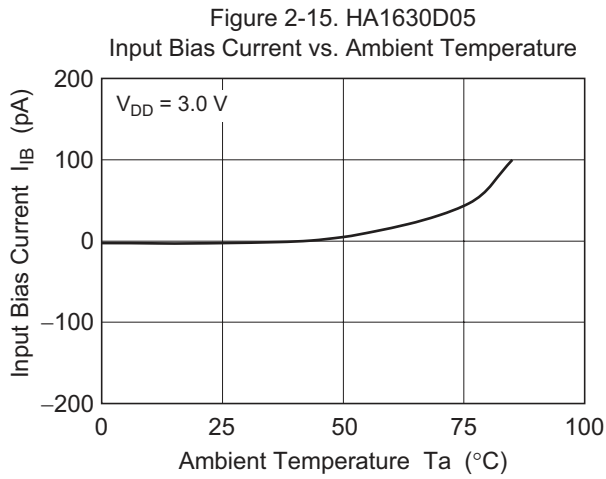


Figure 2-21. HA1630D05
Total Harmonic Distortion + Noise vs.
Output Voltage p-p

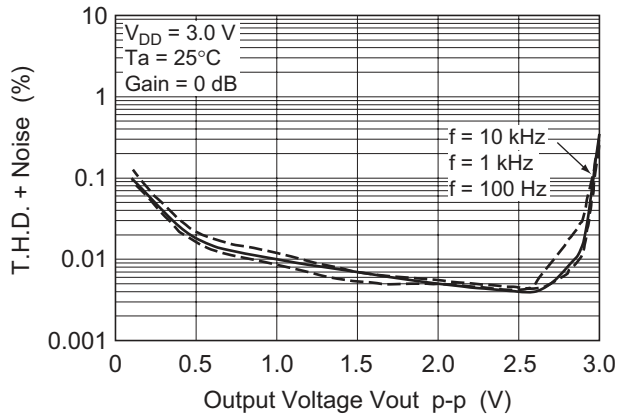


Figure 2-22. HA1630D05
Total Harmonic Distortion + Noise vs.
Output Voltage p-p

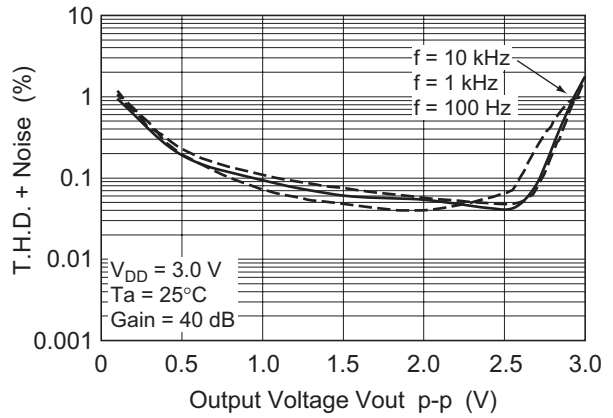


Figure 2-23. HA1630D05
Voltage Output p-p vs. Frequency

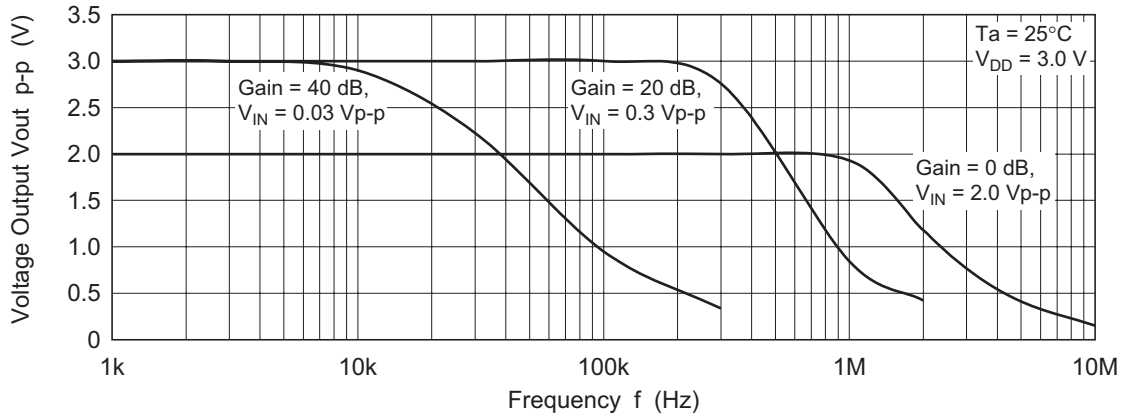


Figure 2-24. HA1630D05
Voltage Noise Density vs. Frequency

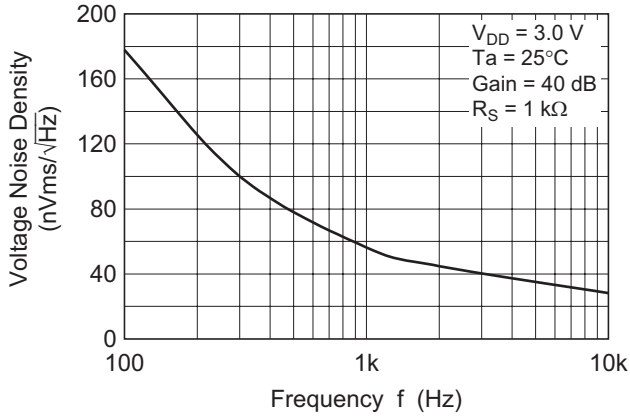
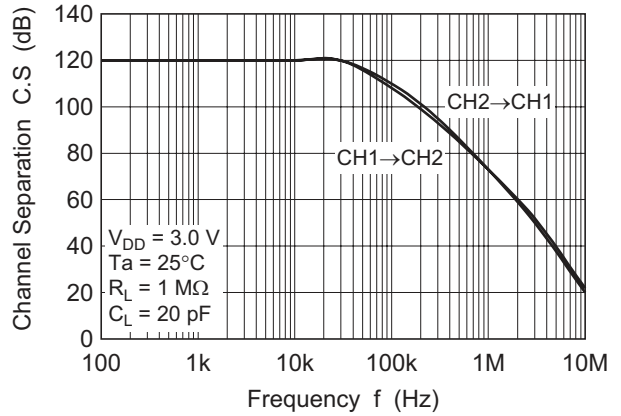
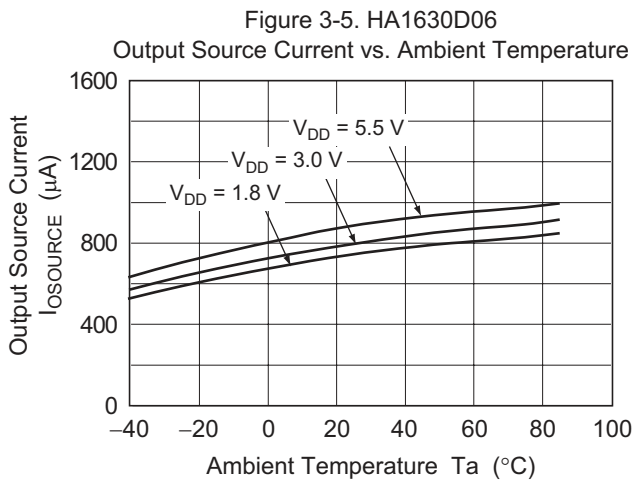
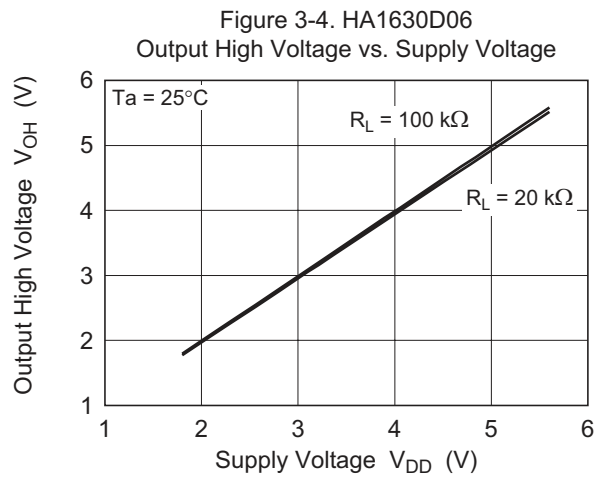
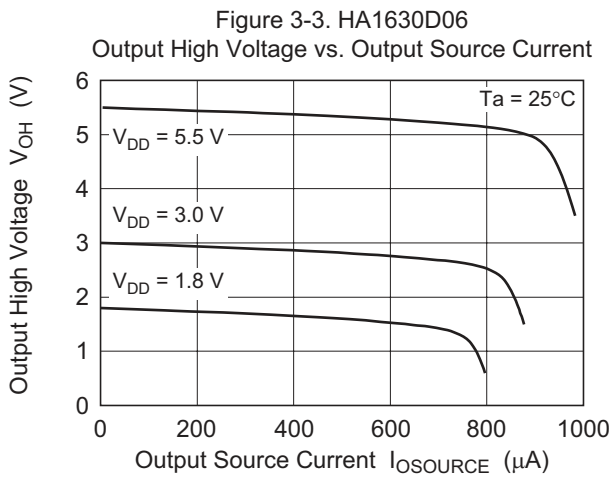
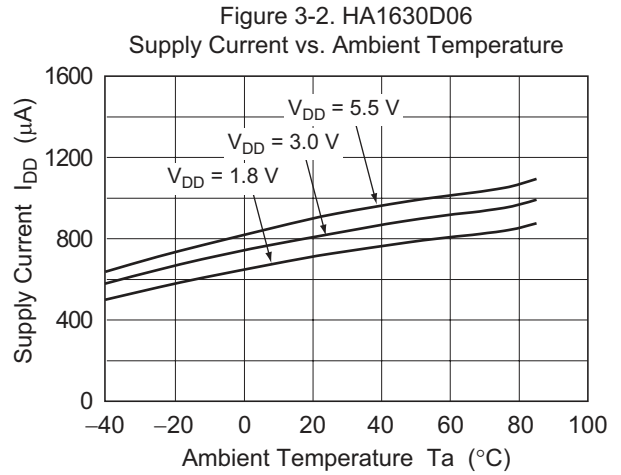
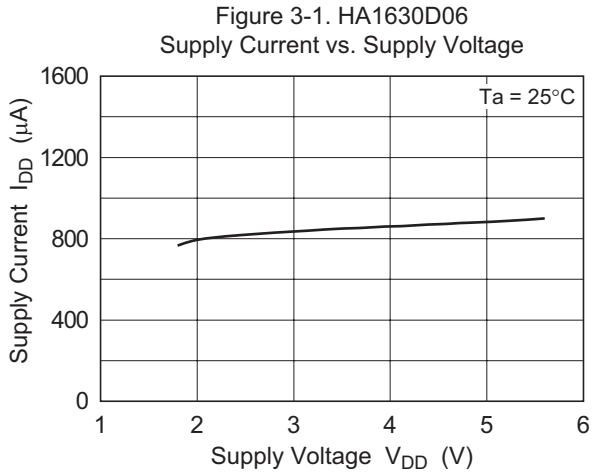


Figure 2-25. HA1630D05
Channel Separation vs. Frequency



Main Characteristics (HA1630D06)



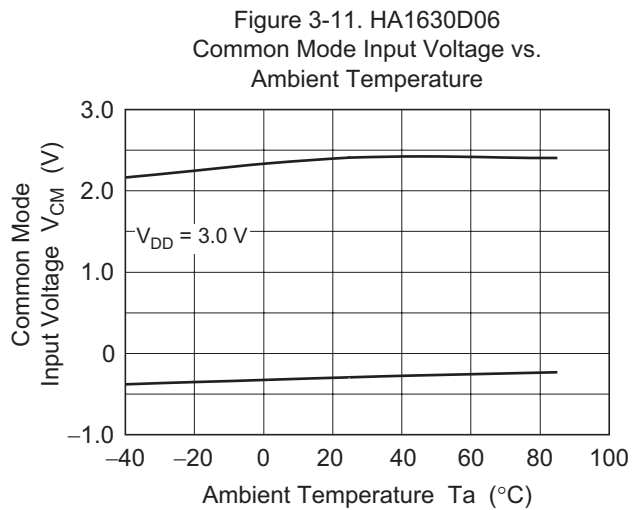
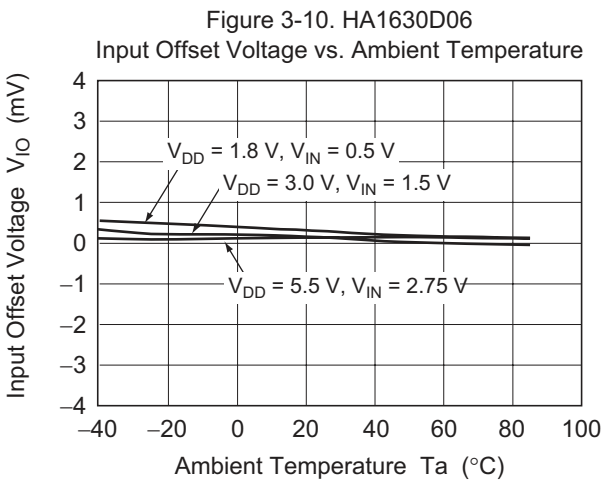
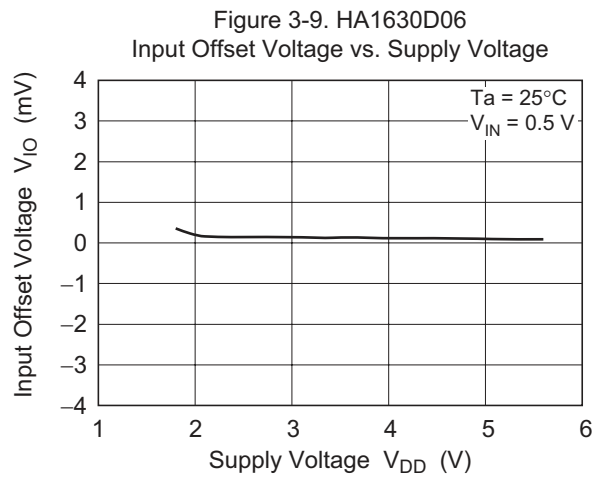
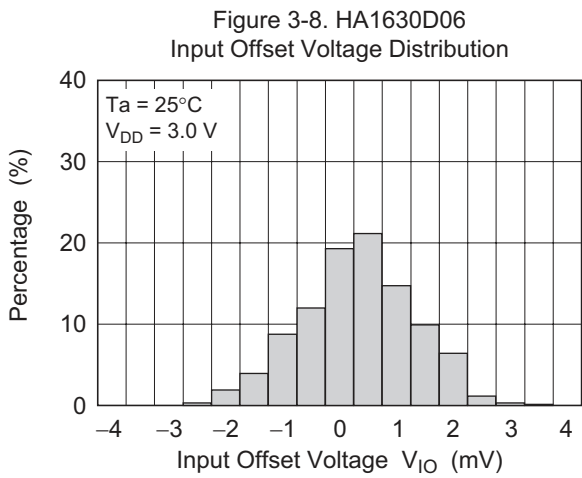
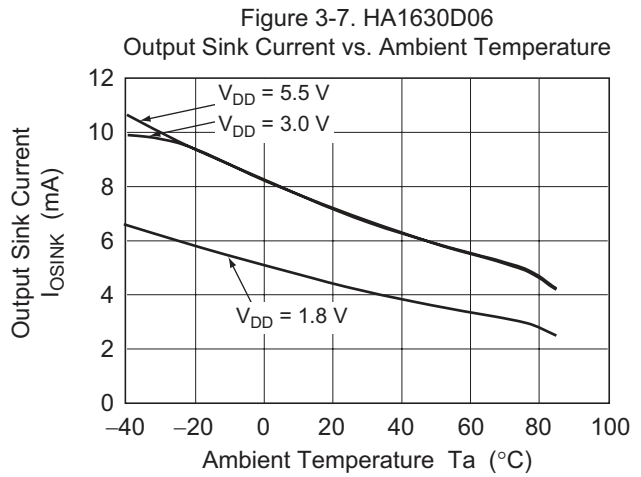
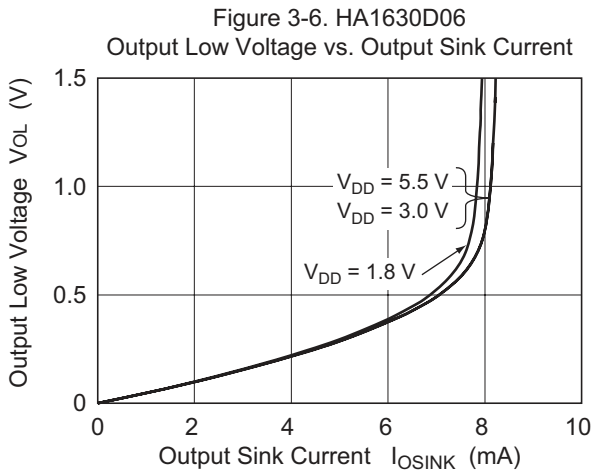


Figure 3-12. HA1630D06
Power Supply Rejection Ratio vs. Frequency

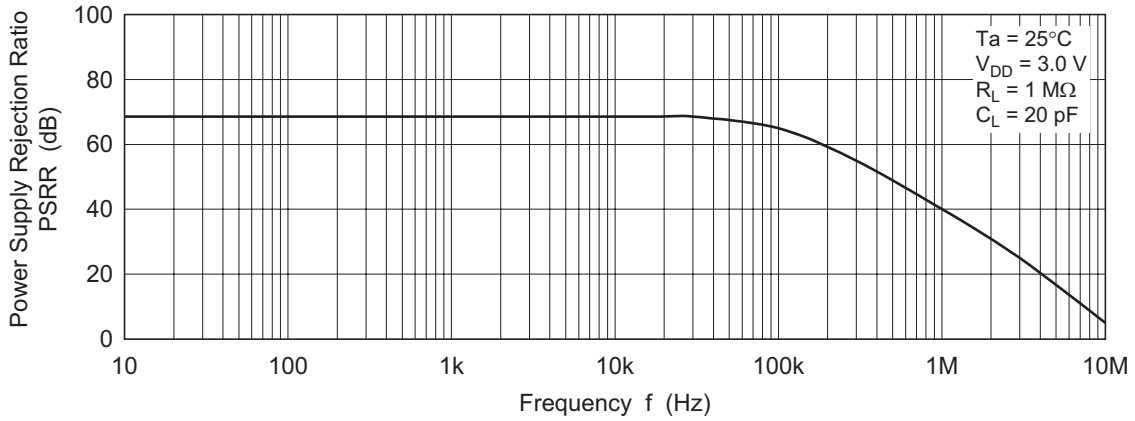


Figure 3-13. HA1630D06
Common Mode Rejection Ratio vs. Frequency

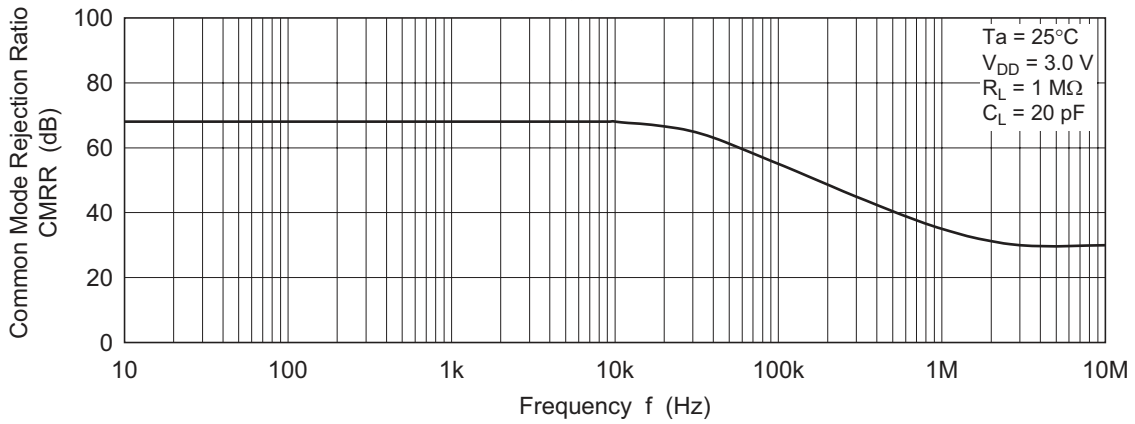
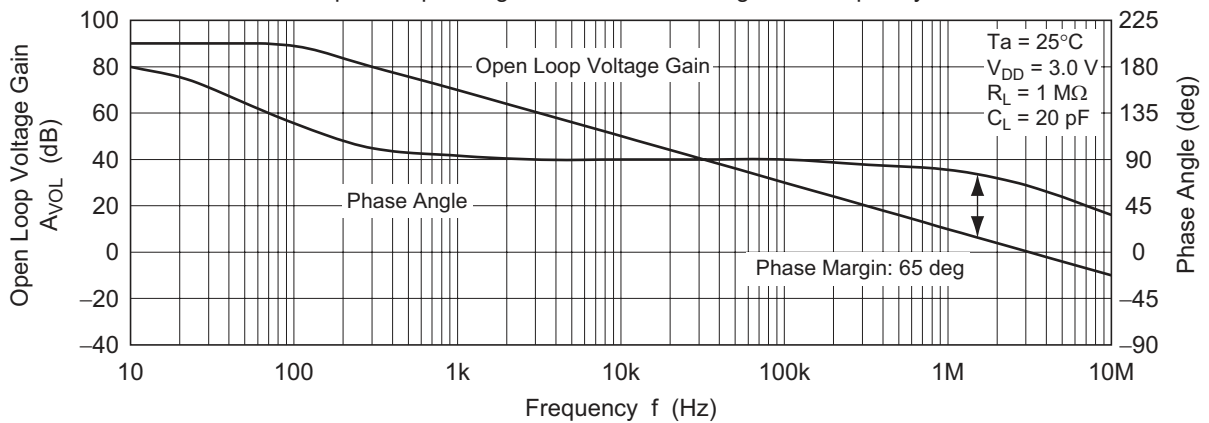


Figure 3-14. HA1630D06
Open Loop Voltage Gain and Phase Angle vs. Frequency



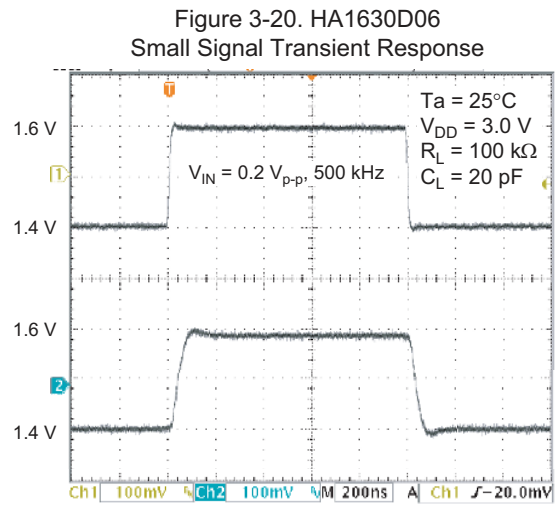
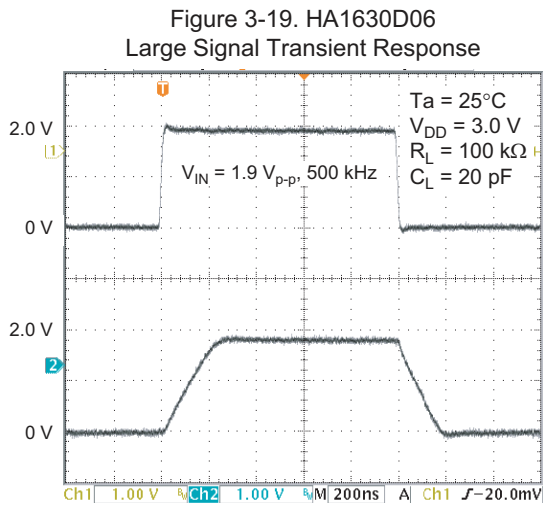
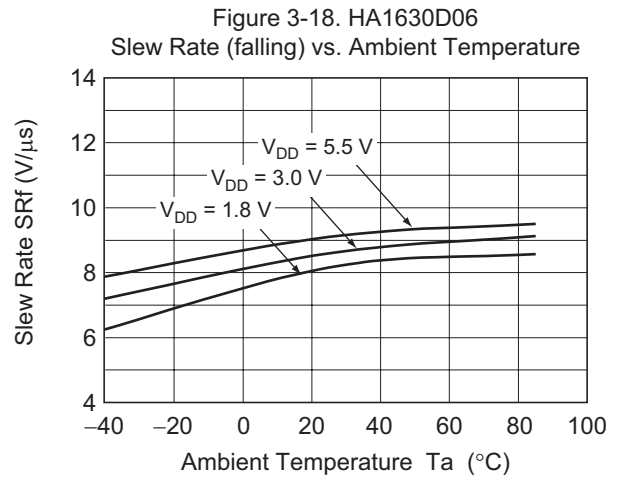
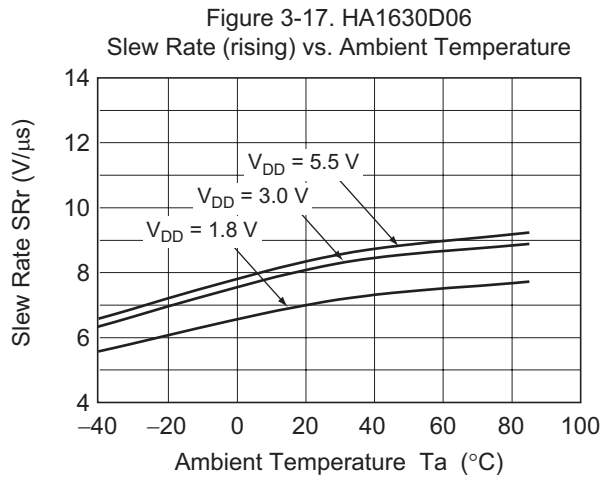
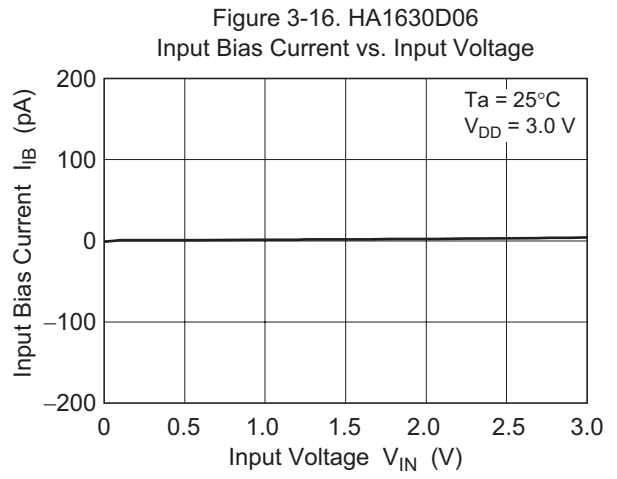
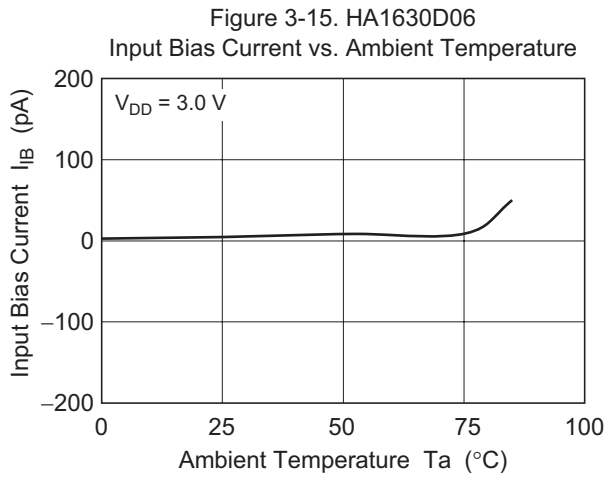


Figure 3-21. HA1630D06
Total Harmonic Distortion + Noise vs.
Output Voltage p-p

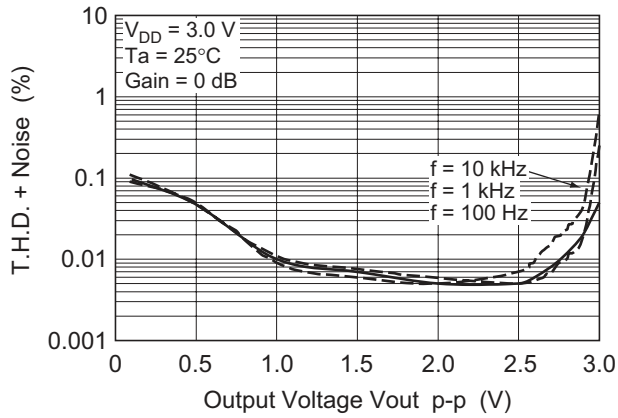


Figure 3-22. HA1630D06
Total Harmonic Distortion + Noise vs.
Output Voltage p-p

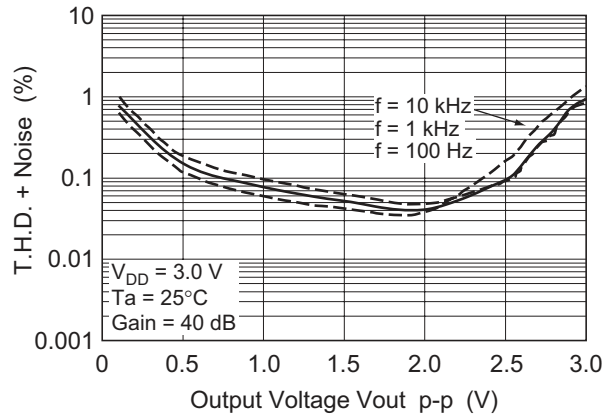


Figure 3-23. HA1630D06
Voltage Output p-p vs. Frequency

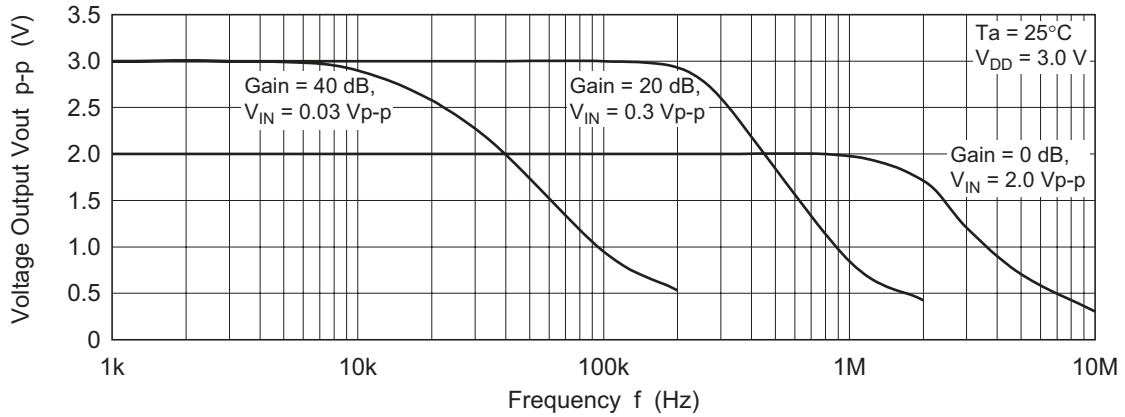


Figure 3-24. HA1630D06
Voltage Noise Density vs. Frequency

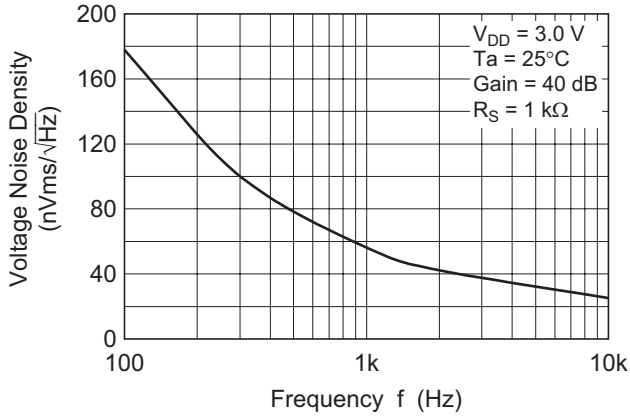
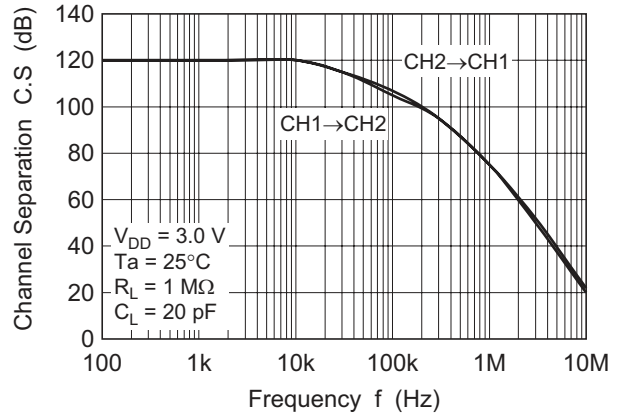
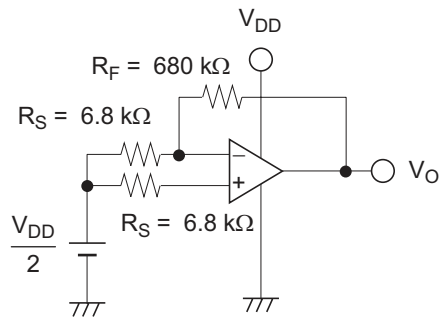


Figure 3-25. HA1630D06
Channel Separation vs. Frequency



Test Circuits

1. Power Supply Rejection Ratio, PSRR & Voltage Offset, V_{IO}



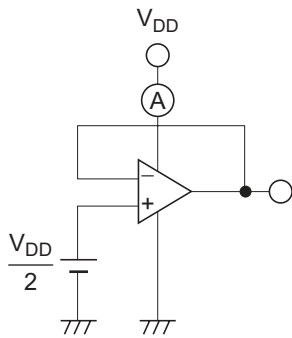
$$V_{IO} = \left(V_O - \frac{V_{DD}}{2} \right) \times \frac{R_S}{R_S + R_F}$$

PSRR

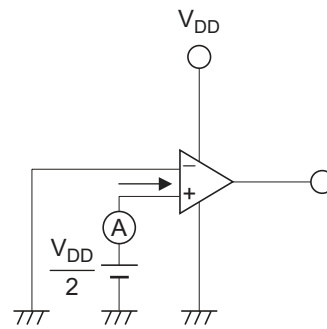
$$PSRR = -20 \log \left(\left| \frac{V_{DD1} - V_{DD2}}{V_{O1} - V_{O2}} \right| \times \frac{R_S}{R_S + R_F} \right)$$

Measure V_O corresponding to $V_{DD1} = 2.95 \text{ V}$ and $V_{DD2} = 3.05 \text{ V}$

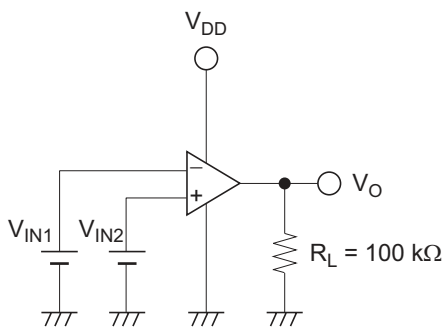
2. Supply Current, I_{DD}



3. Input Bias Current, I_B

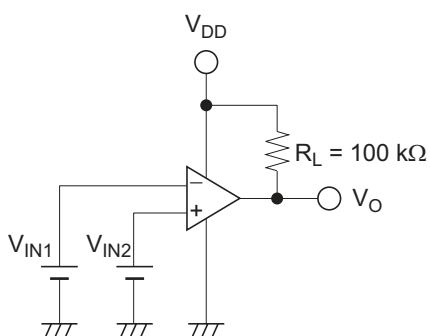


4. Output High Voltage, V_{OH}



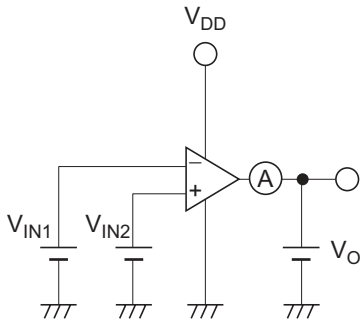
$$\begin{aligned} V_{OH} \\ V_{IN1} &= V_{DD} / 2 - 0.05 \text{ V} \\ V_{IN2} &= V_{DD} / 2 + 0.05 \text{ V} \end{aligned}$$

5. Output Low Voltage, V_{OL}



$$\begin{aligned} V_{OL} \\ V_{IN1} &= V_{DD} / 2 + 0.05 \text{ V} \\ V_{IN2} &= V_{DD} / 2 - 0.05 \text{ V} \end{aligned}$$

6. Output Source Current, $I_{OSOURCE}$ & Output Sink Current, I_{OSINK}



$I_{OSOURCE}$

$$V_O = V_{DD} - 0.5 \text{ V}$$

$$V_{IN1} = V_{DD} / 2 - 0.05 \text{ V}$$

$$V_{IN2} = V_{DD} / 2 + 0.05 \text{ V}$$

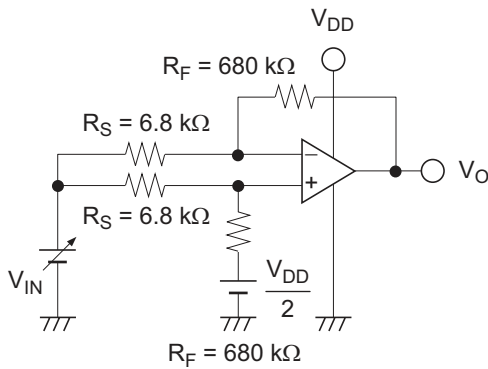
I_{OSINK}

$$V_O = + 0.5 \text{ V}$$

$$V_{IN1} = V_{DD} / 2 + 0.05 \text{ V}$$

$$V_{IN2} = V_{DD} / 2 - 0.05 \text{ V}$$

7. Common Mode Input Voltage, V_{CM} & Common Mode Rejection Ratio, CMRR

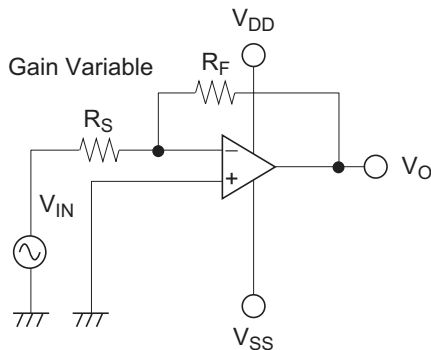


CMRR

$$CMRR = -20 \log \left(\left| \frac{V_{IN1} - V_{IN2}}{V_{O1} - V_{O2}} \right| \times \frac{R_S}{R_S + R_F} \right)$$

Measure V_O corresponding to $V_{IN1} = 1.45 \text{ V}$ and $V_{IN2} = 1.55 \text{ V}$

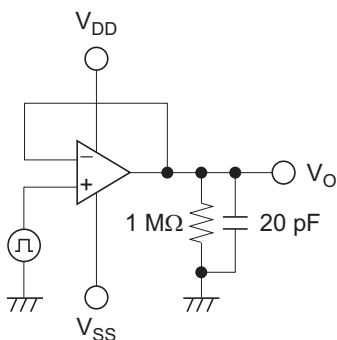
8. Total Harmonic Distortion, THD



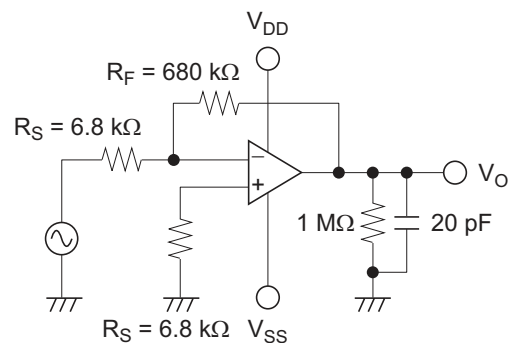
THD

Gain Variable
 $R_F / R_S = 20 \log (100 \text{ k}\Omega / 1 \text{ k}\Omega) = 40 \text{ dB}$
 $R_F / R_S = 20 \log (100 \text{ k}\Omega / 100 \text{ k}\Omega) = 0 \text{ dB}$
 freq = 100 Hz, 1 kHz, 10 kHz
 30 kHz LPF ON

9. Slew Rate, SR

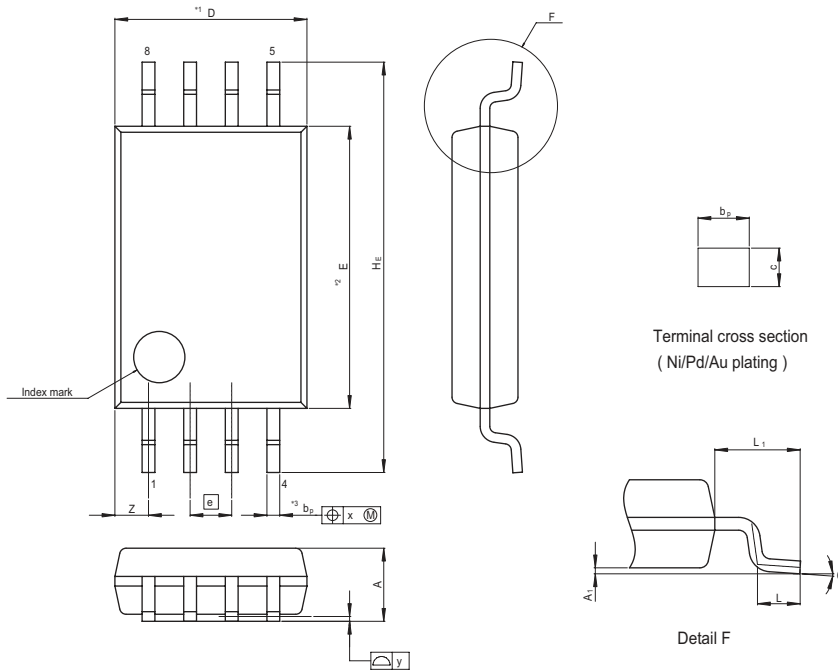


10. Gain, A_V & Phase, GBW



Package Dimensions

JEITA Package Code	RENEASAS Code	Previous Code	MASS[Typ.]
P-TSSOP8-4.4x3-0.65	PTSP0008JC-B	TTP-8DAV	0.034g

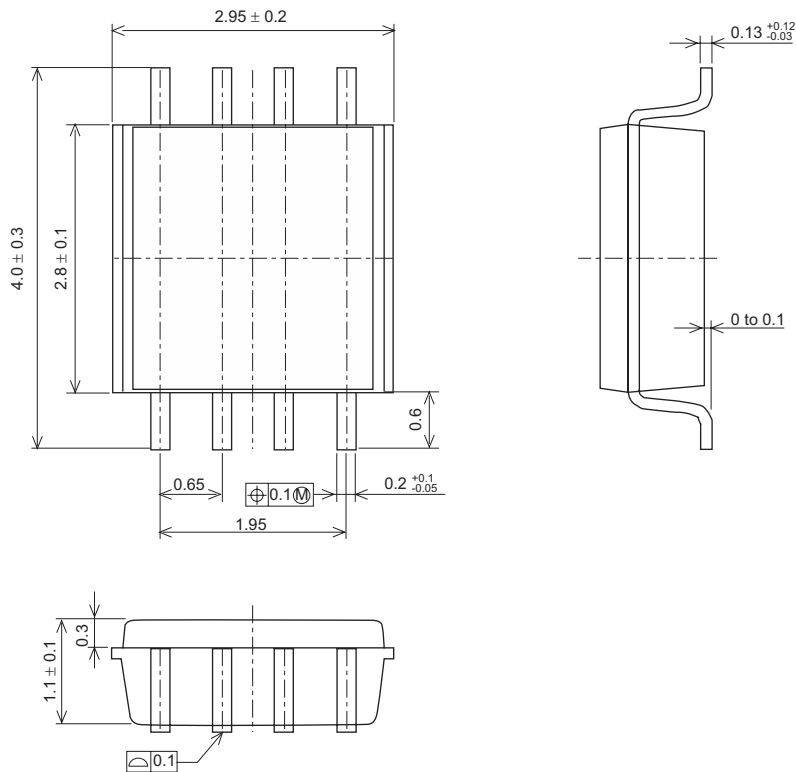


NOTE)
 1. DIMENSIONS*1 (Nom)*AND*2*
 DO NOT INCLUDE MOLD FLASH.
 2. DIMENSION*3*DOES NOT
 INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	3.00	3.30
E	—	4.40	—
A ₂	—	—	—
A ₁	0.03	0.07	0.10
A	—	—	1.10
b _P	0.15	0.20	0.25
b ₁	—	—	—
c	0.10	0.15	0.20
c ₁	—	—	—
θ	0°	—	8°
H _E	6.20	6.40	6.60
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z	—	—	0.805
L	0.40	0.50	0.60
L ₁	—	1.00	—

Package Name	JEITA Package Code	RENEASAS Code	Previous Code	MASS[Typ.]
MMPAK-8	P-LSOP8-2.8 x 2.95 - 0.65	PLSP0008JC-A	—	0.02 g

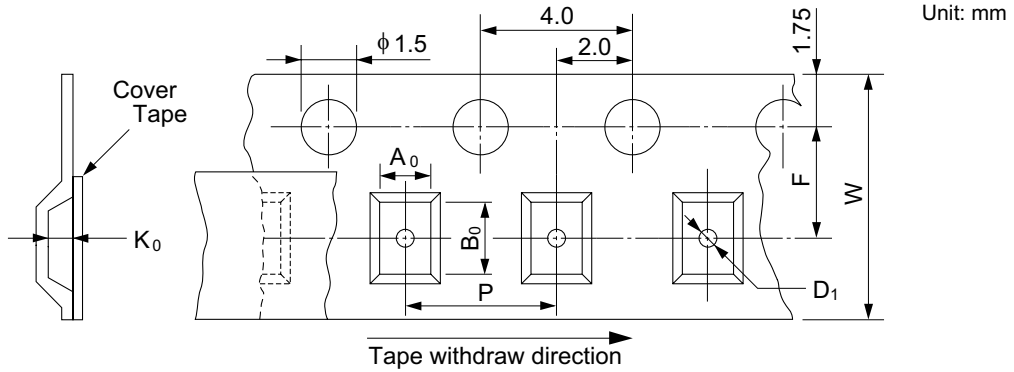
Unit: mm



Taping & Reel Specification

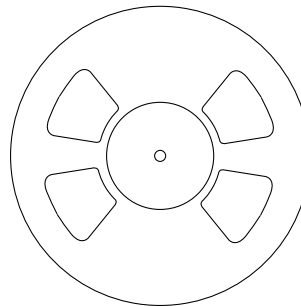
[Taping]

Package Code	W	P	Ao	Bo	Ko	E	F	D1	Maximum Storage No.
TSSOP-8	12	8	6.9	3.6	1.7	1.75	5.5	1.5	3,000 pcs/reel
MMPAK-8	12	4.0	3.15	4.35	—	—	5.5	1.05	3,000 pcs/reel



[Reel]

Package	Tape width	W1	W2	A
TSSOP-8	12	17.4	13.4	330
MMPAK-8	12	17.0	13.0	178

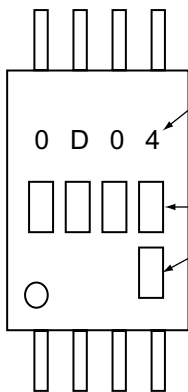


[Ordering Information]

Ordering Unit
3,000 pcs

Mark Indication

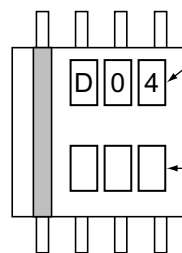
TSSOP-8



Product Name
 0D04: HA1630D04
 0D05: HA1630D05
 0D06: HA1630D06

Trace Code

MMPAK-8



Product Name
 D04: HA1630D04
 D05: HA1630D05
 D06: HA1630D06

Trace Code

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