

74VCX16601

Low Voltage 18-Bit Universal Bus Transceivers with 3.6V Tolerant Inputs and Outputs

General Description

The VCX16601 is an 18-bit universal bus transceiver which combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable (CLKENAB and CLKENBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is HIGH. When LEAB is LOW, the A data is latched if CLKAB is held at a HIGH-to-LOW logic level. If LEAB is LOW, the A bus data is stored in the latch/flip-flop on the LOW-to-HIGH transition of CLKAB. When OEAB is LOW, the outputs are active. When OEAB is HIGH, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, CLKBA and CLKENBA.

The VCX16601 is designed for low voltage (1.4V to 3.6V) V_{CC} applications with I/O capability up to 3.6V.

The VCX16601 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

- 1.4V to 3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- t_{PD} (A to B, B to A)
 - 2.9 ns max for 3.0V to 3.6V V_{CC}
- Power-down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- Static Drive (I_{OH}/I_{OL})
 - ± 24 mA @ 3.0V V_{CC}
- Uses proprietary noise/EMI reduction circuitry
- Latchup performance exceeds 300 mA
- ESD performance:
 - Human body model > 2000V
 - Machine model >200V
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA) (Preliminary)

Note 1: To ensure the high-impedance state during power up or power down, OE should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

Order Number	Package Number	Package Description
74VCX16601GX (Note 2)	BGA54A (Preliminary)	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [TAPE and REEL]
74VCX16601MTD (Note 3)	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

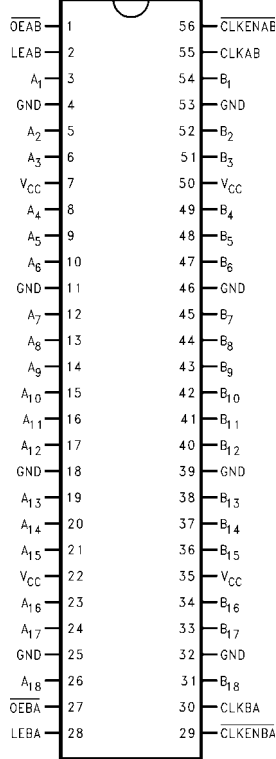
Note 2: BGA package available in Tape and Reel only.

Note 3: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

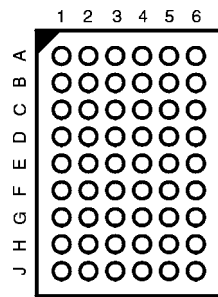
74VCX16601 Low Voltage 18-Bit Universal Bus Transceivers with 3.6V Tolerant Inputs and Outputs

Connection Diagrams

Pin Assignment for TSSOP



Pin Assignment for FBGA



(Top Thru View)

Pin Descriptions

Pin Names	Description
OEAB, OEBA	Output Enable Inputs (Active LOW)
LEAB, LEBA	Latch Enable Inputs
CLKAB, CLKBA	Clock Inputs
CLKENAB, CLKENBA	Clock Enable Inputs
A ₁ -A ₁₈	Side A Inputs or 3-STATE Outputs
B ₁ -B ₁₈	Side B Inputs or 3-STATE Outputs

FBGA Pin Assignments

	1	2	3	4	5	6
A	A ₂	A ₁	OEAB	CLKENAB	B ₁	B ₂
B	A ₄	A ₃	LEAB	CLKAB	B ₃	B ₄
C	A ₆	A ₅	V _{CC}	V _{CC}	B ₅	B ₆
D	A ₈	A ₇	GND	GND	B ₇	B ₈
E	A ₁₀	A ₉	GND	GND	B ₉	B ₁₀
F	A ₁₂	A ₁₁	GND	GND	B ₁₁	B ₁₂
G	A ₁₄	A ₁₃	V _{CC}	V _{CC}	B ₁₃	B ₁₄
H	A ₁₆	A ₁₅	OEBA	CLKBA	B ₁₅	B ₁₆
J	A ₁₇	A ₁₈	LEBA	CLKENBA	B ₁₈	B ₁₇

Truth Table

(Note 4)

Inputs					Outputs
CLKENAB	OEAB	LEAB	CLKAB	A _n	B _n
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B ₀ (Note 5)
H	L	L	X	X	B ₀ (Note 5)
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B ₀ (Note 5)
L	L	L	H	X	B ₀ (Note 6)

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial (HIGH or LOW, inputs may not float)

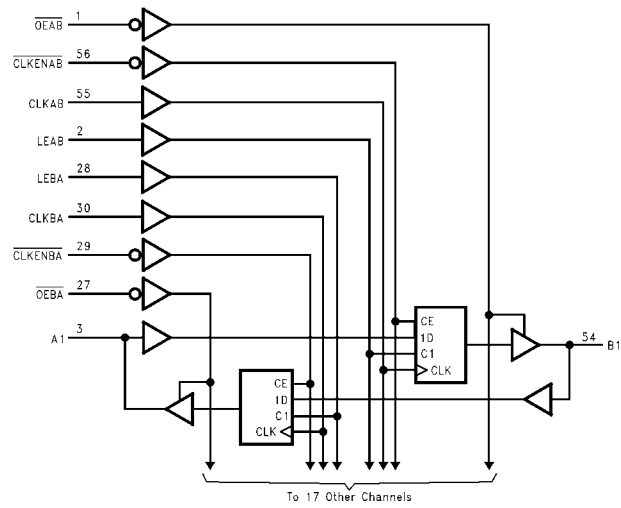
Z = High Impedance

Note 4: A-to-B data flow is shown; B-to-A flow is similar but uses OEBA, LEBA, CLKBA, and CLKENBA.

Note 5: Output level before the indicated steady-state input conditions were established.

Note 6: Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.

Logic Diagram



Absolute Maximum Ratings (Note 7)

Supply Voltage (V_{CC})	-0.5V to +4.6V
DC Input Voltage (V_I)	-0.5V to +4.6V
Output Voltage (V_O)	
Outputs 3-States	-0.5V to +4.6V
Outputs Active (Note 8)	-0.5 to $V_{CC} + 0.5V$
DC Input Diode Current (I_{IK}) $V_I < 0V$	-50 mA
DC Output Diode Current (I_{OK})	
$V_O < 0V$	-50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Current	
(I_{OH}/I_{OL})	± 50 mA
DC V_{CC} or Ground Current per	
Supply Pin (I_{CC} or Ground)	± 100 mA
Storage Temperature Range (T_{STG})	-65°C to +150°C

Recommended Operating Conditions (Note 9)

Power Supply	
Operating	1.4V to 3.6V
Input Voltage	-0.3V to 3.6V
Output Voltage (V_O)	
Output in Active States	0V to V_{CC}
Output in 3-STATE	0.0V to 3.6V
Output Current in I_{OH}/I_{OL}	
$V_{CC} = 3.0V$ to 3.6V	± 24 mA
$V_{CC} = 2.3V$ to 2.7V	± 18 mA
$V_{CC} = 1.65V$ to 2.3V	± 6 mA
$V_{CC} = 1.4V$ to 1.6V	± 2 mA
Free Air Operating Temperature (T_A)	-40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
$V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$	10 ns/V

Note 7: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The Recommended Operating Conditions tables will define the conditions for actual device operation.

Note 8: I_O Absolute Maximum Rating must be observed.

Note 9: Floating or unused pin (inputs or I/O's) must be held HIGH or LOW.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		2.7 - 3.6	2.0		V
			2.3 - 2.7	1.6		
			1.65 - 2.3	$0.65 \times V_{CC}$		
			1.4 - 1.6	$0.65 \times V_{CC}$		
V_{IL}	LOW Level Input Voltage		2.7 - 3.6		0.8	V
			2.3 - 2.7		0.7	
			1.65 - 2.3		$0.35 - V_{CC}$	
			1.4 - 1.6		$0.35 - V_{CC}$	
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	2.7 - 3.6	$V_{CC} - 0.2$		V
		$I_{OH} = -12 \text{ mA}$	2.7	2.2		
		$I_{OH} = -18 \text{ mA}$	3.0	2.4		
		$I_{OH} = -24 \text{ mA}$	3.0	2.2		
		$I_{OH} = -100 \mu A$	2.3 - 2.7	$V_{CC} - 0.2$		
		$I_{OH} = -6 \text{ mA}$	2.3	2.0		
		$I_{OH} = -12 \text{ mA}$	2.3	1.8		
		$I_{OH} = -18 \text{ mA}$	2.3	1.7		
		$I_{OH} = -100 \mu A$	1.65 - 2.3	$V_{CC} - 0.2$		
		$I_{OH} = -6 \text{ mA}$	1.65	1.25		
		$I_{OH} = -100 \mu A$	1.4 - 1.6	$V_{CC} - 0.2$		
		$I_{OH} = -2 \text{ mA}$	1.4	1.05		

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V _{CC} (V)	Min	Max	Units
V _{OL}	LOW Level Output Voltage	I _{OL} = 100 μA	2.7 - 3.6		0.2	V
		I _{OL} = 12 mA	2.7	0.4		
		I _{OL} = 18 mA	3.0	0.4		
		I _{OL} = 24 mA	3.0	0.55		
		I _{OL} = 100 μA	2.3 - 2.7	0.2		
		I _{OL} = 12 mA	2.3	0.4		
		I _{OL} = 18 mA	2.3	0.6		
		I _{OL} = 100 μA	1.65 - 2.3	0.2		
		I _{OL} = 6 mA	1.65	0.3		
		I _{OL} = 100 μA	1.4 - 1.6	0.2		
		I _{OL} = 2 mA	1.4	0.35		
I _I	Input Leakage Current	0V ≤ V _I ≤ 3.6V	2.7 - 3.6		±5.0	μA
I _{OZ}	3-STATE Output Leakage	0V ≤ V _O ≤ 3.6V V _I = V _{IH} or V _{IL}	1.4 - 3.6		±10.0	μA
I _{OFF}	Power Off Leakage Current	0V ≤ (V _I , V _O) ≤ 3.6V	0		10.0	μA
I _{CC}	Quiescent Supply Current	V _I = V _{CC} or GND	1.4 - 3.6		20.0	μA
		V _{CC} ≤ (V _I , V _O) ≤ 3.6V (Note 10)	1.4 - 3.6		±20.0	
ΔI _{CC}	Increase in I _{CC} per Input	V _{IH} = V _{CC} - 0.6V	2.7 - 3.6		750	μA

Note 10: Outputs disabled or 3-STATE only.

AC Electrical Characteristics (Note 11)							
Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40°C to +85°C		Units	Figure Number
				Min	Max		
t _{MAX}	Maximum Clock Frequency	C _L = 30 pF	3.3 ± 0.3	250		MHz	
			2.5 ± 0.2	200			
			1.8 ± 0.15	100			
		C _L = 15 pF	1.5 ± 0.1	80.0			
t _{PHL} t _{PLH}	Propagation Delay Bus-to-Bus	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	0.8	2.9	ns	Figures 1, 2
			2.5 ± 0.2	1.0	3.5		
			1.8 ± 0.15	1.5	7.0		
		C _L = 15 pF, R _L = 2kΩ	1.5 ± 0.1	1.0	14.0		Figures 7, 8
t _{PHL} t _{PLH}	Propagation Delay Clock-to-Bus	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	0.8	3.5	ns	Figures 1, 2
			2.5 ± 0.2	1.0	4.4		
			1.8 ± 0.15	1.5	8.8		
		C _L = 15 pF, R _L = 500Ω	1.5 ± 0.1	1.0	17.6		Figures 7, 8
t _{PHL} t _{PLH}	Propagation Delay LE-to-Bus	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	0.8	3.5	ns	Figures 1, 2
			2.5 ± 0.2	1.0	4.4		
			1.8 ± 0.15	1.5	8.8		
		C _L = 15 pF, R _L = 500Ω	1.5 ± 0.1	1.0	17.6		Figures 7, 8
t _{PZL} t _{PZH}	Output Enable Time	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	0.8	3.8	ns	Figures 1, 3, 4
			2.5 ± 0.2	1.0	4.9		
			1.8 ± 0.15	1.5	9.8		
		C _L = 15 pF, R _L = 2kΩ	1.5 ± 0.1	1.0	19.6		Figures 7, 9, 10
t _{PLZ} t _{PHZ}	Output Disable Time	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	0.8	3.7	ns	Figures 1, 3, 4
			2.5 ± 0.2	1.0	4.2		
			1.8 ± 0.15	1.5	7.6		
		C _L = 15 pF, R _L = 2kΩ	1.5 ± 0.1	1.0	15.2		Figures 7, 9, 10
t _S	Setup Time	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	1.5		ns	Figure 6
			2.5 ± 0.2	1.5			
			1.8 ± 0.15	2.5			
		C _L = 15 pF, R _L = 500Ω	1.5 ± 0.1	3.0			
t _H	Hold Time	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	1.0		ns	Figure 6
			2.5 ± 0.2	1.0			
			1.8 ± 0.15	1.0			
		C _L = 15 pF, R _L = 500Ω	1.5 ± 0.1	2.0			
t _W	Pulse Width	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	1.5		ns	Figure 5
			2.5 ± 0.2	1.5			
			1.8 ± 0.15	4.0			
		C _L = 15 pF, R _L = 500Ω	1.5 ± 0.1	4.0			
t _{OSHL} t _{OSLH}	Output to Output Skew (Note 12)	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3		0.5	ns	
			2.5 ± 0.2		0.5		
			1.8 ± 0.15		0.75		
		C _L = 15 pF, R _L = 2kΩ	1.5 ± 0.1		1.5		

Note 11: For C_L = 50pF, add approximately 300ps to the AC maximum specification.

Note 12: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics						
Symbol	Parameter	Conditions	V _{CC} (V)	T _A = +25°C	Units	
				Typical		
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8	0.25	V	
			2.5	0.6		
			3.3	0.8		
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8	-0.25	V	
			2.5	-0.6		
			3.3	-0.8		
V _{OHV}	Quiet Output Dynamic Valley V _{OH}	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8	1.5	V	
			2.5	1.9		
			3.3	2.2		
Capacitance						
Symbol	Parameter	Conditions	T _A = +25°C	Units		
C _{IN}	Input Capacitance	V _I = 0V or V _{CC} V _{CC} = 1.8V, 2.5V, or 3.3V	6.0	pF		
C _{IO}	Output Capacitance	V _I = 0V or V _{CC} , V _{CC} = 1.8V, 2.5V or 3.3V	7.0	pF		
C _{PD}	Power Dissipation Capacitance	V _I = 0V or V _{CC} , f = 10 MHz V _{CC} = 1.8V, 2.5V or 3.3V	20.0	pF		

AC Loading and Waveforms (V_{CC} 3.3V ± 0.3V to 1.8V ± 0.15V)

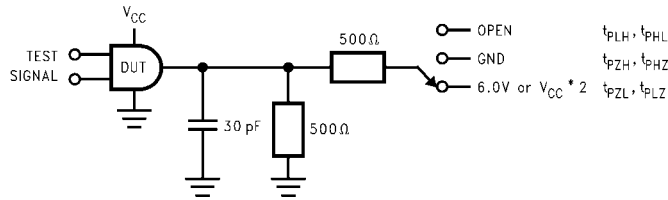


FIGURE 1. AC Test Circuit

TEST	SWITCH
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	6V at $V_{CC} = 3.3V \pm 0.3V$; $V_{CC} \times 2$ at $V_{CC} = 2.5V \pm 0.2V$; $1.8V \pm 0.15V$
t_{PZH} , t_{PHZ}	GND

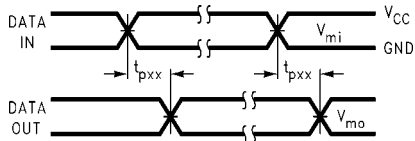


FIGURE 2. Waveform for Inverting and Non-inverting Functions

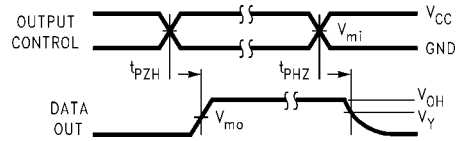


FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

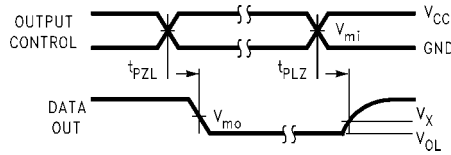


FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

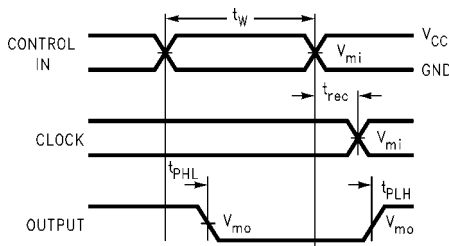


FIGURE 5. Propagation Delay, Pulse Width and t_{rec} Waveforms

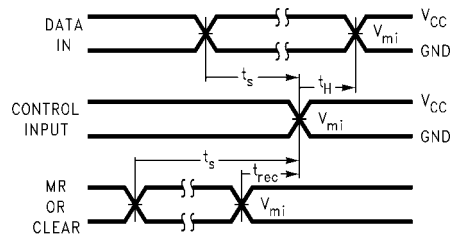
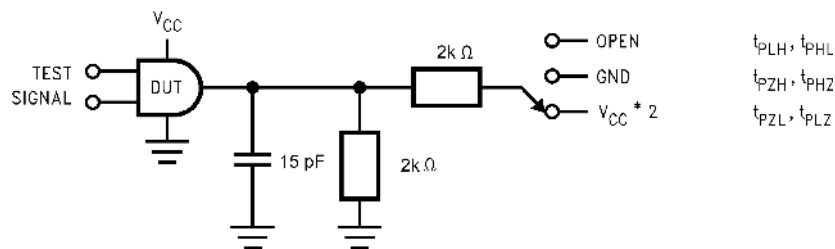


FIGURE 6. Setup Time, Hold Time and Recovery Time for Low Voltage Logic

Symbol	V_{CC}		
	3.3V ± 0.3V	2.5V ± 0.2V	1.8V ± 0.15V
V_{mi}	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_{mo}	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_X	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$	$V_{OL} + 0.15V$
V_Y	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$	$V_{OH} - 0.15V$

AC Loading and Waveforms ($V_{CC} 1.5V \pm 0.1V$)



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	$V_{CC} \times 2$ at $V_{CC} = 1.5 \pm 0.1V$
t_{PZH}, t_{PHZ}	GND

FIGURE 7. AC Test Circuit

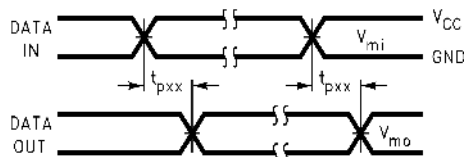


FIGURE 8. Waveform for Inverting and Non-inverting Functions

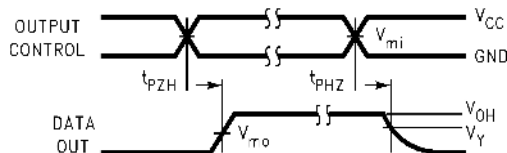


FIGURE 9. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

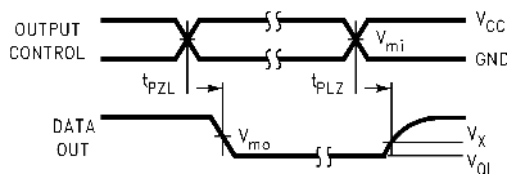
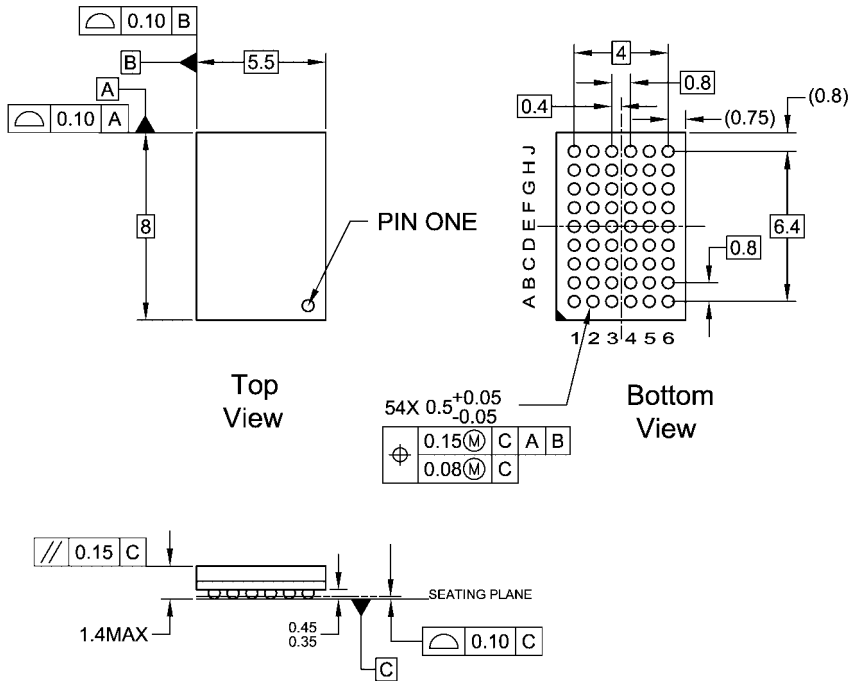


FIGURE 10. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

Symbol	V_{CC}
	$1.5V \pm 0.1V$
V_{mi}	$V_{CC}/2$
V_{mo}	$V_{CC}/2$
V_X	$V_{OL} + 0.1V$
V_Y	$V_{OH} - 0.1V$

Physical Dimensions inches (millimeters) unless otherwise noted



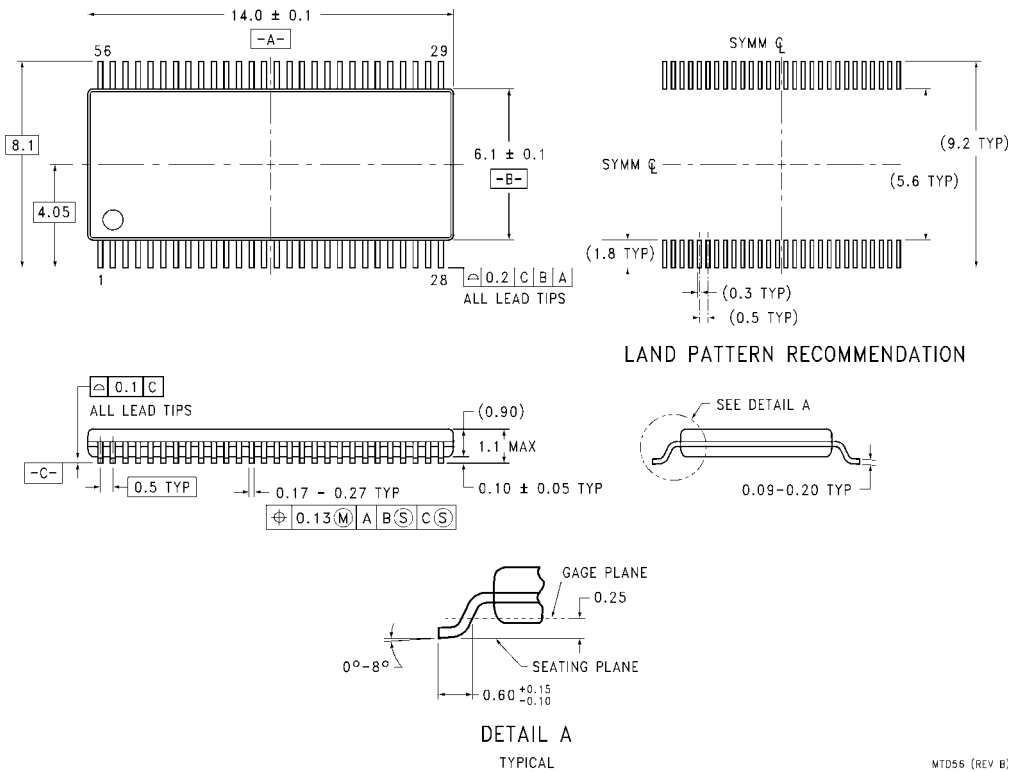
NOTES:

- A. THIS PACKAGE CONFORMS TO JEDEC M0-205
- B. ALL DIMENSIONS IN MILLIMETERS
- C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
- D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

**54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA54A
(Preliminary)**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56**

MTD56 (REV. B)

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