Low Voltage PLL Clock Driver

MPC93H51

**LOW VOLTAGE 3.3 V
PLL CLOCK GENERATOR**

**FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03**

**AC SUFFIX
32-LEAD LQFP PACKAGE
Pb-FREE PACKAGE
CASE 873A-03**

The MPC93H51 is a 3.3 V compatible, PLL based clock generator targeted for high performance clock distribution systems. With output frequencies of up to 240 MHz and a maximum output skew of 150 ps the MPC93H51 is an ideal solution for the most demanding clock tree designs. The device offers 9 low skew clock outputs. Each is configurable to support the clocking needs of the various high-performance microprocessors including the PowerQuicc II integrated communication microprocessor. The devices employs a fully differential PLL design to minimize cycle-to-cycle and long-term jitter.

Features

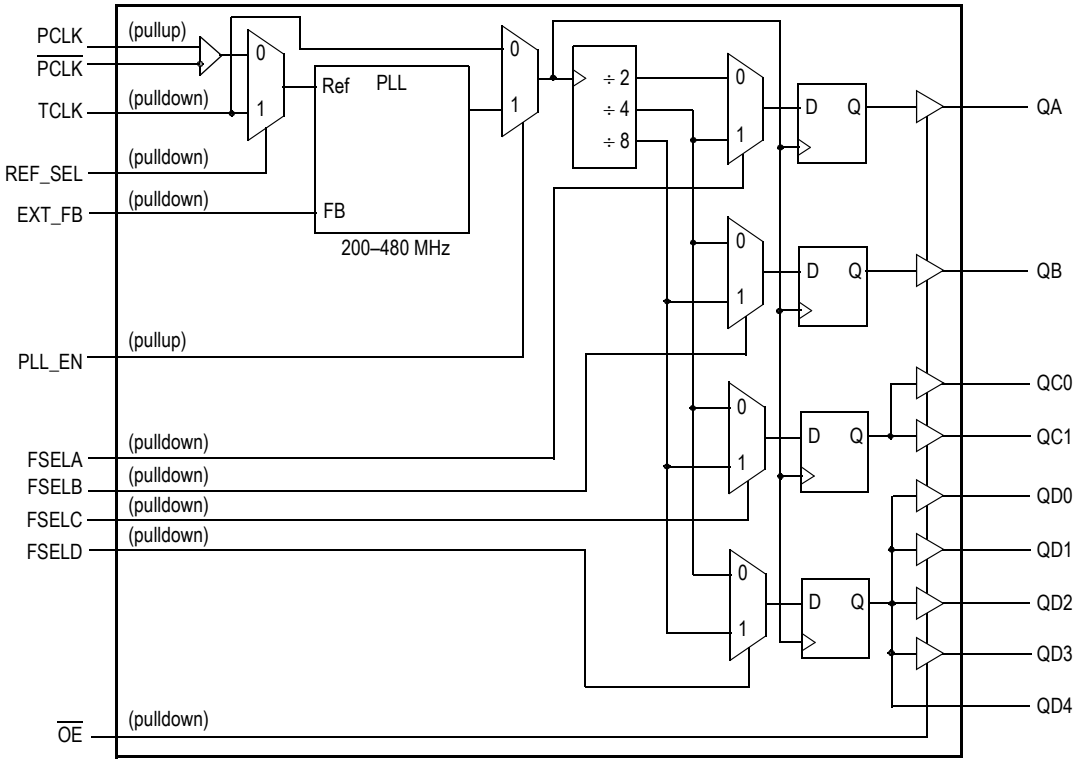
- 9 outputs LVCMOS PLL clock generator
- 25 – 240 MHz output frequency range
- Fully integrated PLL
- Compatible to various microprocessors such as PowerQuicc II
- Supports networking, telecommunications and computer applications
- Configurable outputs: divide-by-2, 4 and 8 of VCO frequency
- LVPECL and LVCMOS compatible inputs
- External feedback enables zero-delay configurations
- Output enable/disable and static test mode (PLL enable/disable)
- Low skew characteristics: maximum 150 ps output-to-output
- 32-lead LQFP package
- 32-lead Pb-free Package Available
- Ambient Temperature Range 0°C to +70°C
- Pin & Function Compatible with the MPC951

Functional Description

The MPC93H51 utilizes PLL technology to frequency and phase lock its outputs onto an input reference clock. Normal operation of the MPC93H51 requires a connection of one of the device outputs to the EXT_FB input to close the PLL feedback path. The reference clock frequency and the output divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range. With available output dividers of divide-by-4 and divide-by-8, the internal VCO of the MPC93H51 is running at either 4x or 8x of the reference clock frequency. The frequency of the QA, QB, QC and QD outputs is either one half, one fourth or one eighth of the selected VCO frequency and can be configured for each output bank using the FSELA, FSELB, FSELC and FSELD pins, respectively. The available output-to-input frequency ratios are 4:1, 2:1, 1:1, 1:2 and 1:4. The REF_SEL pin selects the differential LVPECL (PCLK and $\overline{\text{PCLK}}$) or the LVCMOS compatible reference input (TCLK). The MPC93H51 also provides a static test mode when the PLL enable pin (PLL_EN) is pulled to logic low state. In test mode, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The test mode is intended for system diagnostics, test and debug purpose. This test mode is fully static, and the minimum clock frequency specification does not apply. The outputs can be disabled by deasserting the $\overline{\text{OE}}$ pin (logic high state). In PLL mode, deasserting $\overline{\text{OE}}$ causes the PLL to loose lock due to no feedback signal presence at EXT_FB. Asserting OE will enable the outputs and close the phase locked loop, also enabling the PLL to recover to normal operation. The MPC93H51 is 3.3 V compatible and requires no external loop filter components. All inputs except PCLK and $\overline{\text{PCLK}}$ accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC93H51 outputs can drive one or two traces giving the devices an effective fanout of 1:18. The device is packaged in a 7x7 mm^2 32-lead LQFP package.

Application Information

The fully integrated PLL of the MPC93H51 allows the low skew outputs to lock onto a clock input and distribute it with essentially zero propagation delay to multiple components on the board. In zero-delay buffer mode, the PLL minimizes phase offset between the outputs and the reference signal.



The MPC93H51 requires an external RC filter for the analog power supply pin V_{CCA}. Please see APPLICATIONS INFORMATION for details.

Figure 1. MPC93H51 Logic Diagram

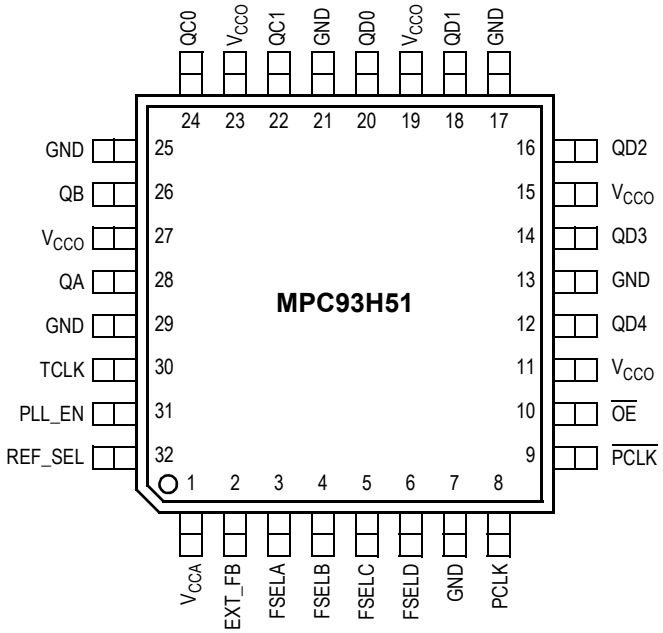


Figure 2. Pinout: 32-Lead LQFP Package Pinout (Top View)

Table 1. Pin Description

Pin	I/O	Type	Function
PCLK, $\overline{\text{PCLK}}$	Input	LVPECL	Differential clock reference Low voltage positive ECL input
TCLK	Input	LVCMOS	Single ended reference clock signal or test clock
EXT_FB	Input	LVCMOS	Feedback signal input, connect to a QA, QB, QC, QD output
REF_SEL	Input	LVCMOS	Selects input reference clock
FSELA	Input	LVCMOS	Output A divider selection
FSELB	Input	LVCMOS	Output B divider selection
FSELC	Input	LVCMOS	Outputs C divider selection
FSELD	Input	LVCMOS	Outputs D divider selection
OE	Input	LVCMOS	Output enable/disable
QA	Output	LVCMOS	Bank A clock output
QB	Output	LVCMOS	Bank B clock output
QC0, QC1	Output	LVCMOS	Bank C clock outputs
QD0 – QD4	Output	LVCMOS	Bank D clock outputs1.5
V_{CCA}	Supply	V_{CC}	Positive power supply for the PLL
V_{CC}	Supply	V_{CC}	Positive power supply for I/O and core
GND	Supply	Ground	Negative power supply

Table 2. Function Table

Control	Default	0	1
REF_SEL	0	Selects PCLK as reference clock	Selects TCLK as reference clock
PLL_EN	1	Test mode with PLL disabled. The input clock is directly routed to the output dividers	PLL enabled. The VCO output is routed to the output dividers
OE	0	Outputs enabled	Outputs disabled, PLL loop is open VCO is forced to its minimum frequency
FSELA	0	QA = VCO ÷ 2	QA = VCO ÷ 4
FSELB	0	QB = VCO ÷ 4	QB = VCO ÷ 8
FSELC	0	QC = VCO ÷ 4	QC = VCO ÷ 8
FSELD	0	QD = VCO ÷ 4	QD = VCO ÷ 8

Table 3. Absolute Maximum Ratings(1)

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.9	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC}+0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	150	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD (Machine Model)	200			V	
HBM	ESD (Human Body Model)	2000			V	
LU	Latch-Up	200			mA	
C_{PD}	Power Dissipation Capacitance		10		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 5. DC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = 0° to 70°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage				0.8	V	LVCMOS
V_{PP}	Peak-to-Peak Input Voltage	PCLK, $\overline{PCLK}$	250			mV	LVPECL
V_{CMR}(1)	Common Mode Range	PCLK, $\overline{PCLK}$	1.0		V_{CC}-0.6	V	LVPECL
V_{OH}	Output High Voltage		2.4			V	I_{OH} = –24 mA(2)
V_{OL}	Output Low Voltage				0.55 0.30	V V	I_{OL} = 24 mA I_{OL} = 12 mA
Z_{OUT}	Output Impedance			7 – 10		Ω	
I_{IN}	Input Leakage Current				±150	μA	V_{IN} = V_{CC} or GND
I_{CCA}	Maximum PLL Supply Current			6.0	12.0	mA	V_{CCA} Pin
I_{CCQ}	Maximum Quiescent Supply Current			10.0	14.0	mA	All V_{CC} Pins

1. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
2. The MPC93H51 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50 Ω series terminated transmission lines.

Table 6. AC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = 0° to 70°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency[2]	÷ 4 feedback	50		120	MHz	PLL_EN = 1
		÷ 8 feedback	25		60	MHz	PLL_EN = 1
		Static test mode	0		300	MHz	PLL_EN = 0
f_{VCO}	VCO Frequency		200		480	MHz	
f_{MAX}	Maximum Output Frequency[2]	÷ 2 output	100		240	MHz	
		÷ 4 output	50		120	MHz	
		÷ 8 output	25		60	MHz	
f_{refDC}	Reference Input Duty Cycle		25		75	%	
V_{PP}	Peak-to-Peak Input Voltage	PCLK, $\overline{PCLK}$	500		1000	mV	LVPECL
V_{CMR}[3]	Common Mode Range	PCLK, $\overline{PCLK}$	1.2		V_{CC}-0.9	V	LVPECL
t_r, t_f[4]	TCLK Input Rise/Fall Time				1.0	ns	0.8 to 2.0 V
$t_{(\varnothing)}$	Propagation Delay (static phase offset)						
		TCLK to EXT_FB	–150		+150	ps	PLL locked
		PCLK to EXT_FB	0		+250	ps	PLL locked
$t_{sk(o)}$	Output-to-Output Skew				300	ps	
DC	Output Duty Cycle	100 – 240 MHz	45	50	55	%	
		50 – 120 MHz	47.5	50	52.5	%	
		25 – 60 MHz	48.75	50	51.75	%	
t_r, t_f	Output Rise/Fall Time		0.1		1.0	ns	0.55 to 2.4 V
$t_{PLZ, HZ}$	Output Disable Time				7.0	ns	
$t_{PZL, ZH}$	Output Enable Time				6.0	ns	
BW	PLL closed loop bandwidth	÷ 2 feedback		9.0 – 20.0		MHz	-3 db point of
		÷ 4 feedback		3.0 – 9.5		MHz	PLL transfer
		÷ 8 feedback		1.2 – 2.1			characteristic
$t_{JIT(CC)}$	Cycle-to-cycle jitter Single Output Frequency Configuration	÷ 4 feedback			40	ps	RMS value
$t_{JIT(PER)}$	Period Jitter Single Output Frequency Configuration	÷ 4 feedback			25	ps	RMS value
$t_{JIT(\varnothing)}$	I/O Phase Jitter				30	ps	RMS value
t_{LOCK}	Maximum PLL Lock Time				5	ms	

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. The PLL will be unstable with a divide by 2 feedback ratio.
3. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} or V_{PP} impacts static phase offset $t_{(\varnothing)}$.
4. The MPC93H51 will operate with input rise/fall times up to 3.0 ns, but the AC characteristics, specifically $t_{(\varnothing)}$, can only be guaranteed if t_r/t_f are within the specified range.

APPLICATIONS INFORMATION

Programming the MPC93H51

The MPC93H51 clock driver outputs can be configured into several divider modes. In addition, the external feedback of the device allows for flexibility in establishing various input-to-output frequency relationships. The output divider of the four output groups allows the user to configure the outputs into 1:1, 2:1, 4:1 and 4:2:1 frequency ratios. The use of even dividers ensure that the output duty cycle is always 50%. Table 7 illustrates the various output configurations. The table describes the outputs using the input clock frequency CLK as a reference.

The output division settings establish the output relationship. In addition, it must be ensured that the VCO will be stable given the frequency of the outputs desired. The feedback frequency should be used to situate the VCO into a frequency range in which the PLL will be stable. The design of the PLL supports output frequencies from 25 MHz to 240 MHz while the VCO frequency range is specified from 200 MHz to 480 MHz and should not be exceeded for stable operation.

Table 7. Output Frequency Relationship(1) for an Example Configuration

Inputs				Outputs			
FSELA	FSELB	FSELC	FSELD	QA	QB	QC	QD
0	0	0	0	2 * CLK	CLK	CLK	CLK
0	0	0	1	2 * CLK	CLK	CLK	CLK ÷ 2
0	0	1	0	4 * CLK	2 * CLK	CLK	2* CLK
0	0	1	1	4 * CLK	2 * CLK	CLK	CLK
0	1	0	0	2 * CLK	CLK ÷ 2	CLK	CLK
0	1	0	1	2 * CLK	CLK ÷ 2	CLK	CLK ÷ 2
0	1	1	0	4 * CLK	CLK	CLK	2 * CLK
0	1	1	1	4 * CLK	CLK	CLK	CLK
1	0	0	0	CLK	CLK	CLK	CLK
1	0	0	1	CLK	CLK	CLK	CLK ÷ 2
1	0	1	0	2 * CLK	2 * CLK	CLK	2 * CLK
1	0	1	1	2 * CLK	2 * CLK	CLK	CLK
1	1	0	0	CLK	CLK ÷ 2	CLK	CLK
1	1	0	1	CLK	CLK ÷ 2	CLK	CLK ÷ 2
1	1	1	0	2 * CLK	CLK	CLK	2 * CLK
1	1	1	1	2 * CLK	CLK	CLK	CLK

1. Output frequency relationship with respect to input reference frequency CLK. QC1 is connected to EXT_FB.

Using the MPC93H51 in Zero-Delay Applications

Nested clock trees are typical applications for the MPC93H51. For these applications the MPC93H51 offers a differential LVPECL clock input pair as a PLL reference. This allows for the use of differential LVPECL primary clock distribution devices such as the Freescale Semiconductor MC100EP111 or MC10EP222, taking advantage of its superior low-skew performance. Clock trees using LVPECL for clock distribution and the MPC93H51 as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers.

The external feedback option of the MPC93H51 PLL allows for its use as a zero delay buffer. The PLL aligns the feedback clock output edge with the clock input reference edge and virtually eliminates the propagation delay through the device.

The remaining insertion delay (skew error) of the MPC93H51 in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset (SPO or $t_{(\varnothing)}$), I/O jitter ($t_{JIT(\varnothing)}$, phase or long-term jitter), feedback path delay and the output-to-output skew ($t_{SK(O)}$ relative to the feedback output.

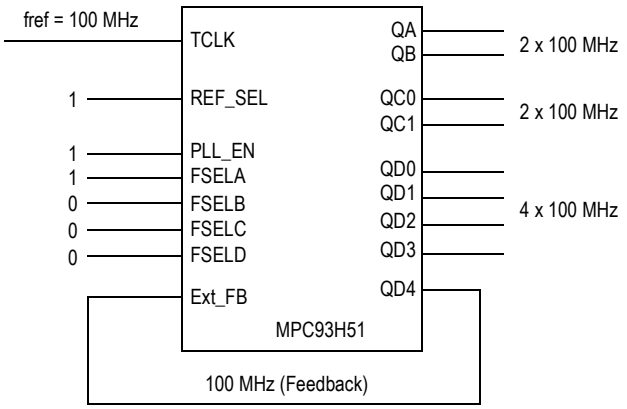


Figure 3. MPC93H51 Zero-Delay Configuration (Feedback of QD4)

Calculation of Part-to-Part Skew

The MPC93H51 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs (TCLK or PCLK) of two or more MPC93H51 are connected together, the maximum overall timing uncertainty from the common TCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \bullet CF$$

This maximum timing uncertainty consists of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

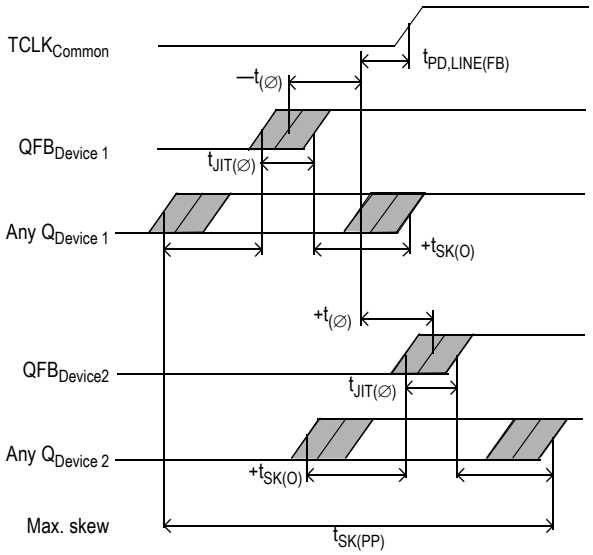


Figure 4. MPC93H51 Maximum Device-to-Device Skew

Due to the statistical nature of I/O jitter, a RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 8.

Table 8. Confidence Factor CF

CF	Probability of Clock Edge within the Distribution
± 1σ	0.68268948
± 2σ	0.95449988
± 3σ	0.99730007
± 4σ	0.99993663
± 5σ	0.99999943
± 6σ	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation, an I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from input to any output of –251 ps to 351 ps relative to TCLK (V_{CC} = 3.3 V and f_{VCO} = 400 MHz):

$$t_{SK(PP)} = [–50ps...150ps] + [–150ps...150ps] + [(17ps\ @\ –3)...(17ps\ @\ 3)] + t_{PD,\ LINE(FB)}$$

$$t_{SK(PP)} = [–251ps...351ps] + t_{PD,\ LINE(FB)}$$

Above equation uses the maximum I/O jitter number shown in the AC characteristic table for V_{CC} = 3.3 V (17 ps RMS). I/O jitter is frequency dependant with a maximum at the lowest VCO frequency (200 MHz for the MPC93H51). Applications using a higher VCO frequency exhibit less I/O jitter than the AC characteristic limit. The I/O jitter characteristics in Figure 5 can be used to derive a smaller I/O jitter number at the specific VCO frequency, resulting in tighter timing limits in zero-delay mode and for part-to-part skew $t_{SK(PP)}$.

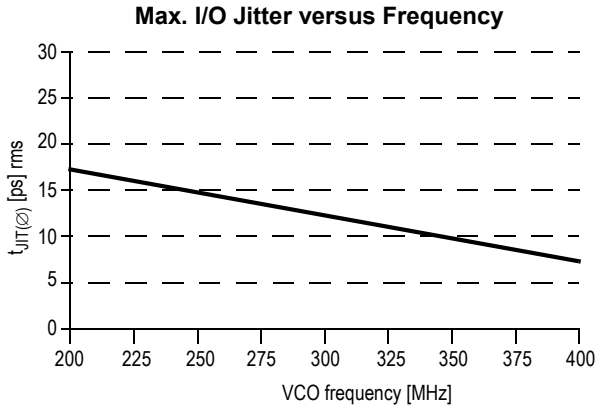


Figure 5. Maximum I/O Jitter (RSM) versus Frequency for V_{CC} = 3.3 V

Power Supply Filtering

The MPC93H51 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Noise on the V_{CCA} (PLL) power supply impacts the device characteristics, for instance I/O jitter. The MPC93H51 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CCA}) of the device.The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies, a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CCA} pin for the MPC93H51.

Figure 6 illustrates a typical power supply filter scheme. The MPC93H51 frequency and phase stability is most susceptible to noise with spectral content in the 100 kHz to 20 MHz range; therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F. From the data sheet the I_{CCA} current (the current sourced through the V_{CCA} pin) is typically 6 mA (12 mA maximum), assuming that a minimum of 3.0 V must be maintained on the V_{CCA} pin. The resistor R_F shown in Figure 6 must have a resistance of 5–15 Ω to meet the voltage drop criteria.

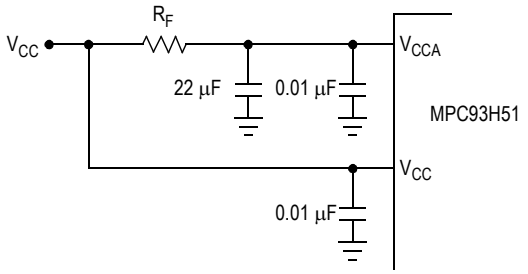


Figure 6. V_{CCA} Power Supply Filter

As the noise frequency crosses the series resonant point of an individual capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC93H51 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL), there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC93H51 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user, the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20 Ω, the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Freescale application note AN1091. In most high performance clock networks, point-to-point distribution of signals is the method of choice. In a point-to-point scheme, either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to $V_{CC} \div 2$.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC93H51 clock driver. For the series terminated case, however, there is no DC current draw; thus, the outputs can drive multiple series terminated lines. Figure 7 illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC93H51 clock driver is effectively doubled due to its capability to drive multiple lines.

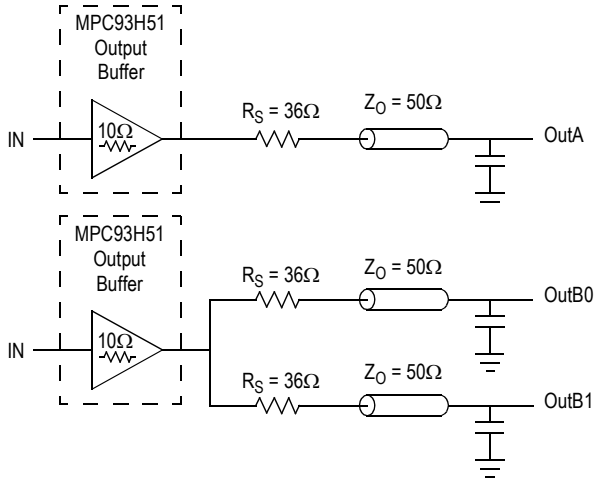


Figure 7. Single versus Dual Transmission Lines

The waveform plots in Figure 8 show the simulation results of an output driving a single line versus two lines. In both cases, the drive capability of the MPC93H51 output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations, a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC93H51. The output waveform in Figure 8 shows a step in the waveform. This step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36 Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 \div (R_S + R_0 + Z_0))$$
$$Z_0 = 50\ \Omega \parallel 50\ \Omega$$
$$R_S = 36\ \Omega \parallel 36\ \Omega$$
$$R_0 = 14\ \Omega$$
$$V_L = 3.0\ (25 \div (18 + 17 + 25)$$
$$= 1.31\ V$$

At the load end, the voltage will double to 2.6 V due to the near unity reflection coefficient. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0 ns).

Since this step is well above the threshold region it will not cause any false clock triggering; however, designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines, the situation in Figure 9 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

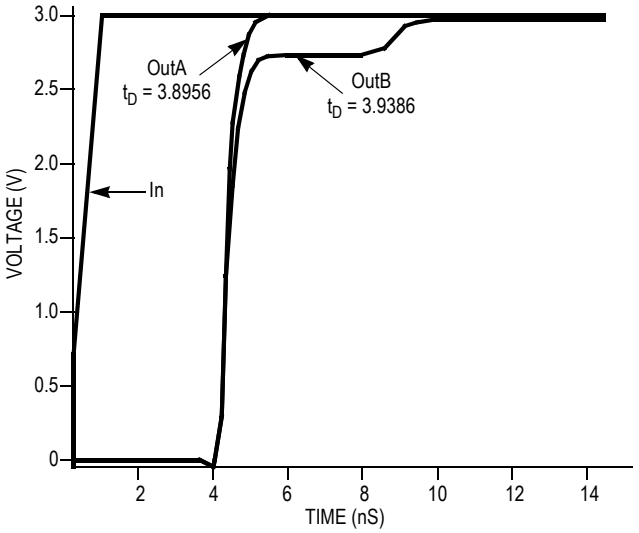
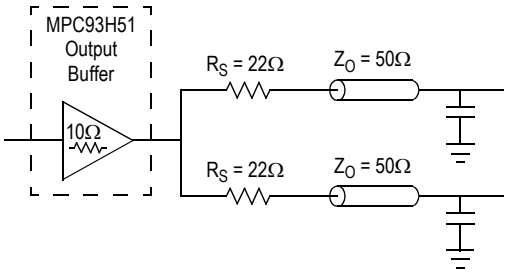


Figure 8. Single versus Dual Waveforms



14Ω + 22Ω || 22Ω = 50Ω || 50Ω
25Ω = 25Ω

Figure 9. Optimized Dual Line Termination

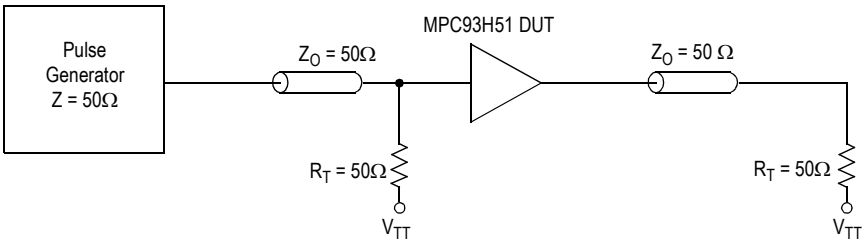


Figure 10. TCLK MPC93H51 AC Test Reference for V_{CC} = 3.3 V

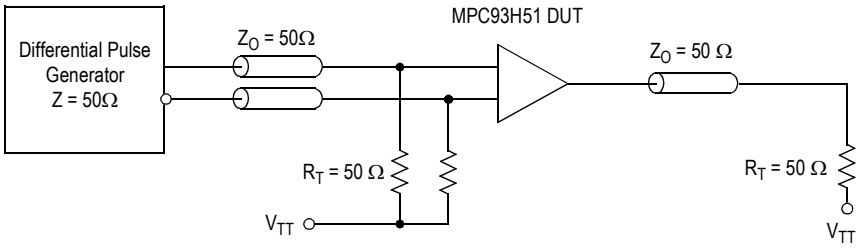


Figure 11. PCLK MPC93H51 AC Test Reference

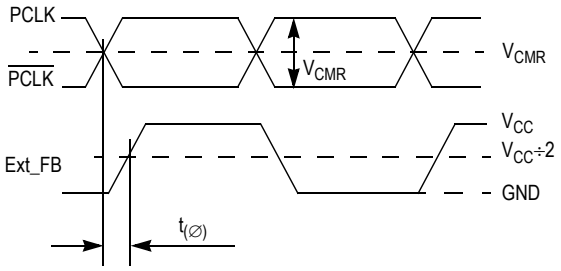


Figure 12. Propagation Delay (t_{PD}, status phase offset) Test Reference

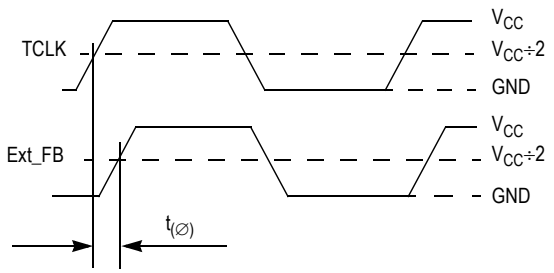
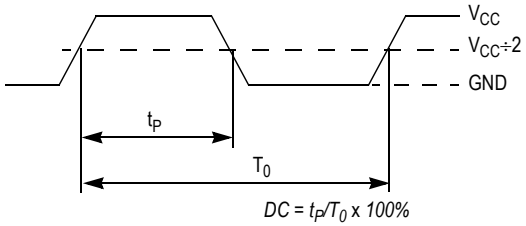
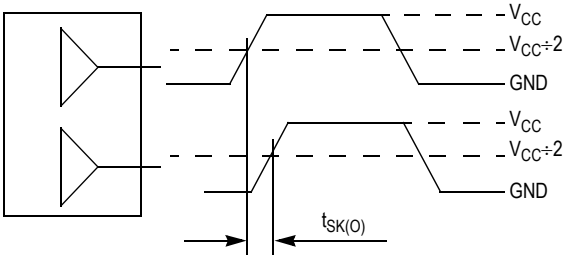


Figure 13. Propagation Delay (t_{PD}) Test Reference



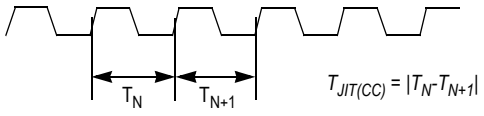
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 14. Output Duty Cycle (DC)



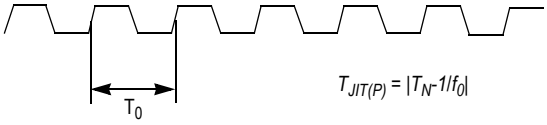
The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 15. Output-to-Output Skew $t_{SK(O)}$



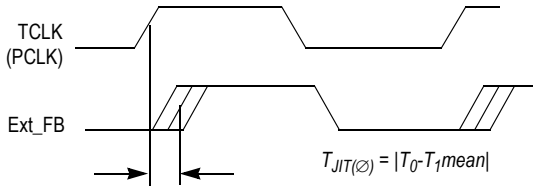
The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 16. Cycle-to-Cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 17. Period Jitter



The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 18. I/O Jitter

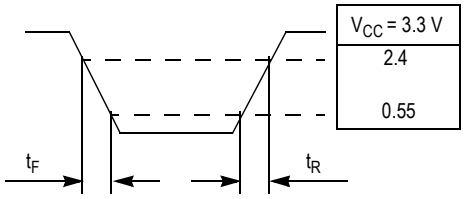
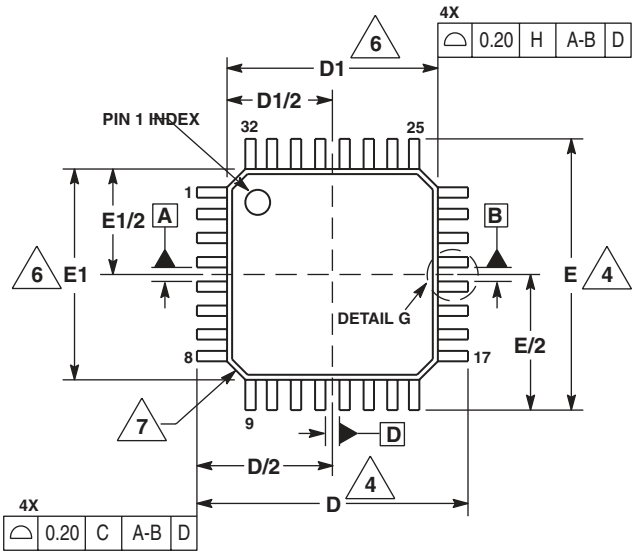
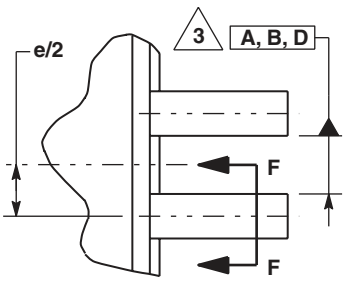


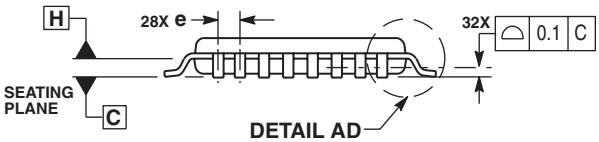
Figure 19. Transition Time Test Reference

PACKAGE DIMENSIONS

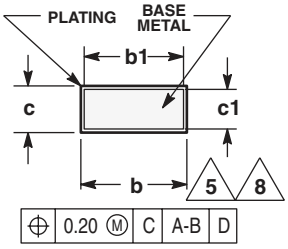




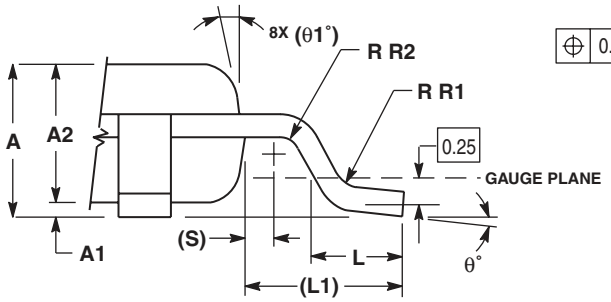
DETAIL G



DETAIL AD



SECTION F-F



DETAIL AD

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08-mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07-mm.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25-mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1-mm AND 0.25-mm FROM THE LEAD TIP.

	MILLIMETERS	
DIM	MIN	MAX
A	1.40	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.30	0.45
b1	0.30	0.40
c	0.09	0.20
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
e	0.80 BSC	
E	9.00 BSC	
E1	7.00 BSC	
L	0.50	0.70
L1	1.00 REF	
q	0°	7°
q1	12 REF	
R1	0.08	0.20
R2	0.08	---
S	0.20 REF	

CASE 873A-03
ISSUE B
32-LEAD LQFP PACKAGE

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