National Semiconductor

NMC2147H 4096 x 1-Bit Static RAM

General Description

The NMC2147H is a 4096-word by 1-bit static random access memory fabricated using N-channel silicon-gate technology. All internal circuits are fully static and therefore require no clocks or refreshing for operation. The data is read out nondestructively and has the same polarity as the input data.

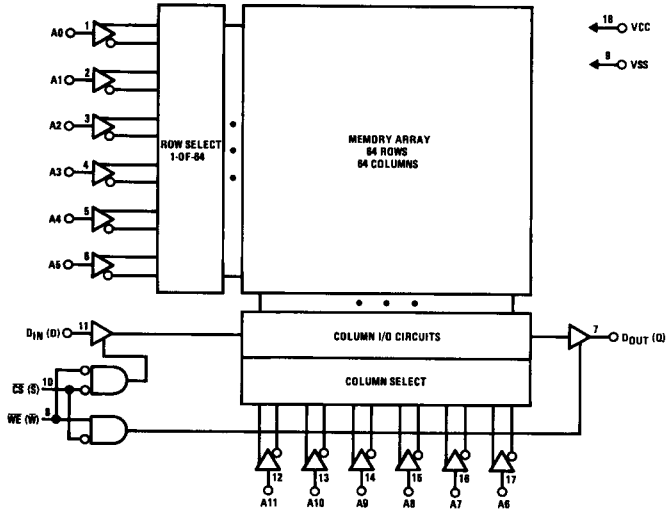
The separate chip select input automatically switches the part to its low power standby mode when it goes high.

The output is held in a high impedance state during write to simplify common I/O applications.

Features

- All inputs and outputs directly TTL compatible
- Static operation—no clocks or refreshing required
- Automatic power-down
- High-speed—down to 35 ns access time
- TRI-STATE® output for bus interface
- Separate Data In and Data Out pins
- Single +5V supply
- Standard 18-pin dual-in-line package
- Available in MIL-STD-883 class B screening

Block Diagram*



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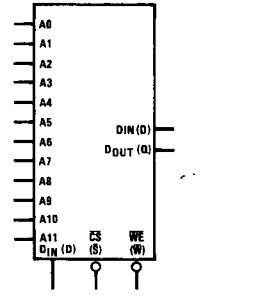
Logic Symbol*



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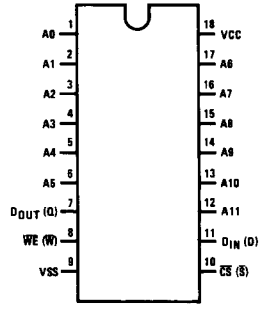
Connection Diagram*

Dual-In-Line Package



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Top View

Pin Names*

A0–A11	Address Inputs
$\overline{WE}$ ($\overline{W}$)	Write Enable
$\overline{CS}$ ($\overline{S}$)	Chip Select
D_{IN} (D)	Data In
D_{OUT} (Q)	Data Out
V_{CC}	Power (5V)
V_{SS}	Ground

Order Number NMC2147HJ-1, NMC2147HJ-2, NMC2147HJ-3, or NMC2147HJ-3L
See NS Package Number J18A

*The symbols in parentheses are proposed industry standard.

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage on Any Pin Relative to VSS	−3.5V to +7V
Storage Temperature Range	−65°C to +150°C
Power Dissipation	1.2W
DC Output Current	20 mA
Bias Temperature Range	−65°C to +135°C
Lead Temperature (Soldering, 10 sec.)	300°C

Truth Table*

$\overline{CS}$ (S)	$\overline{WE}$ ($\overline{W}$)	DIN (D)	DOUT (Q)	Mode	Power
H	X	X	Hi-Z	Not Selected	Standby
L	L	H	Hi-Z	Write 1	Active
L	L	L	Hi-Z	Write 0	Active
L	H	X	DOUT	Read	Active

DC Electrical Characteristics TA = 0°C to +70°C, VCC = 5V ± 10% (Notes 1 and 2)

Symbol	Parameter	Conditions	NMC2147H-3L		NMC2147H-1 NMC2147H-2 NMC2147H-3		NMC2147H		Units
			Min	Max	Min	Max	Min	Max	
|ILI|	Input Load Current (All Input Pins)	VIN = 0V to 5.5V, VCC = Max		10		10		10	μA
|ILO|	Output Leakage Current	$\overline{CS}$ = VIH, VOUT = GND to 4.5V, VCC = Max		50		50		50	μA
VIL	Input Low Voltage		−3.0	0.8	−3.0	0.8	−3.0	0.8	V
VIH	Input High Voltage		2.0	6.0	2.0	6.0	2.0	6.0	V
VOL	Output Low Voltage	IOL = 8.0 mA		0.4		0.4		0.4	V
VOH	Output High Voltage	IOH = −4.0 mA	2.4		2.4		2.4		V
ICC	Power Supply Current	VIN = 5.5V, TA = 0°C, Output Open		125		180		160	mA
ISB	Standby Current	VCC = Min to Max, $\overline{CS}$ = VIH		20		30		20	mA
IPO	Peak Power-On Current	VCC = VSS to VCC Min, $\overline{CS}$ = Lower of VCC or VIH Min		30		40		30	mA

Capacitance TA = 25°C, f = 1 MHz (Note 3)

Symbol	Parameter	Conditions	Min	Max	Units
CIN	Address/Control Capacitance	VIN = 0V		5	pF
COUT	Output Capacitance	VOUT = 0V		6	pF

Note 1: The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.

Note 2: These circuits require 500 μs time delay after VCC reaches the specified minimum limit to ensure proper orientation after power-on. This allows the internally generated substrate bias to reach its functional level.

Note 3: This parameter is guaranteed by periodic testing.

AC Test Conditions

Input Test Levels	GND to 3.0V
Input Rise and Fall Times	5 ns
Input Timing Reference Level	1.5V
Output Timing Reference Level (H-1)	1.5V
Output Timing Reference Level (H-2, H-3, H-3L)	0.8V and 2.0V
Output Load	See *Figure 1*

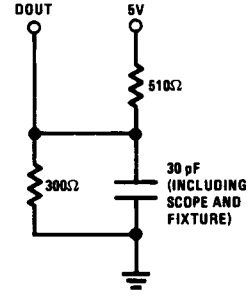

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FIGURE 1. Output Load

*Symbols in parentheses are proposed industry standard.

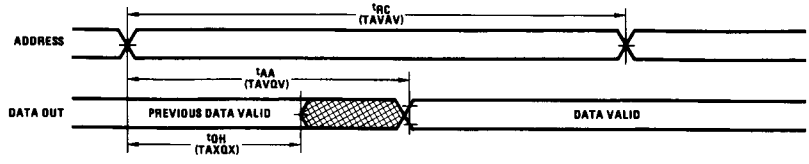
Read Cycle AC Electrical Characteristics TA = 0°C to 70°C, VCC = 5V ±10% (Note 1)

Symbol		Parameter	NMC2147H-1		NMC2147H-2		NMC2147H-3 NMC2147H-3L		NMC2147H		Units
Alternate	Standard		Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	TAVAV	Read Cycle Time	35		45		55		70		ns
t_{AA}	TAVQV	Address Access Time		35		45		55		70	ns
t_{ACS}	TSLQV	Chip Select Access Time (Notes 4)		35		45		55		70	ns
t_{LZ}	TSLQX	Chip Select to Output Active (Note 5)	5		5		10		10		ns
t_{HZ}	TSHQZ	Chip Deselect to Output TRI-STATE (Note 5)	0	30	0	30	0	30	0	30	ns
t_{OH}	TAXQX	Output Hold from Address Change	5		5		5		5		ns
t_{PU}	TSLIH	Chip Select to Power-Up	0		0		0		0		ns
t_{PD}	TSHIL	Chip Deselect to Power-Down		20		20		20		30	ns

Max Access/Current	NMC2147H-1	NMC2147H-2	NMC2147H-3	NMC2147H-3L	NMC2147H
Access (TAVQV—ns)	35	45	55	55	70
Active Current (ICC—mA)	180	180	180	125	160
Standby Current (ISB—mA)	30	30	30	20	20

Read Cycle Waveforms*

Read Cycle 1 (Continuous Selection $\overline{CS}$ = VIL, $\overline{WE}$ = VIH)



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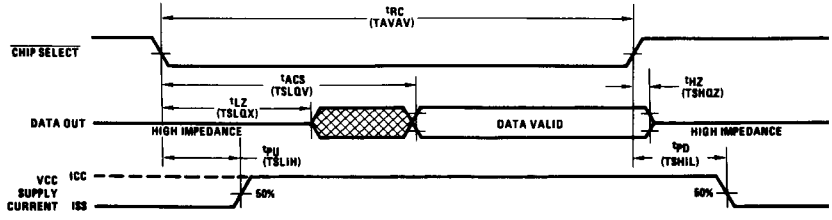
Read Cycle 2 (Chip Select Switched, $\overline{WE}$ = VIH) (Note 4)



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Note 4: Addresses must be valid coincident with or prior to the chip select transition from high to low.

Note 5: Measured ±50 mV from steady state voltage. This parameter is sampled and not 100% tested.

*The symbols in parentheses are proposed industry standard.

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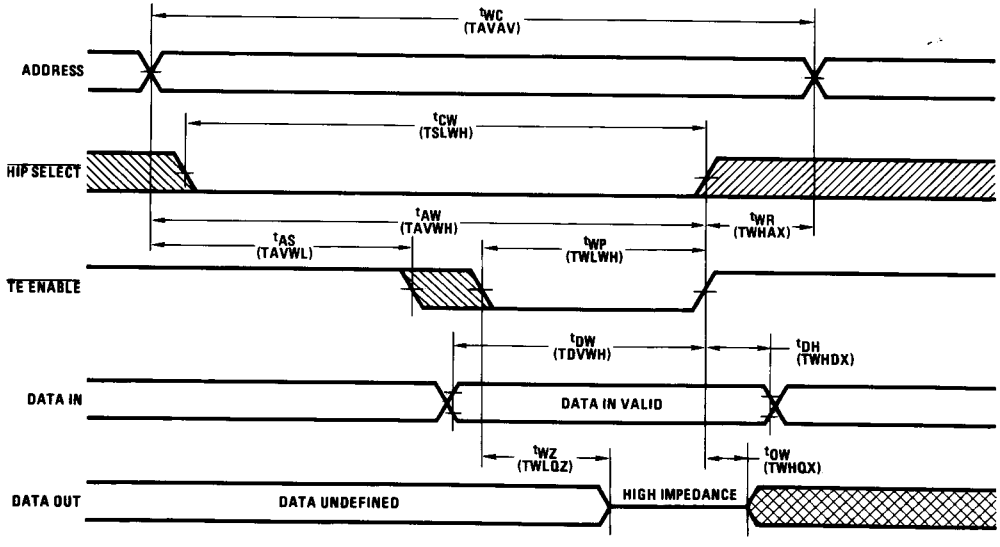
Write Cycle AC Electrical Characteristics TA = 0°C to 70°C, VCC = 5V ±10% (Note 1)

Symbol		Parameter	NMC2147H-1		NMC2147H-2		NMC2147H-3 NMC2147H-3L		NMC2147H		Units
Alternate	Standard		Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	TAVAV	Write Cycle Time	35		45		55		70		ns
t_{CW}	TSLWH	Chip Select to End of Write	35		45		45		55		ns
t_{AW}	TAVWH	Address Valid to End of Write	35		45		45		55		ns
t_{AS}	TAVSL TAVWL	Address Set-Up Time	0		0		0		0		ns
t_{WP}	TWLWH	Write Pulse Width	20		25		25		40		ns
t_{WR}	TWHAX	Write Recovery Time	0		0		10		15		ns
t_{DW}	TDVWH	Data Set-Up Time	20		25		25		30		ns
t_{DH}	TWHDX	Data Hold Time	10		10		10		10		ns
t_{WZ}	TWLQZ	Write Enable to Output TRI-STATE (Note 5)	0	20	0	25	0	25	0	35	ns
t_{OW}	TWHQX	Output Active from End of Write (Note 5)	0		0		0		0		ns

Write Cycle Waveforms* (Note 6)

Write Cycle 1 (Write Enable Limited)



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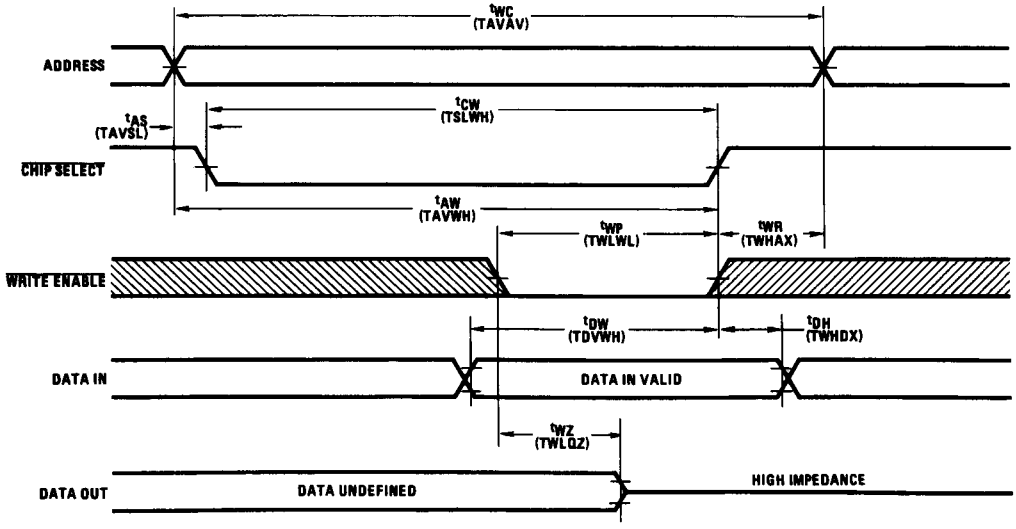
Write Cycle Waveforms* (Note 6)

Write Cycle 2 (Chip Select Limited)



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Note 6: The output remains TRI-STATE if the $\overline{CS}$ and $\overline{WE}$ go high simultaneously. $\overline{WE}$ or $\overline{CS}$ or both must be high during the address transitions to prevent an erroneous write.

*The symbols in parentheses are proposed industry standard.