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# NCP5215

# Dual Synchronous Buck Controller for Notebook Power System

The NCP5215, a high−efficiency and fast−transient−response dual−channel buck controller, provides a multifunctional power solution for notebook power system. 180° interleaved operation function between the two channels has capabilities of reducing the common input capacitor requirement and improving noise immunity. Adaptive−Voltage−Positioning (AVP) control reduces the requirement of output filter capacitors. Programmable power−saving operation ensures high efficiency over entire load range. Input feedforward voltage−mode control is employed to deal with wide input voltage range. Transient−Response−Enhancement (TRE) control for the both channels enables fast transient response.

### Features

- Wide Input Voltage Range: 4.5 V to 24 V
- Adjustable Output Voltage Range: 0.8 V to 3.0 V
- Selectable Nominal Fixed Switching Frequency: 200 kHz, 300 kHz, and 400 kHz
- 180° Interleaved Operation Function between the Two Channels
- Programmable Adaptive−Voltage−Positioning (AVP) Operation
- Programmable Transient−Response−Enhancement (TRE) Control
- Power Saving Operation under Light Load Condition
- Input Feedforward Voltage Mode Control
- Resistive or Inductor's DCR Current Sensing
- 1% Internal 0.8 V Reference
- External Soft−Start Operation
- Output Discharge and Soft−Stop
- Built−in Gate Drivers
- Input Supplies Undervoltage Lockout
- Output Overvoltage and Undervoltage Protections
- Accurate Overcurrent Protection
- Thermal Shutdown Protection
- QFN40 Package
- This is a Pb−Free Device

### Typical Applications

- Notebook Computers
- CPU Chipset Power Supplies

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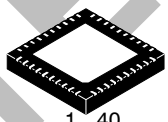
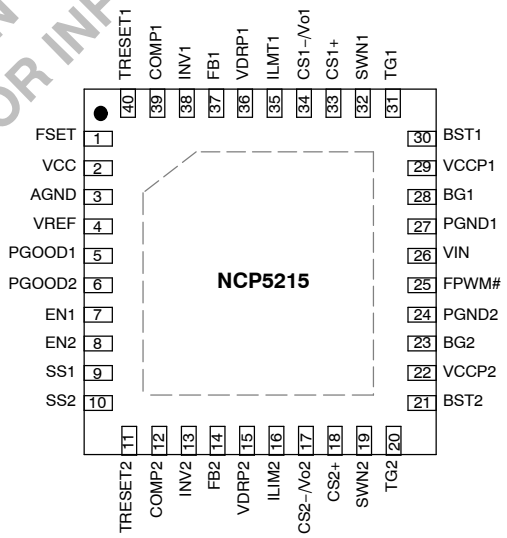



**QFN40**
**MN SUFFIX**
**CASE 488AR**

**MARKING DIAGRAM**


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

**PIN CONNECTIONS**




(Top View)

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NCP5215MNR2G | QFN40 (Pb−Free) | 2500/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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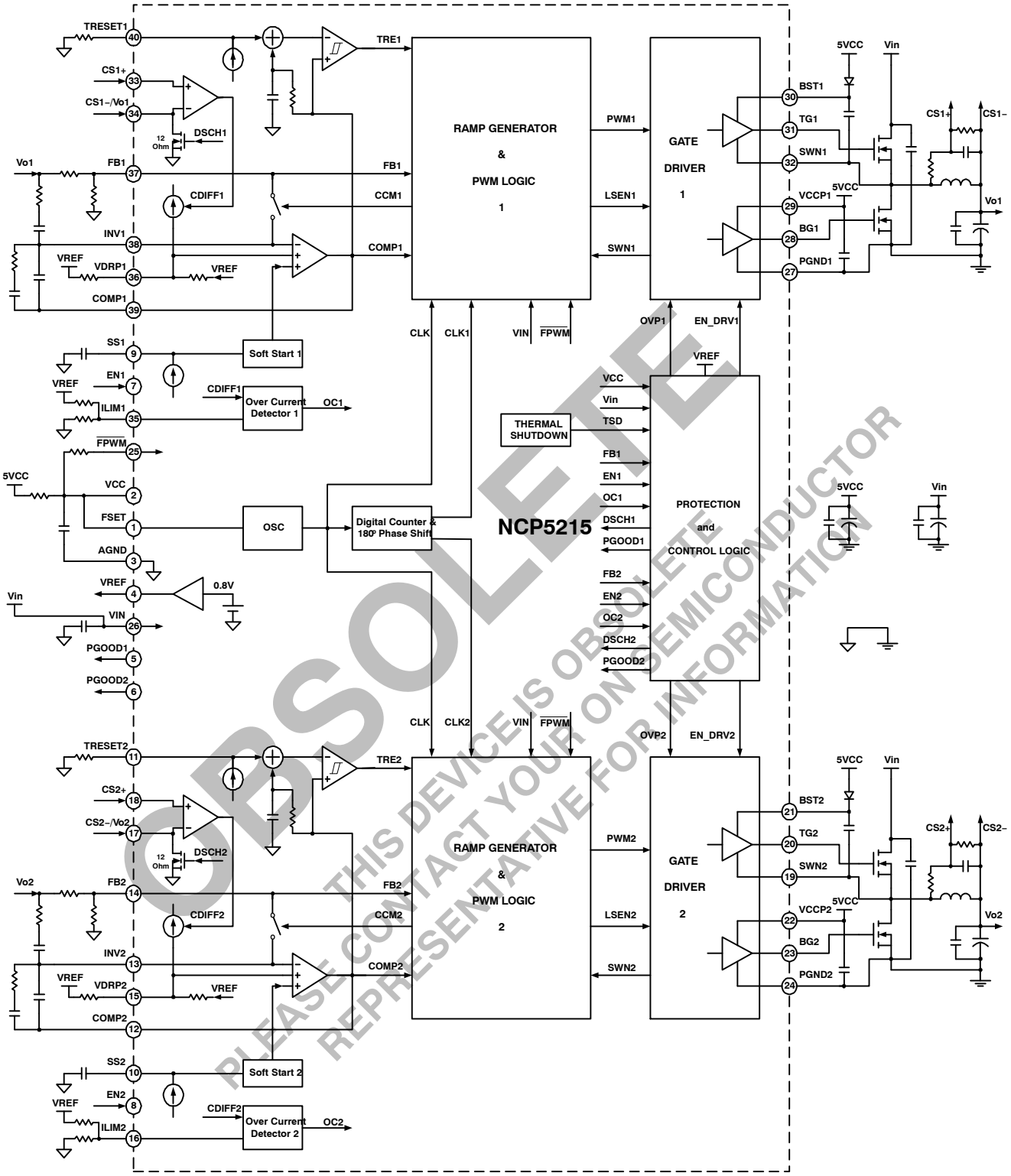


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**Figure 1. Internal Block Diagram and Typical Application**

**PIN FUNCTION DESCRIPTION**

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | FSET | **Frequency SET** Programmable pin of switching frequency for two channels. |
| 2 | VCC | **VCC** This pin powers the control section of IC. |
| 3 | AGND | **Analog Ground** Low noise ground for control section of IC. |
| 4 | VREF | **Reference Voltage Output** Internal 0.8 V reference output. |
| 5 | PGOOD1 | **Power GOOD 1** Power good indicator of the output voltage of Channel 1. (Open drained) |
| 6 | PGOOD2 | **Power GOOD 2** Power good indicator of the output voltage of Channel 2. (Open drained) |
| 7 | EN1 | **Enable 1** Enable logic input of Channel 1. |
| 8 | EN2 | **Enable 2** Enable logic input of Channel 2. |
| 9 | SS1 | **Soft−Start 1** Soft−starting programmable pin of Channel 1. |
| 10 | SS2 | **Soft Start 2** Soft−starting programmable pin of Channel 2. |
| 11 | TRESET2 | **Transient Response Enhancement SET 2** Channel 2 Transient−Response−Enhancement (TRE) programmable pin. |
| 12 | COMP2 | **COMP2** Output of the error amplifier of Channel 2. |
| 13 | INV2 | **Inverting Input 2** Error amplifier's inverting input pin of Channel 2. |
| 14 | FB2 | **Feedback 2** Output voltage feedback of Channel 2. |
| 15 | VDRP2 | **Voltage Droop 2** Channel 2 voltage droop output to the compensation. This pin is used to program the adaptive−voltage−position (AVP) function for Channel 2. |
| 16 | ILMT2 | **Current Limit 2** Current limit programmable pin of Channel 2. |
| 17 | CS2− / Vo2 | **Current Sense 2−** Channel 2 inductor current differential sense inverting input. |
| 18 | CS2+ | **Current Sense 2+** Channel 2 inductor current differential sense non−inverting input. |
| 19 | SWN2 | **Switch Node 2** Switch node between the top MOSFET and bottom MOSFET of Channel 2. |
| 20 | TG2 | **Top Gate 2** Gate driver output of the top N−Channel MOSFET for Channel 2. |
| 21 | BST2 | **BOOTSTRAP Connection 2** Channel 2 top gate driver input supply, a bootstrap capacitor connection between SWN2 and this pin. |
| 22 | VCCP2 | **VCC Power 2** This pin powers the bottom gate driver of Channel 2. |
| 23 | BG2 | **Bottom Gate 2** Gate driver output of the bottom N−Channel MOSFET for Channel 2. |
| 24 | PGND2 | **Power Ground 2** Ground reference and high−current return path for the bottom gate driver of Channel 2. |
| 25 | FPWM# | **Forced PWM** Forced PWM enable logic input. Low to enable forced PWM mode and disable power−saving mode for both channels. |
| 26 | Vin | **Vin** Input voltage monitor input. |
| 27 | PGND1 | **Power Ground 1** Ground reference and high−current return path for the bottom gate driver of Channel 1. |
| 28 | BG1 | **Bottom Gate 1** Gate driver output of the bottom N−Channel MOSFET for Channel 1. |
| 29 | VCCP1 | **VCC Power 1** This pin powers the bottom gate driver of Channel 1. |
| 30 | BST1 | **BOOTSTRAP Connection 1** Channel 1 top gate driver input supply, a bootstrap capacitor connection between SWN1 and this pin. |
| 31 | TG1 | **Top Gate 1** Gate driver output of the top N−Channel MOSFET for Channel 1. |
| 32 | SWN1 | **Switch Node 1** Switch node between the top MOSFET and bottom MOSFET of Channel 1. |
| 33 | CS1+ | **Current Sense 1+** Channel 1 inductor current differential sense non−inverting input. |
| 34 | CS1− / Vo1 | **Current Sense 1−** Channel 1 inductor current differential sense inverting input. |
| 35 | ILMT1 | **Current Limit 1** Current limit programmable pin of Channel 1. |
| 36 | VDRP1 | **Voltage Droop 1** Channel 1 voltage droop output to the compensation. This pin is used to program the Adaptive−Voltage−Position (AVP) function for Channel 1. |
| 37 | FB1 | **Feedback 1** Output voltage feedback of Channel 1. |
| 38 | INV1 | **Inverting Input 1** Error amplifier's inverting input pin of Channel 1. |
| 39 | COMP1 | **COMP1** Output of the error amplifier of Channel 1. |
| 40 | TRESET1 | **Transient Response Enhancement SET 1** Channel 1 Transient−Response−Enhancement (TRE) program pin. |

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**MAXIMUM RATINGS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltages to AGND | $V_{CC}$, $V_{CCP1}$, $V_{CCP2}$ | −0.3, 6.0 | V |
| High−Side Gate Driver Supplies: BST1 to SWN1, BST2 to SWN2<br>High−Side FET Gate Driver Voltages: TG1 to SWN1, TG2 to SWN2 | $V_{BST1} - V_{SWN1}$, $V_{BST2} - V_{SWN2}$, $V_{TG1} - V_{SWN1}$, $V_{TG2} - V_{SWN2}$, | −0.3, 6.0 | V |
| Input Voltage Sense Inputs to AGND | $V_{in}$ | −0.3, 27 | V |
| Switch Nodes | $V_{SWN1}$, $V_{SWN2}$ | −4.0 (<100 ns), −0.3 (dc), 32 | V |
| PGND1, PGND2 to AGND | $V_{GND}$ | −0.3, 0.3 | V |
| Thermal Characteristics<br>Thermal Resistance, Junction−to−Air (Pad soldered to PCB) | $R_{\theta JA}$ | 36 | °C/W |
| Operating Junction Temperature Range | $T_J$ | −40 to +150 | °C |
| Operating Ambient Temperature Range | $T_A$ | −40 to +85 | °C |
| Storage Temperature Range | $T_{stg}$ | −55 to +150 | °C |
| Moisture Sensitivity Level | MSL | 1 | − |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) ≤2.0kV per JEDEC standard: JESD22−A114.
   Machine Model (MM) =≤200V per JEDEC standard: JESD22−A115, except Pin 17 and Pin 34, which are ≤150V.
2. Latchup Current Maximum Rating: ≤150mA per JEDEC standard: JESD78.

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**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 5.0 V, $V_{IN}$ = 12 V, $F_{SET}$ = 5.0 V, Fsw = 300 kHz, $T_A$ = −40°C to 85°C, unless otherwise noted.)

| Characteristic | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **SUPPLY VOLTAGE** | | | | | | |
| Input Voltage | Vin | – | 4.5 | – | 24 | V |
| $V_{CC}$ Operating Voltage | $V_{CC}$ | – | 4.5 | 5.0 | 5.5 | V |
| $V_{CCP1}$ Operating Voltage | $V_{CCP1}$ | – | 4.5 | 5.0 | 5.5 | V |
| $V_{CCP2}$ Operating Voltage | $V_{CCP2}$ | – | 4.5 | 5.0 | 5.5 | V |
| **SUPPLY CURRENT** | | | | | | |
| $V_{CC}$ Quiescent Supply Current in Normal Operation | $I_{VCC\_N}$ | VEN1 = VEN2 = 5.0 V, VFPWM# = 0 V TG1, BG1, TG2, and BG2 are open | – | 3.0 | 6.0 | mA |
| $V_{CC}$ Quiescent Supply Current in Power−Saving Operation | $I_{VCC\_PS}$ | VEN1 = VEN2 = 5.0 V, VFPWM# = 5.0 V TG1, BG1, TG2, and BG2 are open | – | 3.0 | 6.0 | mA |
| $V_{CC}$ Shutdown Current | $I_{VCC\_SD}$ | VEN1 = VEN2 = 0 V | – | – | 10 | μA |
| $V_{CCP}$ Quiescent Supply Current in Normal Operation | $I_{VCCP1\_N}$, $I_{VCCP2\_N}$ | VEN1 = VEN2 = 5.0 V, VFPWM# = 0 V TG1, BG1, TG2, and BG2 are open | – | 1.2 | 2.0 | mA |
| $V_{CCP}$ Shutdown Current | $I_{VCCP1\_SD}$, $I_{VCCP2\_SD}$ | VEN1 = VEN2 = 0 V | – | – | 10 | μA |
| BST Quiescent Supply Current in Normal Operation | $I_{BST1\_N}$, $I_{BST2\_N}$ | VEN1 = VEN2 = 5.0 V, VFPWM# = 0 V TG1, BG1, TG2, and BG2 are open | – | 1.0 | 2.0 | mA |
| BST Shutdown Current | $I_{BST1\_SD}$, $I_{BST2\_SD}$ | VEN1 = VEN2 = 0 V | – | – | 5.0 | μA |
| **VOLTAGE−MONITOR** | | | | | | |
| $V_{CC}$ Start Threshold | $VCC_{UV+}$ | $V_{CC}$ and $V_{CCP}$ are connected to the same voltage source | 4.05 | 4.25 | 4.48 | V |
| $V_{CC}$ UVLO Hysteresis | $VCC_{hys}$ | – | 200 | 275 | 400 | mV |
| Power Good Higher Threshold | VPGH | With Respect to Error Comparator Threshold of 0.8 V | – | 112 | – | % |
| Power Good Lower Threshold | VPGL | With Respect to Error Comparator Threshold of 0.8 V | – | 88 | – | % |
| Output Overvoltage Trip Threshold | FBOVPth | With respect to Error Comparator Threshold of 0.8 V | 113 | 117 | 121 | % |
| Overvoltage Fault Propagation Delay | – | FB forced 2% above trip threshold | – | 1.5 | – | μs |
| Output Undervoltage Trip Threshold | FBUVPth | With respect to Error Comparator Threshold of 0.8 V | 63 | 68 | 73 | % |
| Output Undervoltage Protection Blanking Time | $UVPT_{blk}$ | (Note 3) | – | 16/fsw | – | s |
| **VREF OUTPUT** | | | | | | |
| Reference Voltage | $V_{ref}$ | $T_A$ = 25°C<br>$T_A$ = −40 to 85°C | 0.796<br>0.792 | 0.8<br>– | 0.804<br>0.808 | V |
| Reference Load Regulation | $\Delta V_{ref}$ | Ivref = 0 to 100 μA | – | – | 4.0 | mV |
| Sinking Current | Isink_VREF | Vref rises 10% | 20 | – | – | μA |
| **CURRENT LIMIT** | | | | | | |
| Current Limit Threshold | $V_{((CS+)-(CS-))}$ | $V_{ILIM}$ = 0.4 V | 72 | 80 | 88 | mV |
| ILIM Setting Range | $Range_{ILIM}$ | (Note 3) | – | – | 0.8 | V |

3. Guaranteed by design, not tested in production.

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**ELECTRICAL CHARACTERISTICS (continued)** ($V_{CC}$ = 5.0 V, $V_{IN}$ = 12 V, $F_{SET}$ = 5.0 V, Fsw = 300 kHz, $T_A$ = −40°C to 85°C, unless otherwise noted)

| Characteristic | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **THERMAL SHUTDOWN** | | | | | | |
| Thermal Shutdown | Tsd | (Note 4) | – | 150 | – | °C |
| Thermal Shutdown Hysteresis | Tsdhys | (Note 4) | – | 30 | – | °C |
| **OSCILLATOR** | | | | | | |
| Operation Frequency | Fsw | FSET pin open loop ($T_A$ = 25°C) | 160 | 200 | 240 | kHz |
| | | Pull high FSET pin ($T_A$ = 25°C)<br>($T_A$ = −40°C to 85°C) | 262.5<br>255 | 300<br>– | 337.5<br>345 | kHz |
| | | Pull low FSET pin ($T_A$ = 25°C) | 340 | 400 | 460 | kHz |
| **SOFT−START** | | | | | | |
| Soft−Start Source Current | $I_{SS}$ | – | 3.0 | 4.0 | 5.0 | μA |
| Soft−Start Complete Threshold | $V_{SSTh}$ | (Note 4) | – | 0.9 | – | V |
| **SWITCHING REGULATORS** | | | | | | |
| Main Ramp Amplitude Voltage | Vramp | $V_{IN}$ = 5.0 V (Note 4) | – | 1.25 | – | V |
| Maximum Duty Cycle | Dmax | $V_{IN}$ = 5.0 V | – | 92 | – | % |
| | | $V_{IN}$ = 12 V | – | 48 | – | % |
| | | $V_{IN}$ = 24 V | – | 27 | – | % |
| **GATE DRIVERS** | | | | | | |
| TG Gate Pull−HIGH Resistance | $R_{H\_TG1}$, $R_{H\_TG2}$ | $V_{BST}−V_{SWN}$ = 5.0 V,<br>$V_{TG}−V_{SWN}$ = 4.0 V | – | 1.5 | 4.0 | Ω |
| TG Gate Pull−LOW Resistance | $R_{L\_TG1}$, $R_{L\_TG2}$ | $V_{BST}−V_{SWN}$ = 5.0 V,<br>$V_{TG}−V_{SWN}$ = 1.0 V | – | 1.5 | 4.0 | Ω |
| BG Gate Pull−HIGH Resistance | $R_{H\_BG1}$, $R_{H\_BG2}$ | $V_{CCP}$ = 5.0 V, $V_{BG}$ = 4.0 V | – | 1.5 | 4.0 | Ω |
| BG Gate Pull−LOW Resistance | $R_{L\_BG1}$, $R_{L\_BG2}$ | $V_{CCP}$ = 5.0 V, $V_{BG}$ = 1.0 V | – | 0.5 | 1.5 | Ω |
| Dead Time | $T_{LH}$ | BG Falling to TG Rising | – | 42 | – | ns |
| | $T_{HL}$ | TG Falling to BG Rising | – | 34 | – | |
| **DIFFERENTIAL CURRENT ERROR AMPLIFIER** | | | | | | |
| Input Bias Current | CS−IIB | – | −200 | – | 200 | nA |
| CS+ to CS− Input Signal Range | VCS_MAX | Refer to AGND | – | – | 3.0 | V |
| Output Voltage Swing | VOS_DRP | (Note 4) | 0.6 | – | 1.0 | V |
| Offset Current at VDRP | Ioffset_DRP | (CS+)−(CS−) = 0 V, no connection from VDRP pin to VREF | −1.0 | – | 1.0 | μA |
| [(CS+)−(CS−)] to VDRP Gain | Gain_CS<br>((V_VDRP−Vref)/<br>((CS+)−(CS−))) | (CS+)−(CS−) = 20 mV | 2.35 | 2.6 | 2.85 | V/V |
| Internal Droop Resistance | $R_{DRP}$ | From $V_{DRP}$ to $V_{REF}$ | 2.4 | 2.65 | 2.9 | kΩ |

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**ELECTRICAL CHARACTERISTICS (continued)** ($V_{CC}$ = 5.0 V, $V_{IN}$ = 12 V, $F_{SET}$ = 5.0 V, Fsw = 300 kHz, $T_A$ = −40°C to 85°C, unless otherwise noted)

| Characteristic | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **VOLTAGE ERROR AMPLIFIER** | | | | | | |
| DC Gain | GAIN_VEA | (Note 5) | – | 80 | – | dB |
| Unity Gain Bandwidth | Ft_VEA | (Note 5) | – | 13 | – | MHz |
| Slew Rate | SR_VEA | (Note 5)<br>(COMP PIN TO GND = 100 pF) | – | 1.0 | – | V/μs |
| Inverting Input Current | $I_{INV1}$, $I_{INV2}$ | $V_{INV}$ = 0.8 V | – | – | 0.5 | μA |
| Output Voltage Swing | VOS_EA | – | 1.0 | – | 3.0 | V |
| Source Current | Isource_EA | COMP = 3.0 V | 2.0 | 4.0 | – | mA |
| Sink Current | Isink_EA | COMP = 1.0 V | 1.5 | 2.0 | – | mA |
| **CONTROL SECTION** | | | | | | |
| VEN1, VEN2 Threshold High | $V_{EN1\_H}$, $V_{EN2\_H}$ | – | 1.4 | – | – | V |
| VEN1, VEN2 Threshold Low | $V_{EN1\_L}$, $V_{EN2\_L}$ | – | – | – | 0.5 | V |
| VEN1, VEN2 Source Current | $I_{EN1\_SOURCE}$, $I_{EN2\_SOURCE}$ | – | – | – | 0.5 | μA |
| VEN1, VEN2 Sink Current | $I_{EN1\_SINK}$, $I_{EN2\_SINK}$ | – | – | – | 0.5 | μA |
| VFPWM# Threshold High | $V_{FPWM\_H}$ | – | 1.4 | – | – | V |
| VFPWM# Threshold Low | $V_{FPWM\_L}$ | – | – | – | 0.5 | V |
| VFPWM# Source Current | $I_{FPWM\_SOURCE}$ | – | – | – | 0.5 | μA |
| VFPWM# Sink Current | $I_{FPWM\_SINK}$ | – | – | – | 0.5 | μA |
| PGOOD Pin ON Resistance | PGOOD_R | I_PGOOD = 5.0 mA | – | 25 | – | Ω |
| PGOOD Pin OFF Current | PGOOD_LK | – | – | – | 1.0 | μA |
| **OUTPUT DISCHARGE MODE** | | | | | | |
| Output Discharge On−Resistance | $R_{discharge}$ | – | – | 12 | – | Ω |
| System Restart Threshold of the Output Voltage | Vth_SRST | – | 0.2 | 0.3 | 0.4 | V |
| **TRE OFFSET** | | | | | | |
| TRESET Offset Current | $I_{TRE}$ | – | 3.0 | 4.0 | 5.0 | μA |

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## TYPICAL OPERATING CHARACTERISTICS

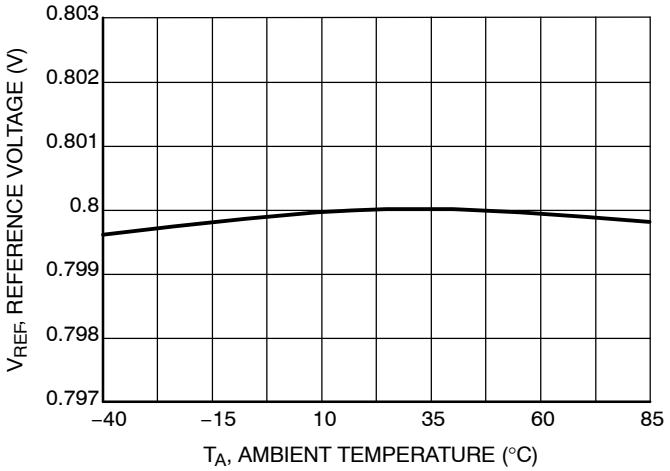


**Figure 2. Reference Voltage vs. Ambient Temperature**

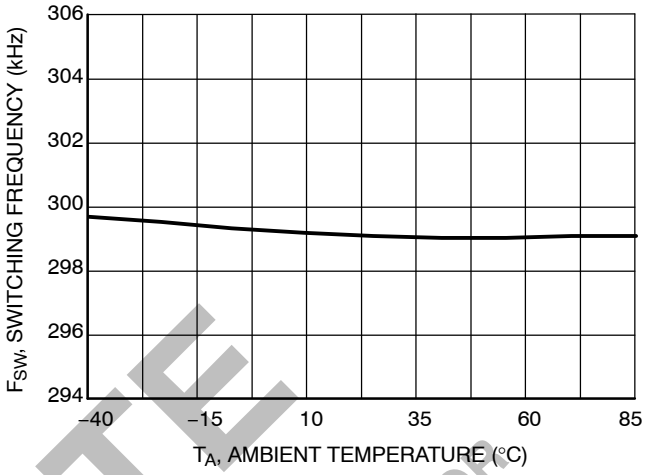


**Figure 3. Switching Frequency vs. Ambient Temperature**

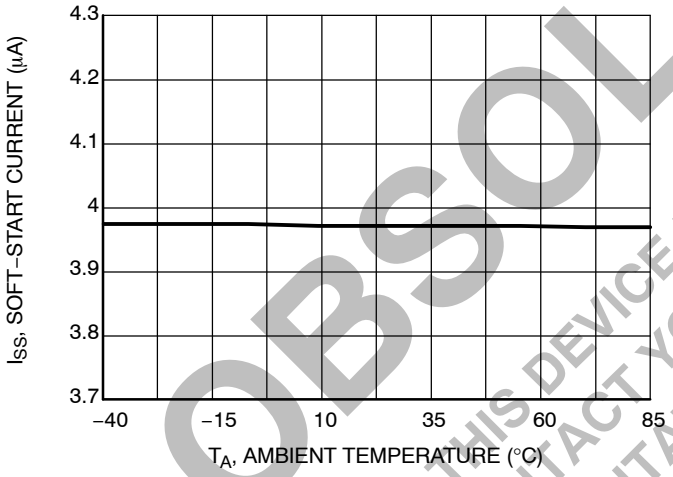


**Figure 4. Soft−Start Current vs. Ambient Temperature**

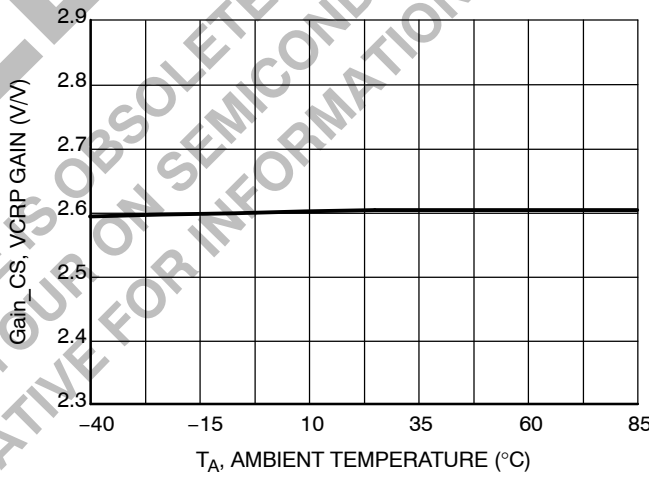


**Figure 5. $V_{DRP}$ Gain vs. Ambient Temperature**

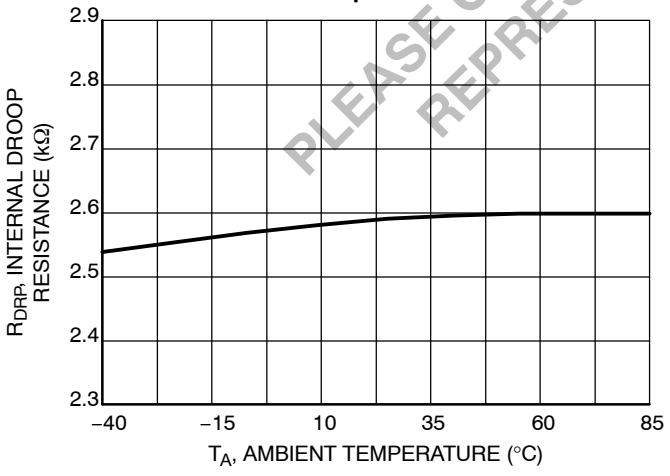


**Figure 6. Internal Droop Resistance vs. Ambient Temperature**

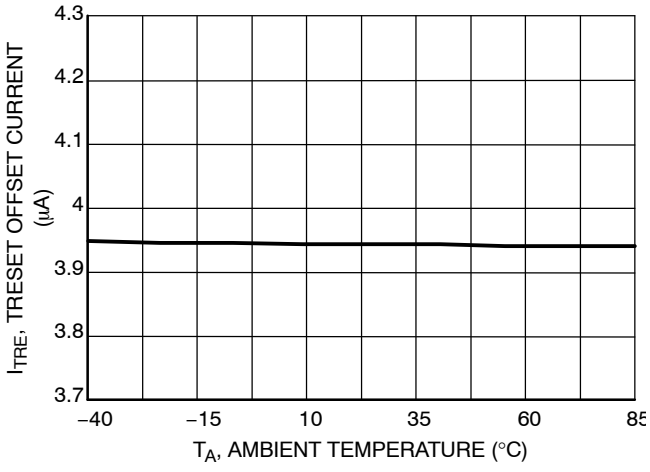


**Figure 7. TRESET Offset Current vs. Ambient Temperature**

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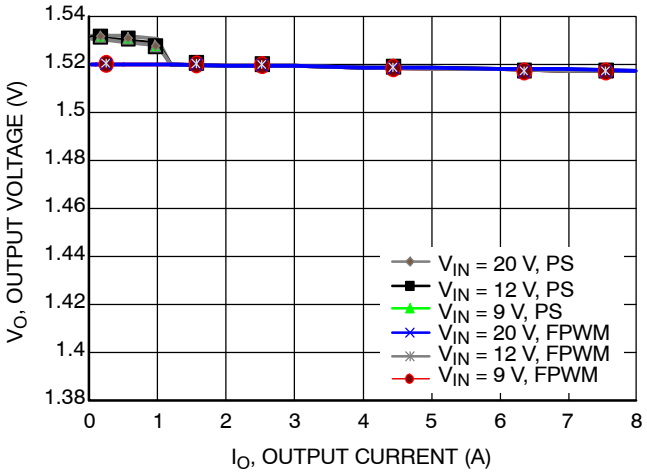


**Figure 8. Output Voltage vs. Output Current ($V_O$ = 1.5 V, without AVP Function)**

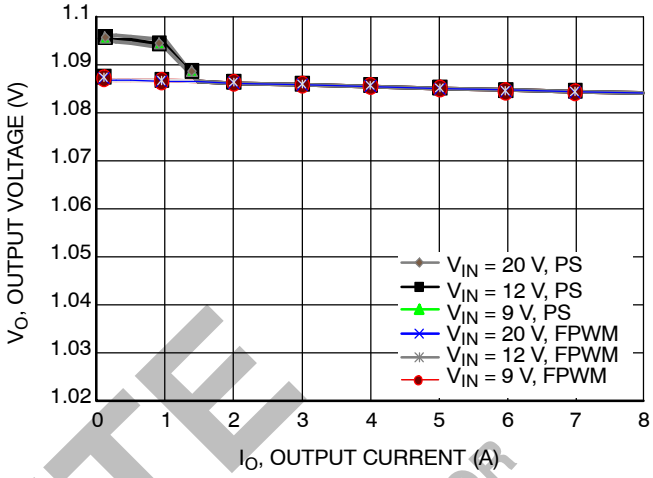


**Figure 9. Output Voltage vs. Output Current (Vo = 1.05 V, Without AVP Function)**

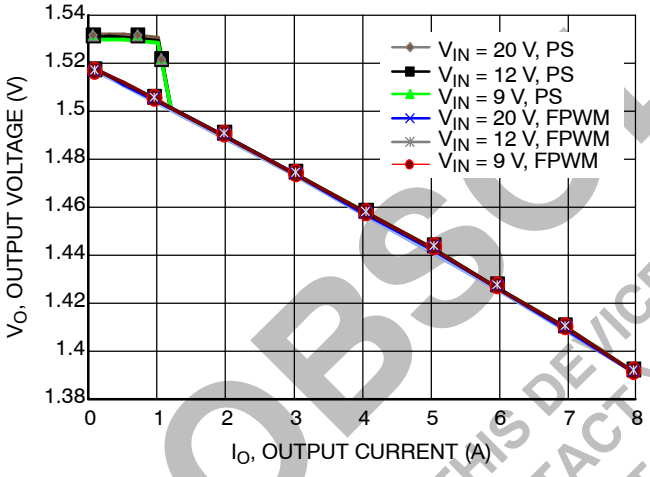


**Figure 10. Output Voltage vs. Output Current ($V_O$ = 1.5 V, with AVP Function)**

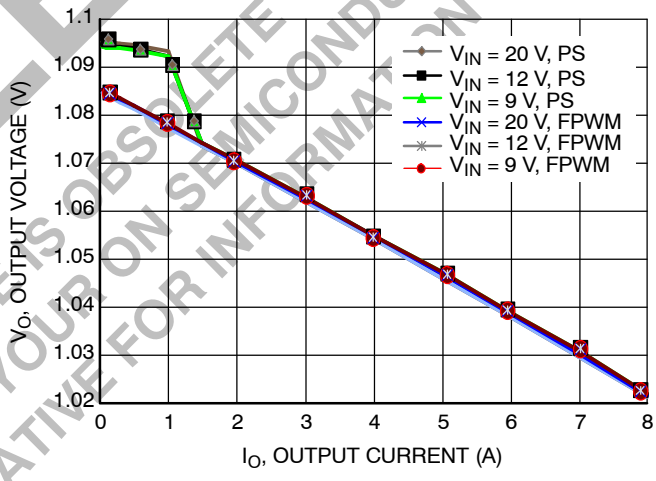


**Figure 11. Output Voltage vs. Output Current ($V_O$ = 1.05 V, with AVP Function)**

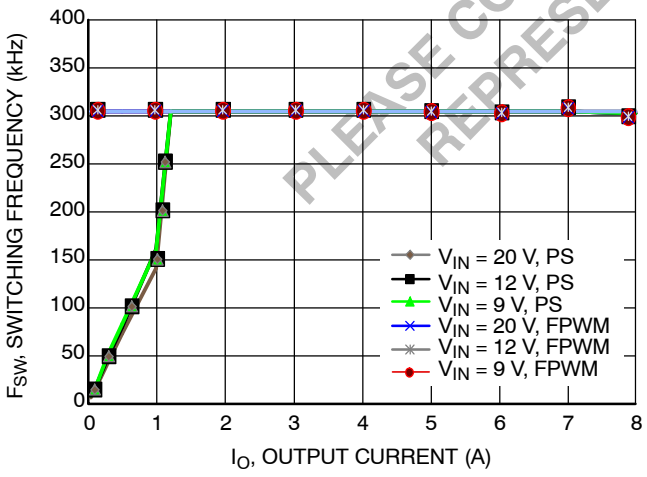


**Figure 12. Switching Frequency vs. Output Current ($V_O$ = 1.5 V)**

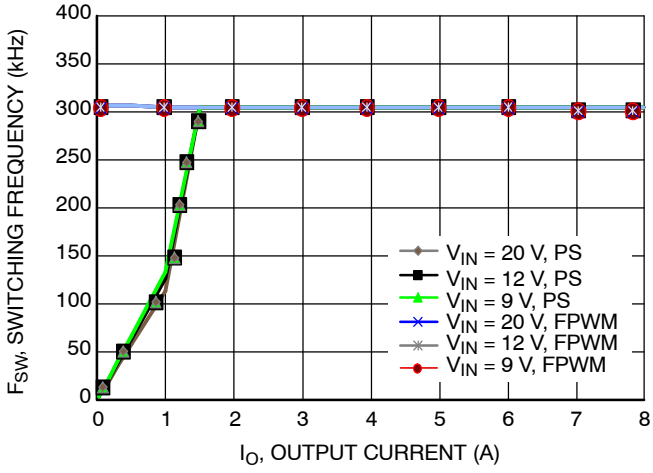


**Figure 13. Switching Frequency vs. Output Current ($V_O$ = 1.05 V)**

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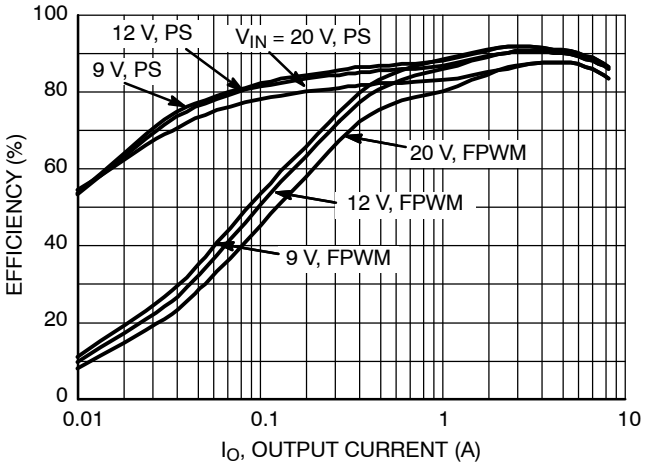


**Figure 14. Efficiency vs. Output Current ($V_O$ = 1.5 V)**

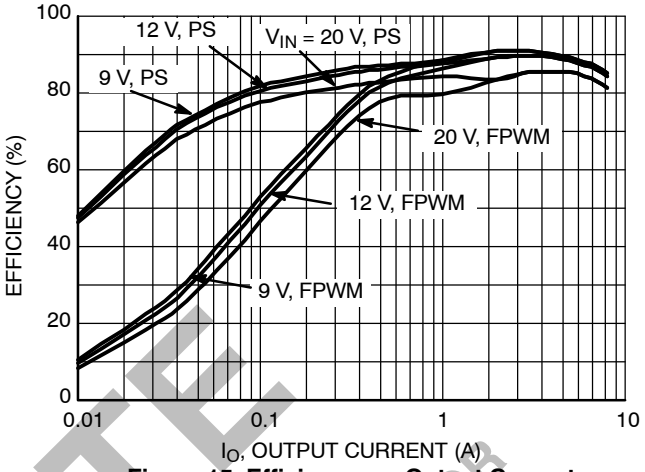


**Figure 15. Efficiency vs. Output Current ($V_O$ = 1.05 V)**

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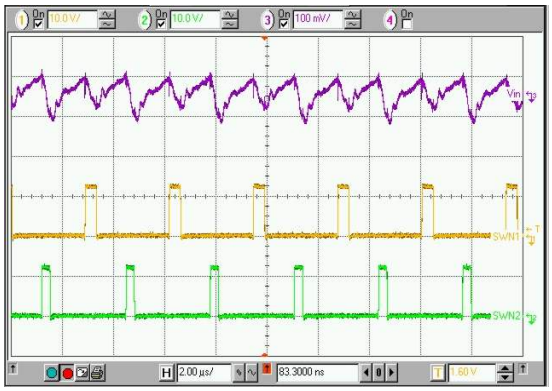
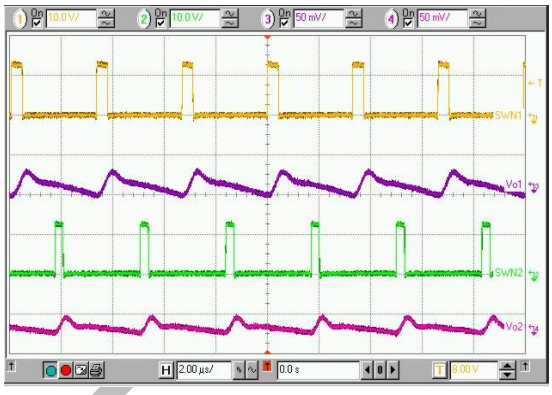



Top: Vin, Input Voltage Ripple, (100mV/div)
Middle: SWN1, CH1 Switching Node Voltage, (10V/div)
Bottom: SWN2, CH2 Switching Node Voltage, (10V/div)
Time: 2μs/div

**Figure 16. Input Voltage Ripple with Interleaved Operation ($V_O1$ = 1.5 V, $I_O1$ = 4 A, $V_O2$ = 1.05 V, $I_O2$ = 6 A)**




Top: SWN1, CH1 Switching Node Voltage, (10V/div)
Middle 1: Vo1, CH1 Output Voltage Ripple, (50mV/div)
Middle 2: SWN2, CH2 Switching Node Voltage, (10V/div)
Bottom: Vo2, CH2 Output Voltage Ripple, (50mV/div)
Time: 2μs/div

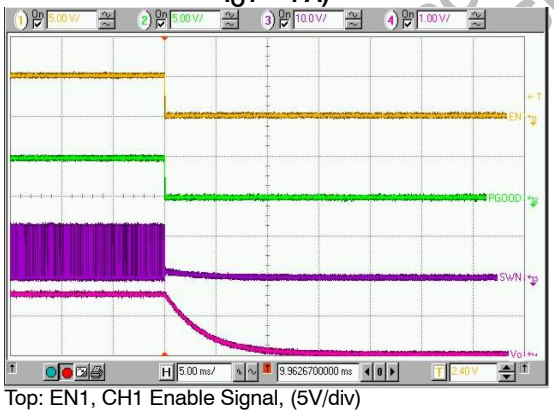
**Figure 17. Output Voltage Ripple with Interleaved Operation ($V_O1$ = 1.5 V, $I_O1$ = 4 A, $V_O2$ = 1.05 V, $I_O2$ = 6 A)**


Top: EN1, CH1 Enable Signal, (5V/div)
Middle 1: PGOOD1, CH1 Power Good Signal, (5V/div)
Middle 2: SWN1, CH1 Switching Node Voltage, (10V/div)
Bottom: $V_O1$, CH1 Output Voltage, (1V/div)
Time: 200μs/div

**Figure 18. Powerup Operation ($V_O1$ = 1.5 V, $I_O1$ = 4 A)**

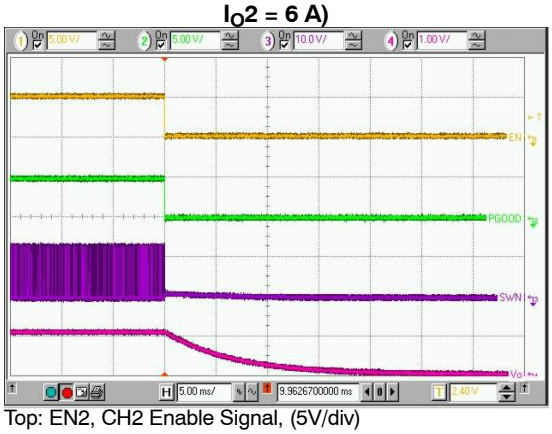

Top: EN2, CH2 Enable Signal, (5V/div)
Middle 1: PGOOD2, CH2 Power Good Signal, (5V/div)
Middle 2: SWN2, CH2 Switching Node Voltage, (10V/div)
Bottom: $V_O2$, CH2 Output Voltage, (1V/div)
Time: 200μs/div

**Figure 19. Powerup Operation ($V_O2$ = 1.05 V, $I_O2$ = 6 A)**




Top: EN1, CH1 Enable Signal, (5V/div)
Middle 1: PGOOD1, CH1 Power Good Signal, (5V/div)
Middle 2: SWN1, CH1 Switching Node Voltage, (10V/div)
Bottom: $V_O1$, CH1 Output Voltage, (1V/div)
Time: 5ms/div

**Figure 20. Powerdown Operation ($V_O1$ = 1.5 V, $I_O1$ = 0 A, FPWM)**




Top: EN2, CH2 Enable Signal, (5V/div)
Middle 1: PGOOD2, CH2 Power Good Signal, (5V/div)
Middle 2: SWN2, CH2 Switching Node Voltage, (10V/div)
Bottom: Vo2, CH2 Output Voltage, (1V/div)
Time: 5ms/div

**Figure 21. Powerdown Operation ($V_O2$ = 1.05 V, $I_O2$ = 0 A, FPWM)**

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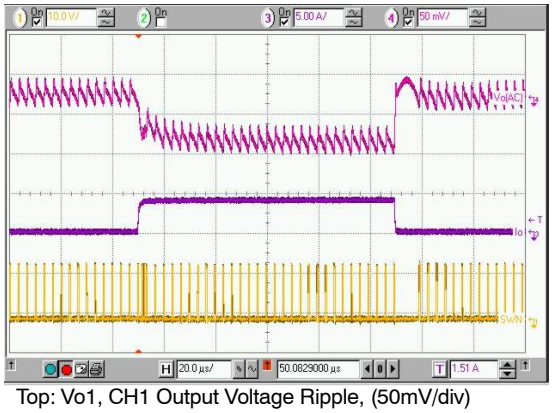
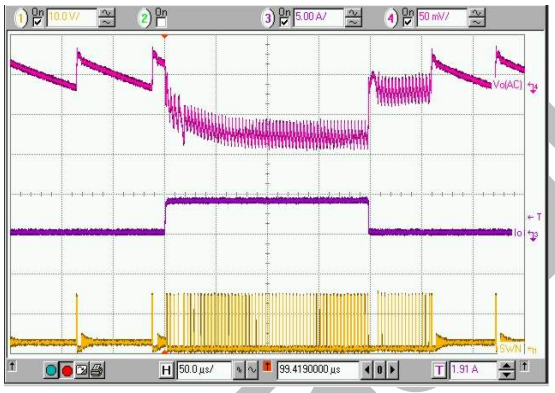


Top: Vo1, CH1 Output Voltage Ripple, (50mV/div)
Middle: Io1, CH1 Output Current, (5A/div)
Bottom: SWN1, CH1 Switching Node Voltage, (10V/div)
Time: 20μs/div

**Figure 22. Load Transient Response with FPWM Operation ($V_O1$ = 1.5 V, $I_O1$ = 0 A–4 A–0 A)**

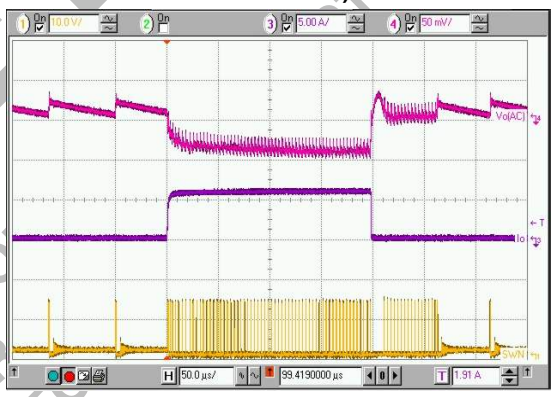
Top: Vo2, CH2 Output Voltage Ripple, (50mV/div)
Middle: Io2, CH2 Output Current, (5A/div)
Bottom: SWN2, CH2 Switching Node Voltage, (10V/div)
Time: 20μs/div

**Figure 23. Load Transient Response with FPWM Operation ($V_O2$ = 1.05 V, $I_O2$ = 0 A–6 A–0 A)**



Top: Vo1, CH1 Output Voltage Ripple, (50mV/div)
Middle: Io1, CH1 Output Current, (5A/div)
Bottom: SWN1, CH1 Switching Node Voltage, (10V/div)
Time: 50μs/div

**Figure 24. Load Transient Response with Skip–Mode Operation ($V_O1$ = 1.5 V, $I_O1$ = 0.1 A–4 A–0.1 A)**

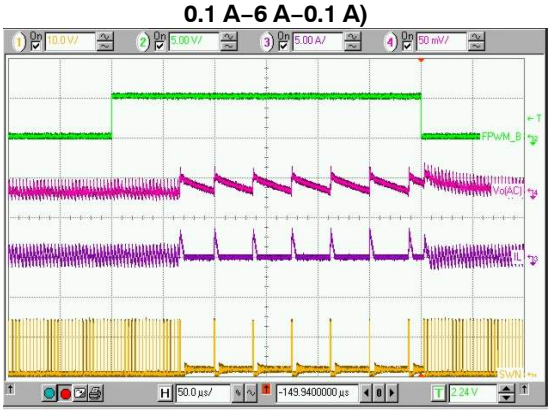


Top: Vo2, CH2 Output Voltage Ripple, (50mV/div)
Middle: Io2, CH2 Output Current, (5A/div)
Bottom: SWN2, CH2 Switching Node Voltage, (10V/div)
Time: 50μs/div

**Figure 25. Load Transient Response with Skip–Mode Operation ($V_O2$ = 1.05 V, $I_O2$ = 0.1 A–6 A–0.1 A)**

Top: FPWM#, FPWM# Signal, (5V/div)
Middle 1: Vo1, CH1 Output Voltage Ripple, (50mV/div)
Middle 2: iL1, CH1 Inductor Current, (5A/div)
Bottom: SWN1, CH1 Switching Node Voltage, (10V/div)
Time: 50μs/div

**Figure 26. On–Line Mode–Changing Operation ($V_O1$ = 1.5 V, $I_O1$ = 0.2 A, FPWM–Skip Mode–FPWM)**



Top: FPWM#, FPWM# Signal, (5V/div)
Middle 1: Vo2, CH2 Output Voltage Ripple, (50mV/div)
Middle 2: iL2, CH2 Inductor Current, (5A/div)
Bottom: SWN2, CH2 Switching Node Voltage, (10V/div)
Time: 50μs/div

**Figure 27. On–Line Mode–Changing Operation ($V_O2$ = 1.05 V, $I_O2$ = 0.2 A, FPWM–Skip Mode–FPWM)**

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## OPERATION DESCRIPTION

### General

The NCP5215, a high−efficiency and fast−transient−response dual−channel buck controller, provides a multifunctional power solution for notebook power system. 180° interleaved operation function between the two channels has capabilities of reducing the common input capacitor requirement and improving noise immunity. Adaptive−Voltage−Positioning (AVP) control reduces the requirement of output filter capacitors. Programmable power−saving operation ensures high efficiency over entire load range. Input feedforward voltage−mode control is employed to deal with wide input voltage range. Transient−Response−Enhancement (TRE) control for the both channels enables fast transient response.

### PWM Operation

The NCP5215 operates at a pin−selectable normal operation switching frequency, allowing 200 kHz, 300 kHz, or 400 kHz. As shown in Table 1, the connection of the pin FSET determines normal operation frequency in continuous−conduction−mode (CCM).

**Table 1. SWITCHING FREQUENCY SELECTION**

| FSET Pin | Float | VCC | GND |
|---|---|---|---|
| Fsw (kHz) | 200 | 300 | 400 |

To speed up transient response and increase sampling rate, an internal high−frequency clock is employed, which frequency is four times of the selected normal operating frequency. As an instance, if the FSET pin is connected to $V_{CC}$, the normal switching frequency is set to 300 kHz. The internal high−frequency clock is 1.2 MHz. Figure 28 shows internal clocks of the NCP5215 in this case. The 1.2MHz high−frequency clock with 50% duty−ratio introduced to the two PWM channels. A digital circuitry generates two interleaved 300 kHz clocks using the 1.2 MHz clock and output them to the two PWM channels as normal operation clocks in CCM, respectively.

### Forced−PWM Operation (FPWM Mode)

If the FPWM# pin is pulled low, the NCP5215 works under forced−PWM operation and thus always in CCM. The two channels always run in selected fixed frequency and 180° interleaved operation. In this mode, the low−side gate−drive signal is forced to be the complement of the high−side gate−drive signal. This mode allows reverse inductor current, in such a way that it provides more accurate voltage regulation and fast transient response.

During soft−start operation, the NCP5215 automatically runs in FPWM mode regardless of the FPWM# pin's setting to guarantee smooth powerup.

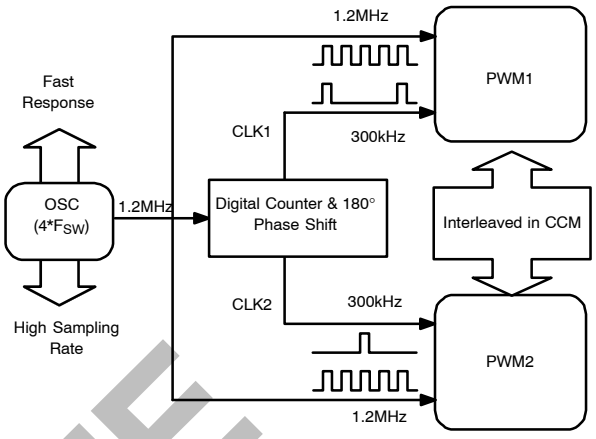


**Figure 28. Internal Clocks in the NCP5215 as $F_{SW}$ = 300 kHz**

### Light−Load Pulse−Skipping Operation (Skip Mode)

If the skip mode is enabled by pulling high FPWM# pin, the NCP5215 works in pulse−skipping enabled operation (PS).

In medium and high load range, the converter still runs in CCM, and the switching frequency is fixed as the selected frequency. If both channels run in CCM, they operate interleaved.

In light load range, the converter will enter skip mode if negative inductor current appears continuously. In the skip mode, the bottom MOSFET will be turned off when the inductor current is going negative. The top MOSFET's on−time is fixed to around 1.5 times as the on−time in CCM. The NCP5215 continuously monitors the voltage at FB pin and comparing to the voltage at VDRP Pin. When the FB voltage drops below the VDRP voltage, a fixed on−time will be initiated at the time of the next coming high−frequency clock edge, which can be either rising edge or falling edge. The minimum off−time is half high−frequency cycle.

When the load increases and the inductor current becomes continuous, the controller will automatically return to fixed−frequency operation and be synchronized to the normal operation clock.

### Transient Response Enhancement (TRE)

In the skip mode, the operation of the NCP5215 is similar to constant on−time scheme. The response time of the controller is between half to one cycle of the high−frequency clock. However, for a conventional trailing−edge PWM controller in CCM, the fastest response time is one switching cycle in the worst case. To further improve transient response in CCM, a transient

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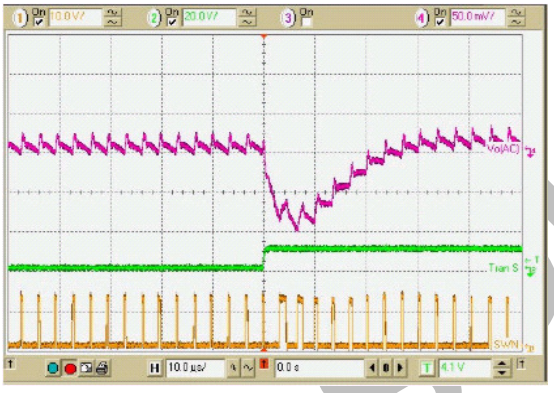
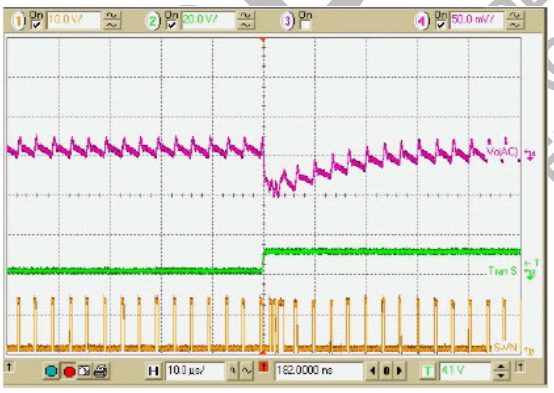
response enhancement circuitry is introduced to the NCP5215.

In CCM operation, the controller continuously monitors the output voltage (COMP) of the error amplifier to detect load transient events. As shown in Figure 1, there is a threshold voltage in each channel made in a way that a filtered COMP signal pluses an adjustable offset voltage, which is set by an external resistor. Once large load transient occurs, the COMP signal is possible to exceed the threshold and then TRE signal will be high in a short period, which is typically around one normal switching cycle. In this short period, the controller will be running at high frequency and therefore has faster response. After that the controller comes back to normal switching frequency operation. Figure 29 shows TRE effect on a load transient response.



Top: Vo (50mV/div), Middle: Transient signal (20V/div), Bottom: SWN (10V/div), Time: (10us/div)
(a) TRE disabled



Top: Vo (50mV/div), Middle: Transient signal (20V/div), Bottom: SWN (10V/div), Time: (10us/div)
(b) TRE enabled

**Figure 29. Transient Response Comparison on TRE**

The internal offset voltage of the TRE threshold is set by an external resistor $R_{TRE}$ connected from the TRESET Pin to AGND.

$$V_{th\_TRE} = \frac{I_{TRE} \cdot R_{TRE}}{4} \quad \text{(eq. 1)}$$

where $I_{TRE}$ is a sourcing current out the TRESET pin. A recommended value for $V_{th\_TRE}$ is around 1.5 times of peak−to−peak value of the COMP signal in CCM operation. The higher $V_{th\_TRE}$, the lower sensitivity to load transient. The TRE function can be disabled by pulling high the TRESET pin to $V_{CC}$ or just leaving it float.

### Adaptive Voltage Positioning (AVP)

For applications with fast transient currents, adaptive voltage positioning can reduce peak−to−peak output voltage deviations due to load transients and allow use of a smaller output filter. Adaptive voltage positioning sets output voltage higher than nominal at light loads, and output voltage is allowed limited sag when the load current is applied. Upon removal of the load, output voltage returns no higher than the original level, allowing one output transient peak to be canceled over a load stepup and release cycle.

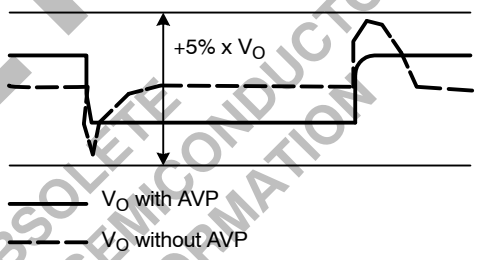



**Figure 30. Adaptive Voltage Positioning**

Figure 30 shows how AVP works. The waveform labeled “Vo without AVP” shows output voltage waveform in a converter without AVP. On the left, the output voltage sags when the output current is stepped up and later overshoots when current is stepped back down. With AVP, the peak−to−peak excursions are cut around in half. The controller can be configured to adjust the output voltage based on the output current of the converter as shown in Figure 31. In order to realize the AVP function, a resistor is connected between $V_{REF}$ and $V_{DRP}$. During no−load conditions, the VDRP Pin voltage stays at the same voltage level as the $V_{REF}$. As the output current increases, the VDRP Pin voltage decreases. This causes $V_{OUT}$ to droop according to a loadline set by the resistor.

In the NCP5215, the output current of each channel is sensed differentially. A high gain and low offset−voltage differential amplifier in each channel allows low−resistance current−sensing resistor or low−DCR inductor to be used to minimize power dissipation. For lossless inductor current sensing as shown in Figure 31, the sensing RC network should satisfy

$$R_{CS} \times C_{CS} = \frac{L}{DCR} \quad \text{(eq. 2)}$$

where DCR is a DC resistance of a inductor, and normally $C_{cs}$ is selected to be around 0.1 μF. In high accuracy

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applications, to compensate measurement error caused by temperature, an additional resistance network including a negative−temperature−coefficient (NTC) thermistor can be connected with $C_{CS}$ in parallel.

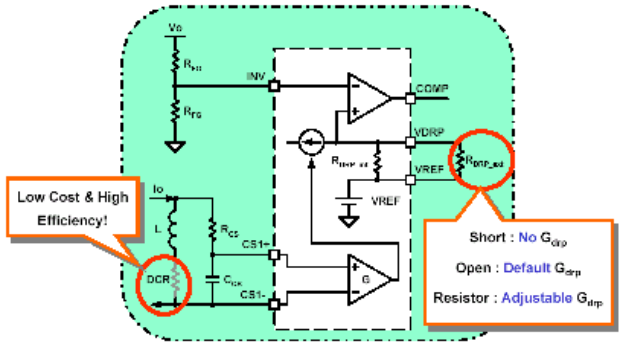


**Figure 31. Programmable AVP with Lossless Inductor Current Sensing**

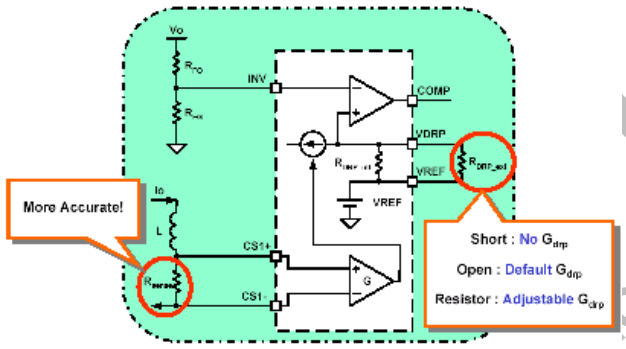


**Figure 32. Figure 32. Programmable AVP with Resistive Current Sensing**

The output voltage with AVP is

$$V_O = V_{O0} - I_O \cdot R_{LL} \quad \text{(eq. 3)}$$

where $I_o$ is load current, no−load output voltage $V_{O0}$ is set by the external resistor divider, that is

$$V_{O0} = \left(1 + \frac{R_{FO}}{R_{FG}}\right) \cdot V_{REF} \quad \text{(eq. 4)}$$

$R_{FO}$ is a resistor connected between the output and the FB pin, and $R_{FG}$ is a resistor connected between the FB Pin to AGND. The load−line impedance $R_{LL}$ by the AVP function is given by

$$R_{LL} = \text{DCR Gain\_CS} \cdot \frac{R_{DRP\_ext}}{R_{DRP\_int} + R_{DRP\_ext}} \cdot \frac{V_{O0}}{V_{REF}} \quad \text{(eq. 5)}$$

where DCR is DC resistance of the inductor, Gain_CS is a gain from [(CS+)−(CS−)] to (VDRP−VREF), $R_{DRP\_int}$ is a internal resistance connected between the output reference and the VDRP Pin, $R_{DRP\_ext}$ is a external resistance connected between the output reference and the VDRP pin.

If an additional current sensing resistor ($R_{CS}$) is employed to improve accuracy, as shown in Figure 32, the load line resistance can be calculated by

$$R_{LL} = R_{CS}\,\text{Gain\_CS} \cdot \frac{R_{DRP\_ext}}{R_{DRP\_int} + R_{DRP\_ext}} \cdot \frac{V_{O0}}{V_{REF}} \quad \text{(eq. 6)}$$

The AVP function can be easily disabled by shorting VDRP pin and VREF pin together.

### Control Logic

The internal control logic is powered by $V_{CC}$. Figure 33 shows a power−up and powerdown timing diagram for each channel. Figure 34 shows a state diagram for each channel.

The NCP5215 continuously monitors $V_{CC}$ and $V_{IN}$ level with an undervoltage lockout (UVLO) function. If both $V_{CC}$ and $V_{IN}$ are in operation range, and output voltage is below 0.3 V, the converter has a soft−start after ENBL signal goes high. The soft−start time is programmed by an external capacitor $C_{SS}$ connected from the SS Pin to AGND, which can be calculated by

$$t_{SS} = \frac{0.8 \times C_{SS}}{I_{SS}} \quad \text{(eq. 7)}$$

where $I_{SS}$ is a sourcing current output from the SS pin.

When the ENBL goes low, or the internal fault latch is set by over current or output undervoltage, the device operates in soft stop and output discharge mode. The output is discharged to GND through an internal 12 Ω switch connected from the CS−/Vo pin to the PGND Pin, until the output voltage decreases to 0.3 V. Also if restart the system when the output voltage is still above 0.3 V, the device will discharge the output voltage to 0.3 V first and then start soft−start.

### Overcurrent Protection (OCP)

The NCP5215 protects power system if overcurrent occurs. The current through each channel is continuously monitored with the differential current sense. Current limit threshold is related to an external voltage at the $I_{LIM}$ pin, which is normally produced by an external resistor divider ($R_{il1}$ and $R_{il2}$) connected from the $V_{REF}$ pin to AGND. The current−limit threshold for peak current is set by

$$I_{LIM(Peak)} = 0.2 \cdot \frac{R_{il2} \cdot V_{REF}}{(R_{il1} + R_{il2}) \cdot \text{DCR}} \quad \text{(eq. 8)}$$

or

$$I_{LIM(Peak)} = 0.2 \cdot \frac{R_{il2} \cdot V_{REF}}{(R_{il1} + R_{il2}) \cdot R_{CS}} \quad \text{(eq. 9)}$$

If inductor current exceeds the current threshold continuously, the top gate drive will be turned off cycle−by−cycle. In the meanwhile, an internal fault timer will be triggered to count normal operation clock. After 16 continuous clock pulses, if the fault still exists the part latches off, both the top gate drive and the bottom gate drive

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are turned off and their outputs are float. The fault remains set until the system has shutdown and re−applied power or the enable input signal to the regulator controller has toggled states.

### Overvoltage Protection (OVP)

An OVP circuit monitors the output voltages to prevent from over voltage. OVP limit is typically 117% of the nominal output voltage level. If the output voltage is above this threshold, an OV fault is set, the top gate drive is turned OFF, and then the bottom gate drive is latched ON to discharge the output. The fault remains set until the system has shutdown and re−applied power or the enable input signal to the regulator controller has toggled states.

### Undervoltage Protection (UVP)

A UVP circuit monitors the output voltages to detect undervoltage. UVP limit is 68% of the nominal output voltage level. If the output voltage is below this threshold, a UV fault is set. If an OV protection is set before, the bottom gate drive is forced high. If no OV protection set, an internal fault timer will be triggered to count normal operation clock. After 16 continuous clock pulses, if the fault still exists the part latches off, both the top gate drive and the bottom gate drive are turned off and their outputs are float. The fault remains set until the system has shutdown and re−applied power or the enable input signal to the regulator controller has toggled states.

### Thermal Protection

The NCP5215 has a thermal shutdown protection to protect the device from overheating when the die temperature exceeds 150°C. Once the thermal protection is triggered, the fault state can be ended by re−applying $V_{CC}$, $V_{IN}$, or ENBL when the temperature drops down below 120°C.

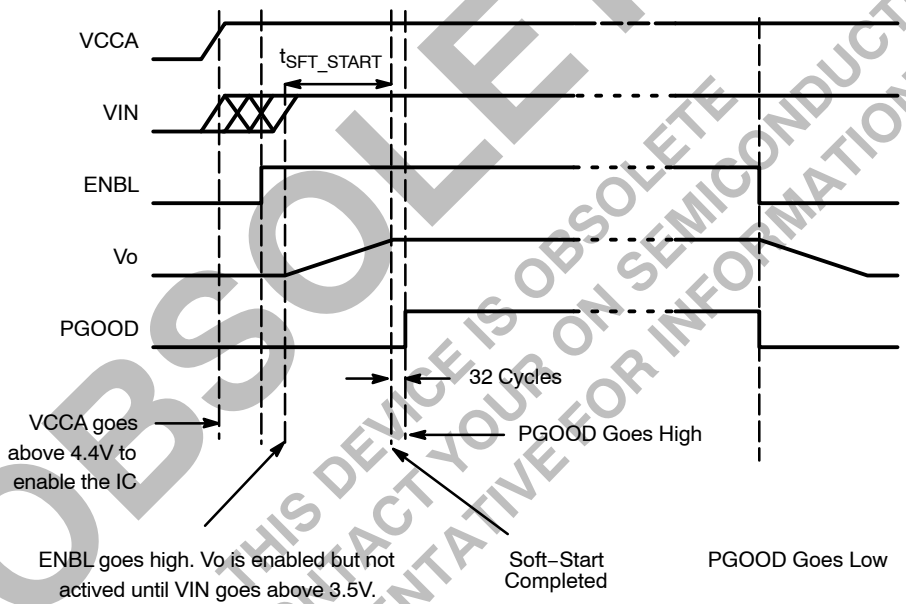


**Figure 33. Powerup and Powerdown Timing Diagram per Channel**

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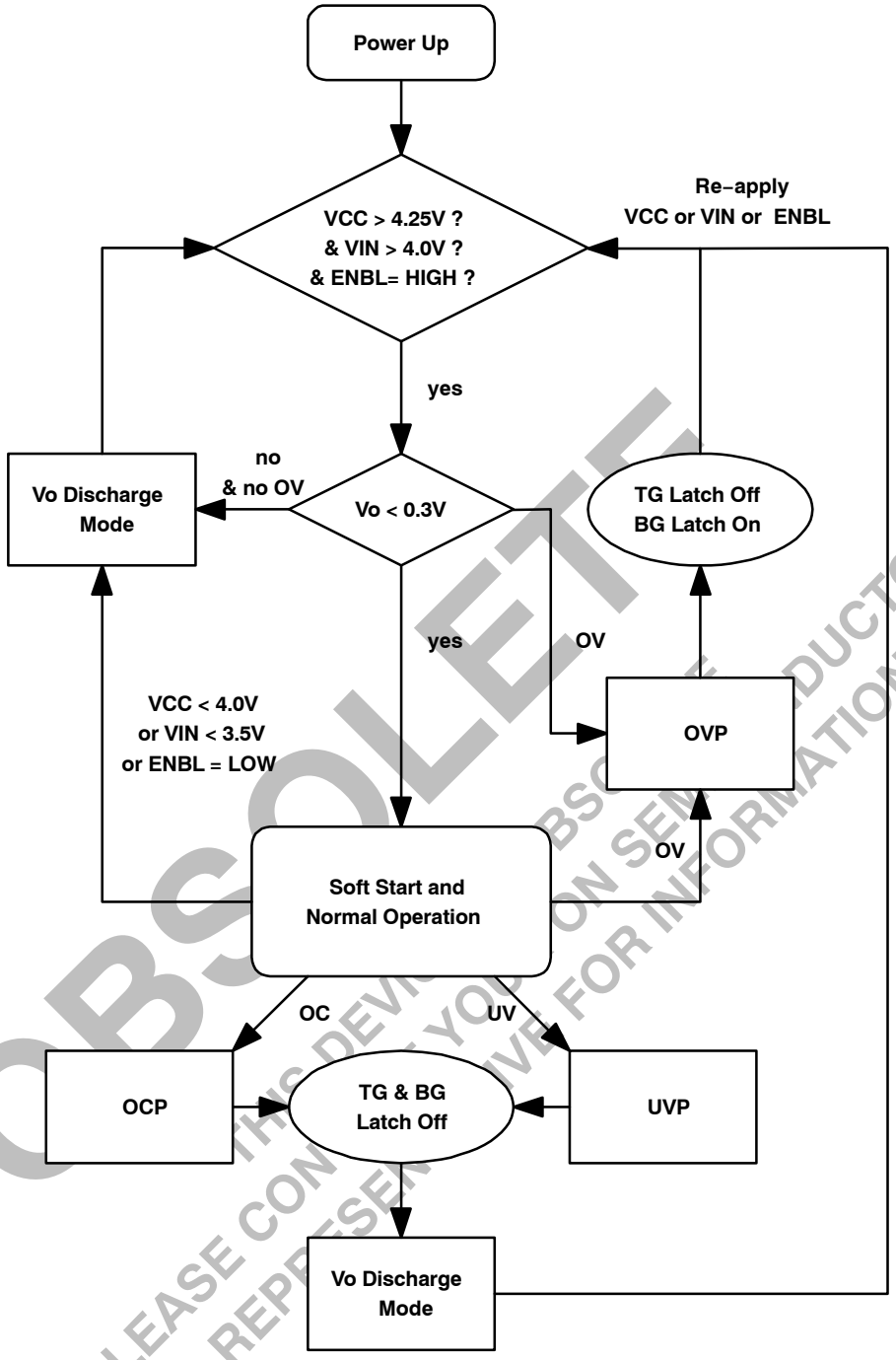


Figure 34. State Diagram per Channel

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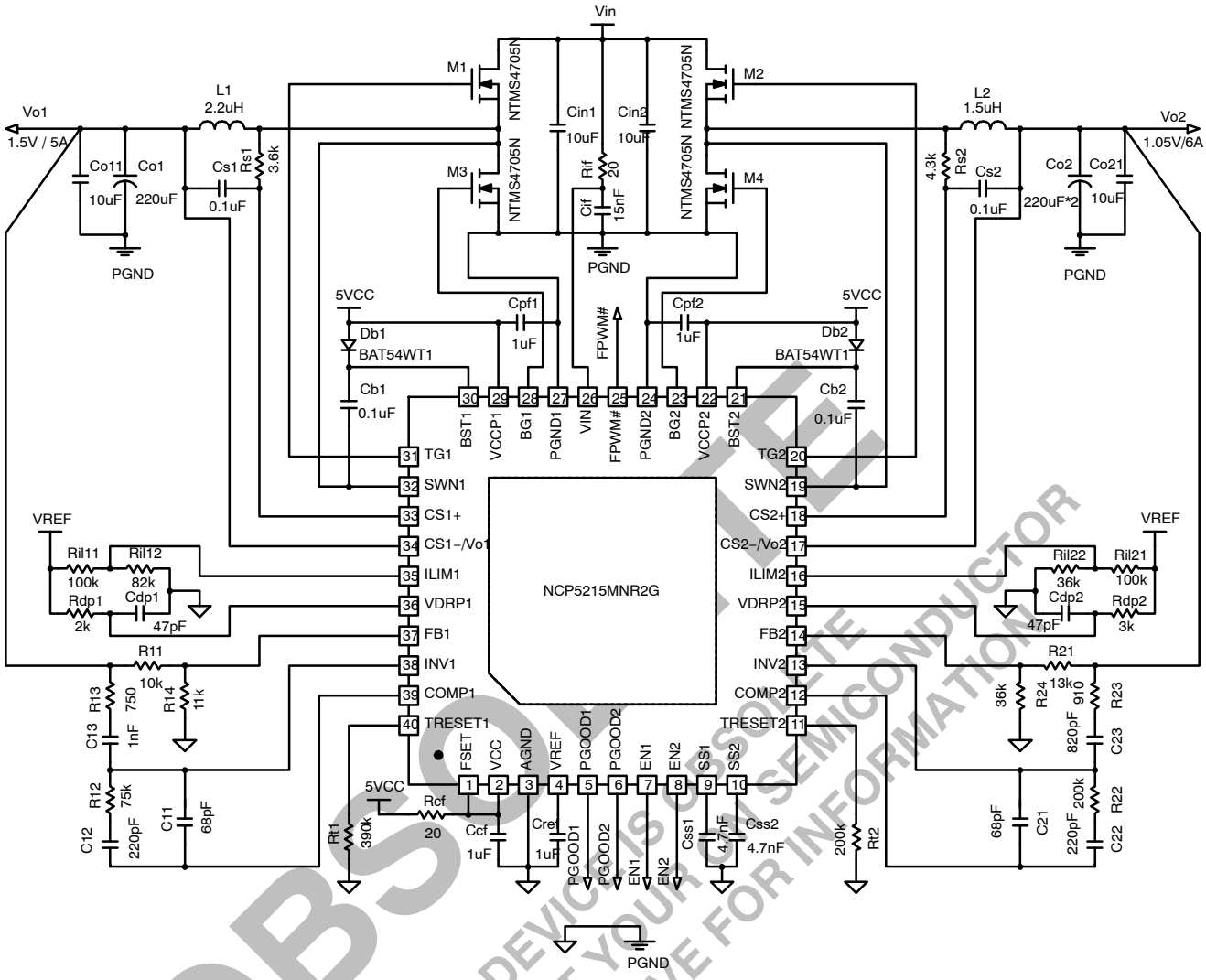


**Figure 35. Typical Application Schematic Diagram**

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**Table 2. BILL OF MATERIALS FOR THE TYPICAL APPLICATION**

| Item | PCS | Part Reference | Description | Value | Package | Part Number | Manufacturer |
|---|---|---|---|---|---|---|---|
| 1 | 1 | IC1 | NCP5215 | | QFN40 | NCP5215MNR2G | ON Semiconductor |
| 2 | 4 | M1, M2, M3, M4 | Power MOSFET 30 V, 12 A, Single N−Channel SO−8 | | SO8 | NTMS4705N | ON Semiconductor |
| 3 | 2 | Db1, Db2 | Schottky Diode, 30V | | SC70 | BAT54WT1G | ON Semiconductor |
| 4 | 2 | Cdp1, Cdp2 | MLCC Cap 50V, ±5%, Char: COG | 47pF | 0603 | ECJ1VB1H470J | Panasonic |
| | | | | | | C1608C0G1H470J | TDK |
| 5 | 2 | C11, C22 | MLCC Cap 50V, ±5%, Char: COG | 68pF | 0603 | ECJ1VB1H680J | Panasonic |
| | | | | | | C1608C0G1H680J | TDK |
| 6 | 2 | C12, C22 | MLCC Cap 50V, ±5%, Char: COG | 220pF | 0603 | ECJ1VC1H221J | Panasonic |
| | | | | | | C1608C0G1H221J | TDK |
| 7 | 1 | C23 | MLCC Cap 50V, ±5%, Char: COG | 820pF | 0603 | ECJ1VC1H821J | Panasonic |
| | | | | | | C1608C0G1H821J | TDK |
| 8 | 1 | C13 | MLCC Cap 50V, ±5%, Char: COG | 1000pF | 0603 | ECJ1VC1H102J | Panasonic |
| | | | | | | C1608C0G1H102J | TDK |
| 9 | 2 | CSS1, CSS2 | MLCC Cap 50V, ±10%, Char: X7R | 4700pF | 0603 | ECJ1VB1H472K | Panasonic |
| | | | | | | C1608X7R1H472K | TDK |
| 10 | 1 | CIF | MLCC Cap 50V, ±10%, Char: X7R | 15nF | 0603 | ECJ1VB1H153K | Panasonic |
| | | | | | | C1608X7R1H153K | TDK |
| 11 | 4 | Cb1, Cb2, Cs1, Cs2 | MLCC Cap 16V, ±10%, Char: X7R | 0.1μF | 0603 | ECJ1VB1C104K | Panasonic |
| | | | | | | C1608X7R1H104K | TDK |
| 12 | 4 | Ccf, Cpf1, Cpf2, Cref | MLCC Cap 25V, ±10%, Char: X5R | 1μF | 0805 | ECJ2FB1E105K | Panasonic |
| | | | | | | C3216X5R1H105K | TDK |
| 13 | 2 | Co11, Co21 | MLCC Cap 10V, ±20%, Char: X7R | 10μF | 0805 | ECJ3YB1C106M | Panasonic |
| | | | | | | C3216X7R1C106M | TDK |
| 14 | 2 | CIN1, CIN2 | MLCC Cap 25V, ±20%, Char: X7R | 10μF | 1812 | C4532X7R1E106M | TDK |
| 15 | 3 | Co1, Co2 (x2) | SP−Cap/Polymer Aluminum Capacitors, 22 μF, 2 V, ESR = 12 mΩ | 220μF | 7343 | EEFUD0D221XR | Panasonic |
| 16 | 2 | Rcf, Rif | Thick Film Chip Resistors, Power Rating 0.1W, Tol: ±1% | 20Ω | 0603 | ERJ3EKF20R0V | Panasonic |
| 17 | 1 | R13 | Thick Film Chip Resistors, Power Rating 0.1W, Tol: ±1% | 750Ω | 0603 | ERJ3EKF7500V | Panasonic |
| 18 | 1 | R23 | Thick Film Chip Resistors, Power Rating 0.1W, Tol: ±1% | 910Ω | 0603 | ERJ3EKF9100V | Panasonic |
| 19 | 1 | Rdp1 | Thick Film Chip Resistors, Power Rating 0.1W, Tol: ±1% | 2kΩ | 0603 | ERJ3EKF2001V | Panasonic |
| 20 | 1 | Rdp2 | Thick Film Chip Resistors, Power Rating 0.1W, Tol: ±1% | 3kΩ | 0603 | ERJ3EKF3001V | Panasonic |
| 21 | 1 | RS1 | Thick Film Chip Resistors, Power Rating 0.1W, Tol: ±1% | 3.6kΩ | 0603 | ERJ3EKF3601V | Panasonic |
| 22 | 1 | RS2 | Thick Film Chip Resistors, Power Rating 0.1W, Tol: ±1% | 4.3kΩ | 0603 | ERJ3EKF4301V | Panasonic |
| 23 | 1 | R11 | Thick Film Chip Resistors, Power Rating 0.1W, Tol: ±1% | 10kΩ | 0603 | ERJ3EKF1002V | Panasonic |

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| Item | PCS | Part Reference | Description | Value | Package | Part Number | Manufacturer |
|---|---|---|---|---|---|---|---|
| 24 | 1 | R14 | Thick Film Chip Resistors, Power Rating 0.1W, Tol: ±1% | 11kΩ | 0603 | ERJ3EKF1102V | Panasonic |
| 25 | 1 | R21 | Thick Film Chip Resistors, Power Rating 0.1W, Tol: ±1% | 13kΩ | 0603 | ERJ3EKF1302V | Panasonic |
| 26 | 2 | R24, Ril22 | Thick Film Chip Resistors, Power Rating 0.1W, Tol: ±1% | 36kΩ | 0603 | ERJ3EKF3602V | Panasonic |
| 27 | 1 | R12 | Thick Film Chip Resistors, Power Rating 0.1W, Tol: ±1% | 75kΩ | 0603 | ERJ3EKF7502V | Panasonic |
| 28 | 1 | Ril12 | Thick Film Chip Resistors, Power Rating 0.1W, Tol: ±1% | 82kΩ | 0603 | ERJ3EKF8202V | Panasonic |
| 29 | 2 | Ril11, Ril21 | Thick Film Chip Resistors, Power Rating 0.1W, Tol: ±1% | 100kΩ | 0603 | ERJ3EKF1003V | Panasonic |
| 30 | 2 | R22, Rt2 | Thick Film Chip Resistors, Power Rating 0.1W, Tol: ±1% | 200kΩ | 0603 | ERJ3EKF2003V | Panasonic |
| 31 | 1 | Rt1 | Thick Film Chip Resistors, Power Rating 0.1W, Tol: ±1% | 390kΩ | 0603 | ERJ3EKF3903V | Panasonic |
| 32 | 1 | L1 | Power Choke Coil, DCR = 7.0mΩ, IDC = 12A, ISAT = 27A | 2.2μH | | PCMC104T−2R2MN | Cyntec |
| 33 | 1 | L2 | Power Choke Coil, DCR = 4.2mΩ, IDC = 16A, ISAT = 33A | 1.5μH | | PCMC104T−1R5MN | Cyntec |

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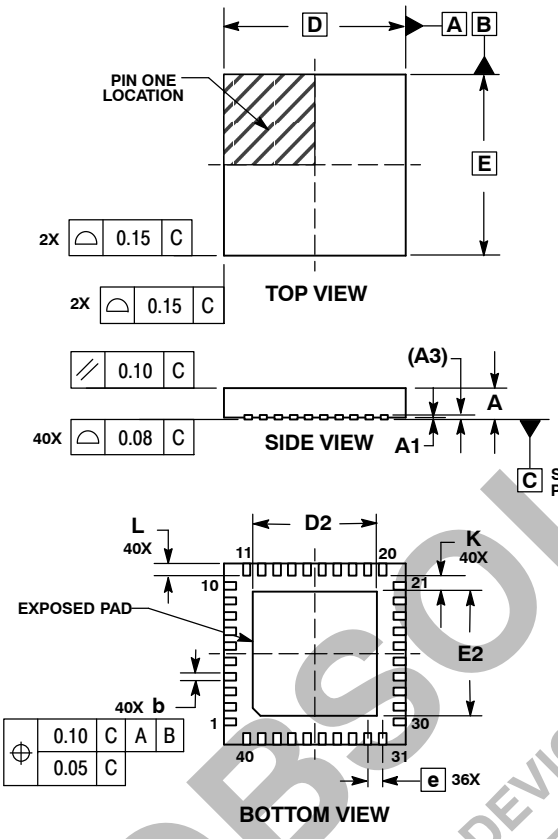
## PACKAGE DIMENSIONS

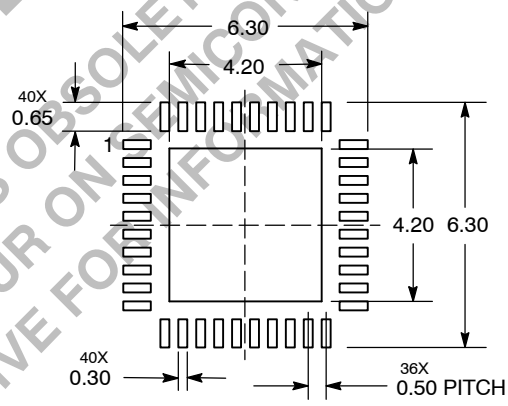
**QFN40 6x6, 0.5P**
**MN SUFFIX**
CASE 488AR−01
ISSUE A




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.18 | 0.30 |
| D | 6.00 BSC | |
| D2 | 4.00 | 4.20 |
| E | 6.00 BSC | |
| E2 | 4.00 | 4.20 |
| e | 0.50 BSC | |
| L | 0.30 | 0.50 |
| K | 0.20 | --- |

**SOLDERING FOOTPRINT***




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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