

SN74AVC2T244 2-Bit Unidirectional Voltage-level Translator

1 Features

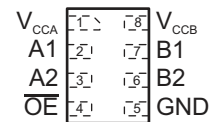
- Wide Operating V_{CC} Range of 0.9 V to 3.6 V
- Low Static-Power Consumption, 6- μ A Max I_{CC}
- Output Enable Feature Allows User to Disable Outputs to Reduce Power Consumption
- \pm 24-mA Output Drive at 3.0 V
- I_{off} Supports Partial Power-Down-Mode Operation
- Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at Input
- Maximum Data Rates
 - 380 Mbps (1.8-V to 3.3-V Translation)
 - 200 Mbps (<1.8-V to 3.3-V Translation)
 - 200 Mbps (Translate to 2.5 V or 1.8 V)
 - 150 Mbps (Translate to 1.5 V)
 - 100 Mbps (Translate to 1.2 V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 5000-V Human-Body Model (A114-A)

2 Applications

- Handset, Smartphone, Tablet, Server

3 Description

This 2-bit unidirectional translator uses two separate configurable power-supply rails. The A port is designed to track V_{CCA} . V_{CCA} accepts any supply voltage from 0.9 V to 3.6 V. The B port is designed to track V_{CCB} . V_{CCB} accepts any supply voltage from 0.9 V to 3.6 V. This allows for low-voltage translation between 0.9-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V and 3.6-V voltage nodes. For the SN74AVC2T244, when the output-enable (\overline{OE}) input is high, all outputs are placed in the high-impedance state. The SN74AVC2T244 is designed so that the \overline{OE} input circuit is referenced to V_{CCA} . This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



DQE and DQM Packages 8 Pin X2SON (Top View)



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (September 2011) to Revision C (March 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Updated the title of the data sheet.....	1
• Deleted <i>Ordering Information</i> table, see POA at the end of the datasheet.	1

5 Pin Configuration and Functions

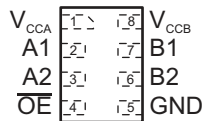


Figure 5-1. DQE and DQM Packages 8 Pin X2SON (Top View)

Table 5-1. Pin Functions

PIN	FUNCTION
VCCA	Input Port DC Power Supply
VCCB	Output Port DC Power Supply
GND	Ground
A _n	Input Port
B _n	Output Port
OE	Output Enable

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT	
Voltage	DC Supply voltage, V_{CCA} V_{CCB}	-0.5	4.6	V	
	DC Input voltage, V_I	A_n	-0.5	4.6	V
	Control Input, V_C	\overline{OE}	-0.5	4.6	V
	DC Output voltage, V_O , $V_{CCA} = V_{CCB} = 0$	(Power Down) B_n	-0.5	4.6	V
		(Active Mode) B_n	-0.5	4.6	
	3-State Mode B_n	-0.5	4.6		
	DC Input Diode current, I_{IK}	$V_I < GND$	-20	mA	
	DC Output Diode current, I_{OK}	$V_O < GND$	-50	mA	
	DC Output Source/Sink current, I_O		± 50	mA	
	DC Supply current per supply pin, I_{CCA} , I_{CCB}		± 100	mA	
I_{GND}	DC Ground current per ground pin		± 100	mA	
T_{stg}	Storage temperature range	-65	150	°C	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Recommended Operating Conditions

		MIN	MAX	UNIT	
V_{CCA} , V_{CCB}	Positive DC Supply voltage	0.9	3.6	V	
V_I	Bus input voltage	GND	3.6	V	
V_I	Input voltage	GND	3.6	V	
V_C	Control input	\overline{OE}	GND	3.6	V
V_O	Bus output voltage	(Power Down Mode) B_n	GND	3.6	V
		(Active Mode) B_n	GND	V_{CCB}	V
		3-State Mode B_n	GND	3.6	V
T_A	Operating free-air temperature	-40	85	°C	
$\Delta t/\Delta v$	Input transition rise or fall rate V_I from 30% to 70% of V_{CC} ; $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	0	10	nS	

6.3 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER ^{(1) (2)}		TEST CONDITIONS	V _{CCA} (V)	V _{CCB} (V)	–40°C to 85°C		UNIT
					MIN	MAX	
V _{IH}	Input HIGH Voltage (An, \overline{OE})		2.7 – 3.6	0.9 – 3.6	2.0	–	V
			2.3 – 2.7		1.6	–	
			1.4 – 2.3		$0.65 \times V_{CCA}$	–	
			0.9 – 1.4		$0.9 \times V_{CCA}$	–	
V _{IL}	Input LOW voltage (An, \overline{OE})		2.7 – 3.6	0.9 – 3.6	–	0.8	V
			2.3 – 2.7		–	0.7	
			1.4 – 2.3		–	$0.35 \times V_{CCA}$	
			0.9 – 1.5		–	$0.1 \times V_{CCA}$	
V _{OH}	Output HIGH voltage	I _{OH} = –100 μ A; V _I = V _H	0.9 – 3.6	0.9 – 3.6	V _{CCB} – 0.2	–	V
		I _{OH} = –0.5 mA; V _I = V _H	0.9	0.9	$0.75 \times V_{CCB}$	–	
		I _{OH} = –2 mA; V _I = V _H	1.4	1.4	1.05	–	
		I _{OH} = –6 mA; V _I = V _H	1.65	1.65	1.25	–	
			2.3	2.3	2.0	–	
		I _{OH} = –12 mA; V _I = V _H	2.3	2.3	1.8	–	
			2.7	2.7	2.2	–	
		I _{OH} = –18 mA; V _I = V _H	2.3	2.3	1.7	–	
I _{OH} = –24 mA; V _I = V _H	3.0	3.0	2.4	–			
V _{OL}	Output LOW voltage	I _{OH} = 100 μ A; V _I = V _H	0.9 – 3.6	0.9 – 3.6	–	0.2	V
		I _{OH} = 0.5 mA; V _I = V _H	1.1	1.1	–	0.3	
		I _{OH} = 2 mA; V _I = V _H	1.4	1.4	–	0.35	
		I _{OH} = 6 mA; V _I = V _H	1.65	1.65	–	0.3	
			2.3	2.3	–	0.4	
		I _{OH} = 12 mA; V _I = V _H	2.7	2.7	–	0.4	
			2.3	2.3	–	0.6	
		I _{OH} = 24 mA; V _I = V _H	3.0	3.0	–	0.4	
I _I	Input Leakage Current	V _I = V _{CCA} or GND	0.9 – 3.6	0.9 – 3.6	–1.0	1.5	μ A
I _{OFF}	Power-Off Leakage Current	$\overline{OE} = 0V$	0	0.9 – 3.6	–1.0	1.3	μ A
			0.9 – 3.6	0	–1.0	1.5	
I _{CCA}	Quiescent Supply Current	V _I = V _{CCA} or GND; I _O = 0	0.9 – 3.6	0.9 – 3.6	–	3.0	μ A
I _{CCB}	Quiescent Supply Current	V _I = V _{CCA} or GND; I _O = 0	0.9 – 3.6	0.9 – 3.6	–	3.0	μ A
I _{CCA} + I _{CCB}	Quiescent Supply Current	V _I = V _{CCA} or GND; I _O = 0	0.9 – 3.6	0.9 – 3.6	–	6.0	μ A
ΔI_{CCA}	Increase in I _{CC} per Input Voltage, Other inputs at V _{CCA} or GND	V _I = V _{CCA} – 0.3 V; V _I = V _{CCA} or GND	3.6	3.6	–	5.0	μ A

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER ^{(1) (2)}		TEST CONDITIONS	V _{CCA} (V)	V _{CCB} (V)	–40°C to 85°C		UNIT
					MIN	MAX	
ΔI_{CCB}	Increase in I _{CC} per Input Voltage, Other inputs at V _{CCA} or GND	V _I = V _{CCA} – 0.3 V; V _I = V _{CCA} or GND	3.6	3.6	–	5.0	μA
I _{oz}	I/O Tri-State Output Leakage Current	TA = 25°C, \overline{OE} = 0 V	0.9 – 3.6	0.9 – 3.6	–1.0	1.0	μA

 (1) V_{CCO} is the V_{CC} associated with the output port.

 (2) V_{CCI} is the V_{CC} associated with the input port.

6.4 AC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		V _{CCA} (V)	V _{CCB} (V)	MIN	MAX	UNIT
t _{PLH} , t _{PHL}	Propagation Delay, A _n to B _n	0.9 – 3.6	0.9 – 3.6		20	nS
		1.2 – 3.6	1.2 – 3.6		7	
		1.8 – 3.6	1.8 – 3.6		3.5	
t _{PZH} , t _{PZL}	Output Enable, \overline{OE} to B _n	0.9 – 3.6	0.9 – 3.6		23	nS
		1.2 – 3.6	1.2 – 3.6		6.5	
		1.8 – 3.6	1.8 – 3.6		4.1	
t _{PHZ} , t _{PLZ}	Output Disable, \overline{OE} to B _n	0.9 – 3.6	0.9 – 3.6		17	nS
		1.2 – 3.6	1.2 – 3.6		7	
		1.8 – 3.6	1.8 – 3.6		4.3	
t _{OSHL} , t _{OSLH}	Output to Output Skew, Time	0.9 – 3.6	0.9 – 3.6		0.15	nS
		1.2 – 3.6	1.2 – 3.6		0.15	
		1.8 – 3.6	1.8 – 3.6		0.15	

Table 6-1. Capacitance

(2)	PARAMETER	TEST CONDITIONS	TYP ⁽¹⁾	UNIT
C _{IN}	Control Pin Input Capacitance	V _{CCA} = V _{CCB} = 3.3 V, V _I = 0 V or V _{CCA/B}	3.5	pF
C _{I/O}	I/O Pin Input capacitance	V _{CCA} = V _{CCB} = 3.3 V, V _I = 0 V or V _{CCA/B}	5.0	pF
C _{PD}	Power Dissipation Capacitance	V _{CCA} = V _{CCB} = 3.3 V, V _I = 0 V or V _{CCA/B} , f = 10 MHz	33	pF

(1) Typical values are at TA = +25°C.

 (2) C_{PD} is defined as the value of the IC's equivalent capacitance from which the operating current can be calculated from: I_{CC(operating)} ≈ C_{PD} × V_{CC} × f_{IN} × N_{SW} where I_{CC} = I_{CCA} + I_{CCB} and N_{SW} = total number of outputs switching.

7 Device and Documentation Support

7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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7.3 Trademarks

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7.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AVC2T244DQER	ACTIVE	X2SON	DQE	8	5000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	VA	Samples
SN74AVC2T244DQMR	ACTIVE	X2SON	DQM	8	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	VA	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AVC2T244DQER	X2SON	DQE	8	5000	180.0	8.4	1.2	1.6	0.55	4.0	8.0	Q1
SN74AVC2T244DQMR	X2SON	DQM	8	3000	180.0	8.4	1.57	2.21	0.59	4.0	8.0	Q1

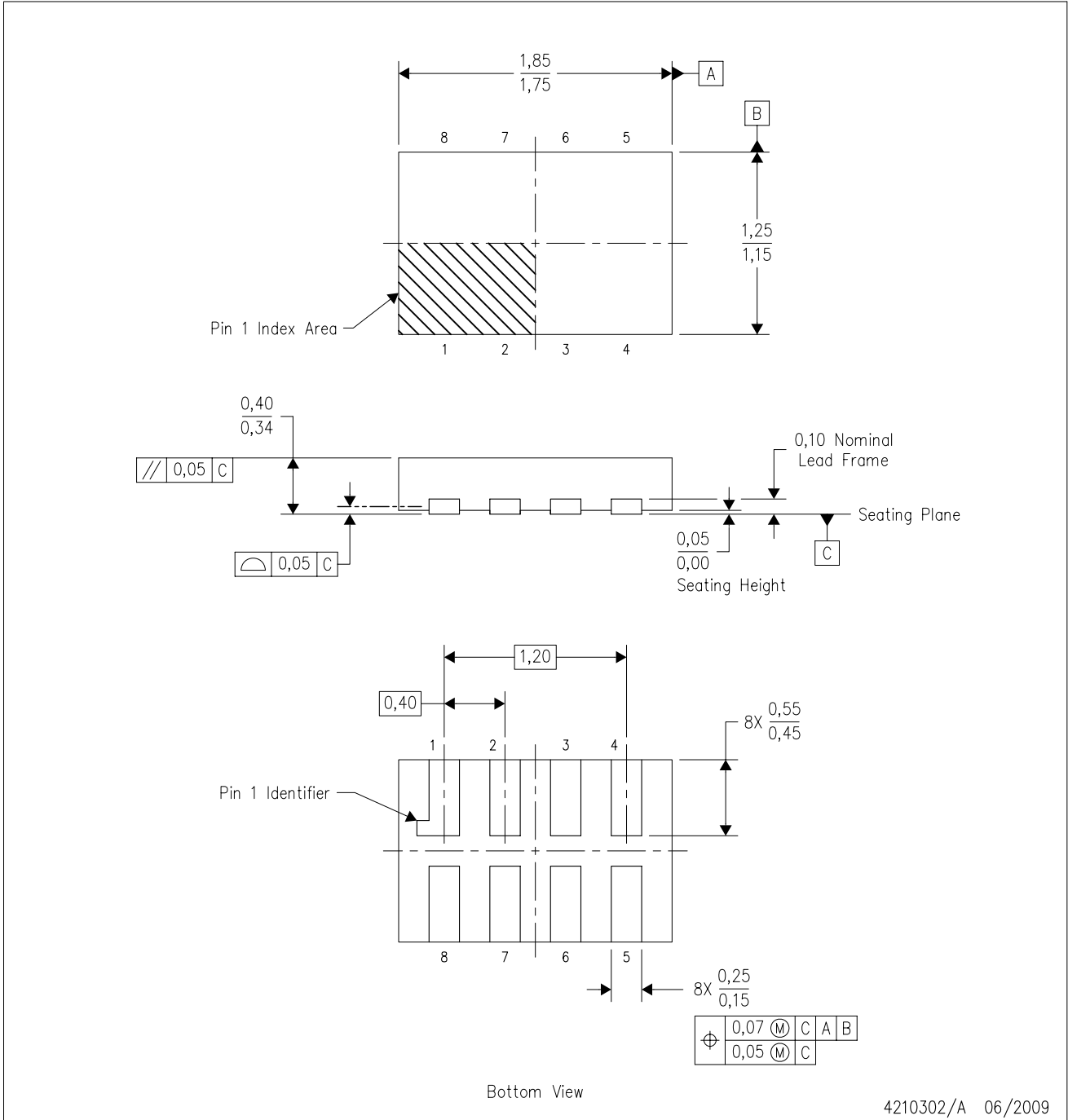
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AVC2T244DQER	X2SON	DQE	8	5000	202.0	201.0	28.0
SN74AVC2T244DQMR	X2SON	DQM	8	3000	202.0	201.0	28.0

DQM (R-PX2SON-N8)

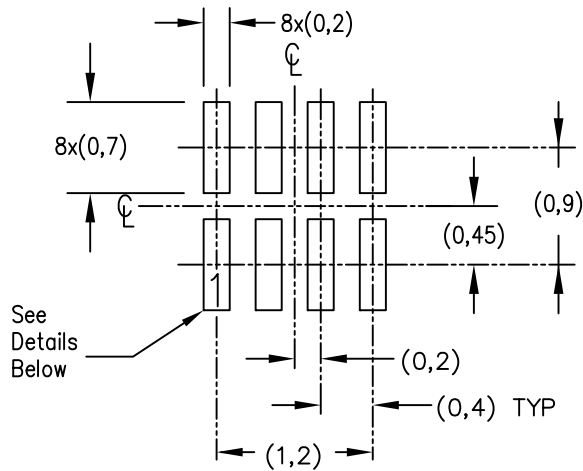
PLASTIC SMALL OUTLINE NO-LEAD



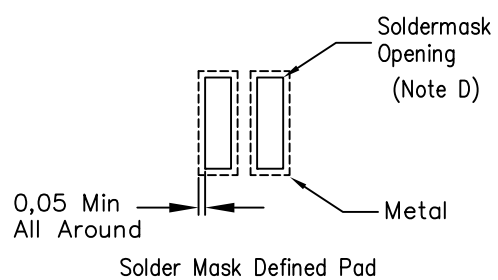
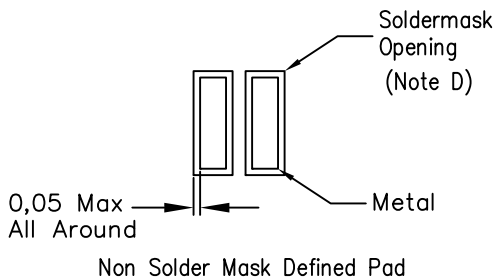
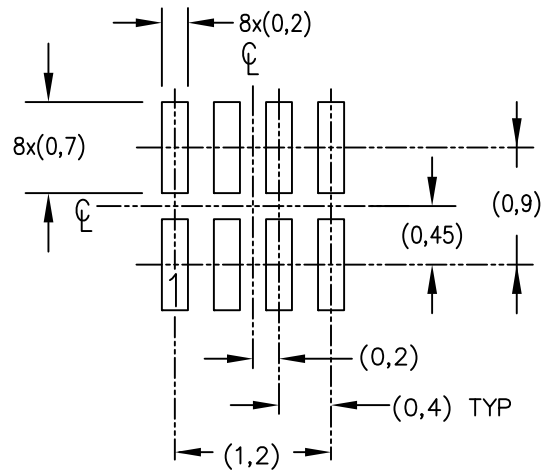
4210302/A 06/2009

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. SON (Small Outline No-Lead) package configuration.

Example Board Layout



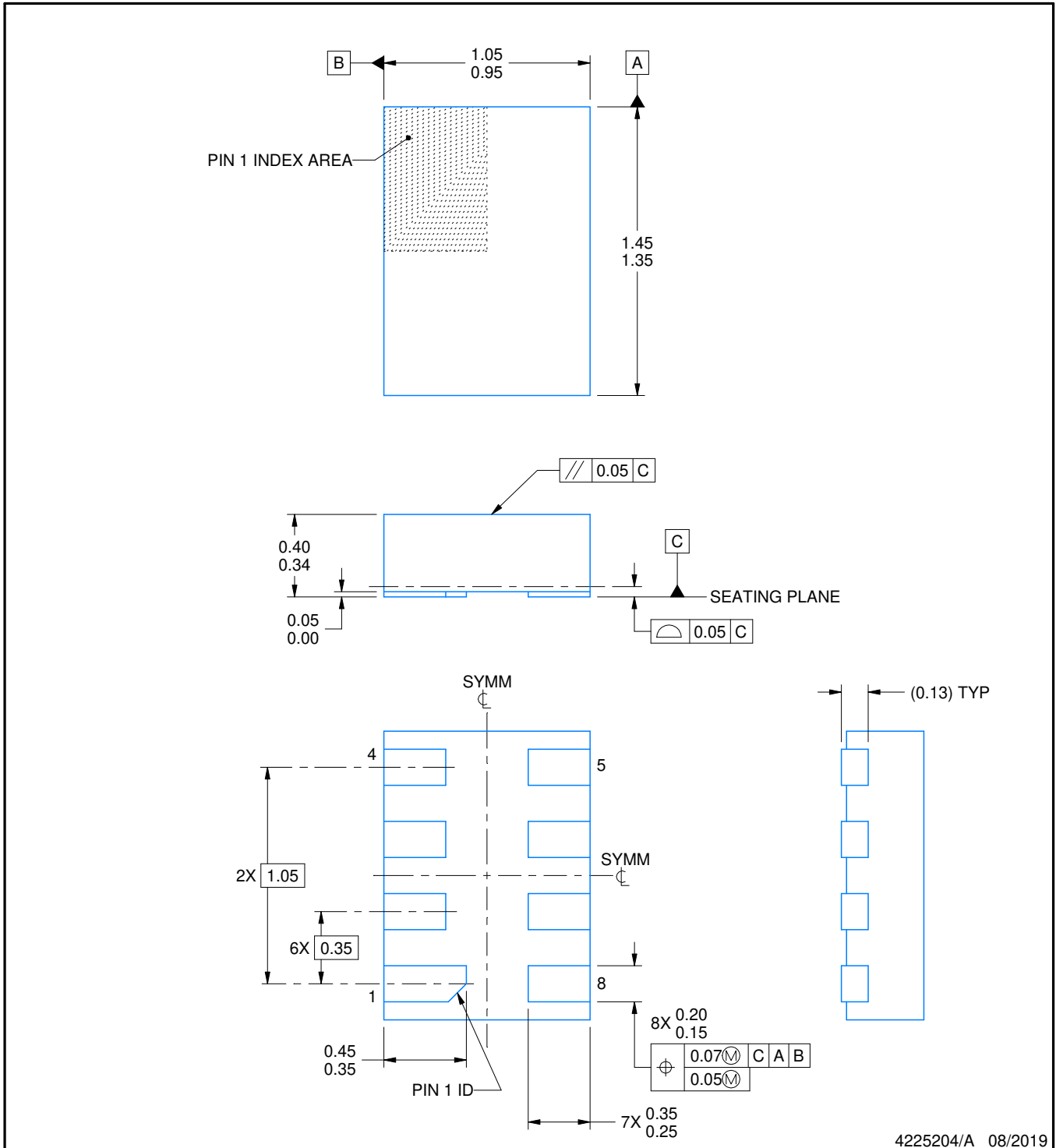
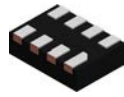
Example Stencil Design
0.1mm Thick Stencil
(Note C)



Solder Mask Details

4218746/A 07/13

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - D. Customers should contact their board fabrication site for recommended solder mask tolerances.



NOTES:

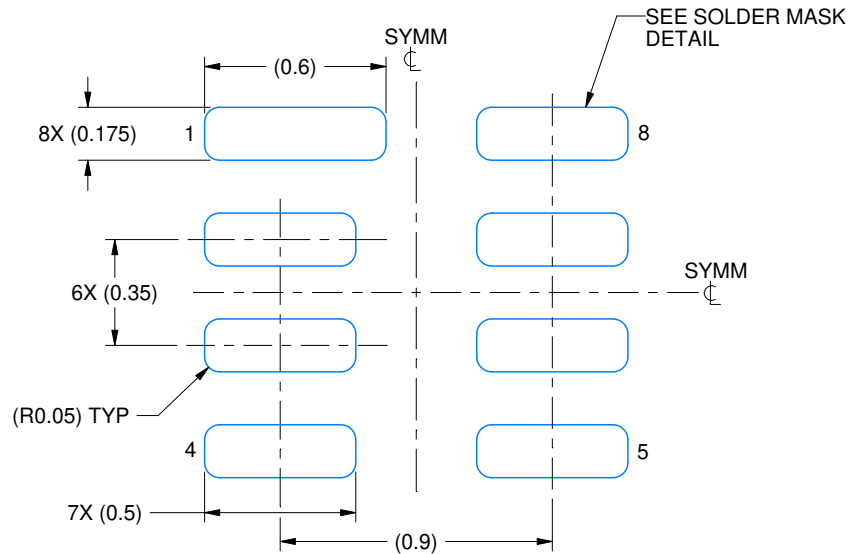
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package complies to JEDEC MO-287 variation X2EAF.

EXAMPLE BOARD LAYOUT

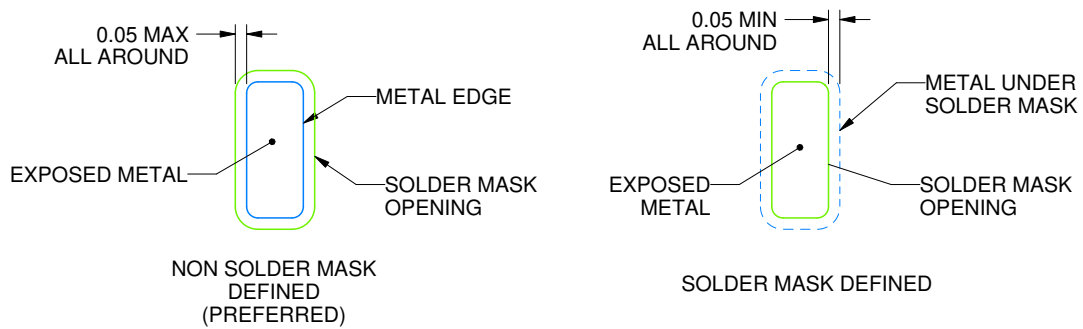
DQE0008A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X



SOLDER MASK DETAILS

4225204/A 08/2019

NOTES: (continued)

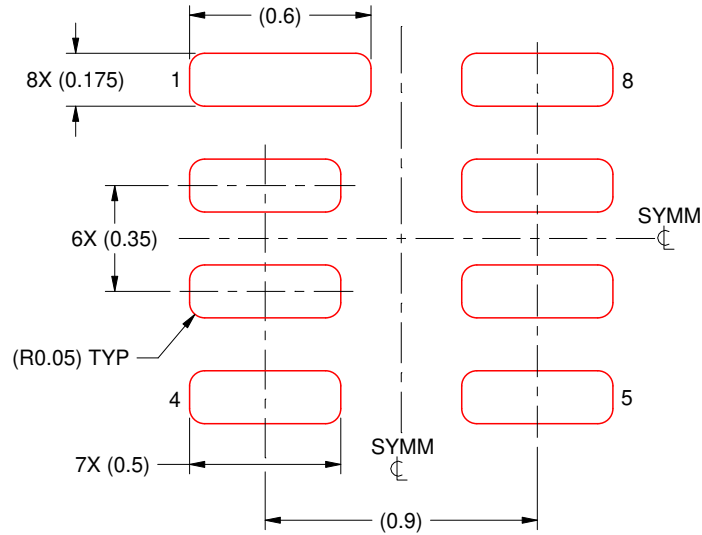
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DQE0008A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 MM THICK STENCIL
SCALE: 40X

4225204/A 08/2019

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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