DOC-0508-010, REV A

TWR-S12G128

Demonstration Board for Freescale MC9S12G128 Microcontroller

USER GUIDE

Web Site: www.axman.com

Support: support@axman.com

CONTENTS

FIGURES

REVISION

Date	Rev	Comments
June 2, 2010	A	Initial Release

CAUTIONARY NOTES

1) Electrostatic Discharge (ESD) prevention measures should be used when handling this product. ESD damage is not a warranty repair item.

2) Axiom Manufacturing does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under patent rights or the rights of others.

3) EMC Information on the TWR-S12G128 board:

   a) This product as shipped from the factory with associated power supplies and cables, has been verified to meet with requirements of CE and the FCC as a CLASS A product.

   b) This product is designed and intended for use as a development platform for hardware or software in an educational or professional laboratory.

   c) In a domestic environment, this product may cause radio interference in which case the user may be required to take adequate prevention measures.

   d) Attaching additional wiring to this product or modifying the products operation from the factory default as shipped may effect its performance and cause interference with nearby electronic equipment. If such interference is detected, suitable mitigating measures should be taken.

TERMINOLOGY

This development module utilizes option select jumpers to configure default board operation. Terminology for application of the option jumpers is as follows:

Jumper – a plastic shunt that connects 2 terminals electrically

Jumper on, in, or installed = jumper is a plastic shunt that fits across 2 pins and the shunt is installed so that the 2 pins are connected with the shunt.

Jumper off, out, or idle = jumper or shunt is installed so that only 1 pin holds the shunt, no 2 pins are connected, or jumper is removed. It is recommended that the jumpers be placed idle by installing on 1 pin so they will not be lost.

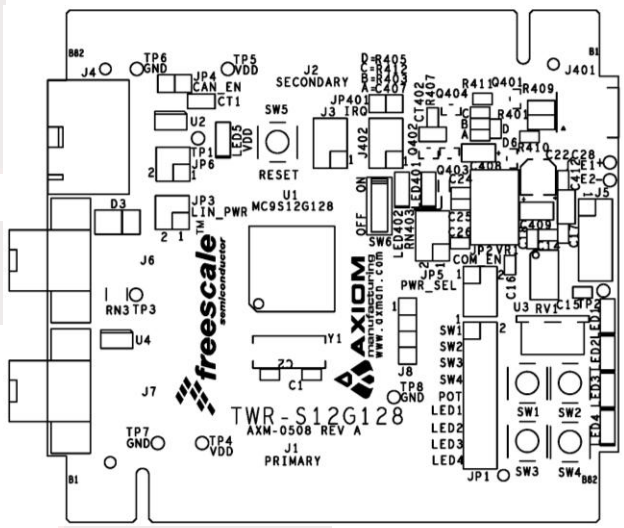
Cut-Trace – a circuit trace connection between component pads. The circuit trace may be cut using a knife to break the default connection. To reconnect the circuit, simply install a suitably sized 0-ohm resistor or attach a wire across the pads.

Signal names followed by an asterisk (*) denote active-low signals.

FEATURES

The TWR-S12G128 is a demonstration board for the MC9S12G128 microcontroller; an automotive, 16-bit microcontroller focused on low-cost, high-performance in a low pin-count device. The MC9S12G128 provides16-bit wide accesses, without wait states, for all peripherals and memories. The MC9S12G128 targets automotive applications requiring CAN or LIN/J2602 communications. Examples include body controllers, occupant detection, etc…

The board is designed to interface to the Freescale Tower System, a modular development platform which aids in rapid prototyping and tool-reuse. An integrated Open-Source BDM, software tools, and examples provided with the development board make application development and debug quick and easy. All MCU signals are available on one or both edge connectors.



- MC9S12G128, 100 LQFP
  - 128K Bytes Flash
  - 4096 Bytes EEPROM
  - 8192 Bytes RAM
  - 25MHz Bus Frequency
  - Internal Oscillator
  - SCI, SPI, MSCAN
- Integrated Open Source BDM (OSBDM)
- BDM_PORT header for external BDM cable support
- 1 ea. High-Speed CAN Physical Layer Transceiver
- 1 ea, Enhanced LIN Physical Layer Transceiver
- RS-232 Serial Data Physical Layer Transceiver
- On-board +5V regulator
- Power input from OSBDM, Tower System, or input vias at E1/E2
- Power Input Selection Jumpers
  - Power input from USB-BDM
  - Power input from on-board regulator
  - Power input from Tower System edge connector
- User Peripherals
  - 4 User Push Button Switches
  - 4 User LED Indicators
  - 5K ohm POT w /LP Filter
- User Option Jumpers to disconnect Peripherals
- Connectors
  - BDM_PORT Connector for External BDM Cable
  - USB mini-AB Connector
  - 2x5, 0.1” ctr, RS-232 Header
  - 1x4, 4.2mm, Molex CAN Cable Connector
  - 2x2, 4.2mm, Molex LIN Cable Connector

Specifications:
Board Size 3.55” x 3.20” overall
Power Input: +5V from USB connector or from Tower System
NOTE: LIN functionality requires +12V on LIN +V input or +12V at E1/E2 input.

MEMORY MAP

Figure 1 below shows the target device memory map. Refer to the MC9S12G128 Reference Manual (RM) for further information.

Figure 1: Memory Map

Address	Module	Size (Bytes)
0x0000–0x0009	PIM (port integration module)	10
0x000A–0x000B	MMC (memory map control)	2
0x000C–0x000D	PIM (port integration module)	2
0x000E–0x000F	Reserved	2
0x0010–0x0017	MMC (memory map control)	8
0x0018–0x0019	Reserved	2
0x001A–0x001B	Device ID register	2
0x001C–0x001F	PIM (port integration module)	4
0x0020–0x002F	DBG (debug module)	16
0x0030–0x0033	Reserved	4
0x0034–0x003F	CPMU (clock and power management)	12
0x0040–0x006F	TIM0 (timer module)	48
0x0070–0x009F	ATD (analog-to-digital converter, 10 bit, 8-channel)	48
0x00A0–0x00C7	PWM (pulse-width modulator)	40
0x00C8–0x00CF	SCI0 (serial communications interface)	8
0x00D0–0x00D7		8
0x00D8–0x00DF		8
0x00E0–0x00E7	Reserved	8
0x00E8–0x00EF	SCI2 (serial communications interface)	8
0x00F0–0x00F7F	SPI1 (serial peripheral interface)	8
0x00F8–0x00FF	SPI1 (serial peripheral interface)	8
0x0100–0x0113	FTMRC control registers	20
0x0114–0x011F	Reserved	12
0x0120	INT (interrupt module)	1
0x0121–0x013F	Reserved	31
0x0140–0x017F	CAN	64
0x0180–0x023F	Reserved	192
0x0240–0x027F	PIM (port integration module)	64
0x0280–0x02EF	Reserved	112
0x02F0–0x02FF	CPMU (clock and power management)	16
0x0300–0x03BF	Reserved	192
0x03C0–0x03C7	DAC0 (digital to analog converter)	8
0x03C8–0x03CF	DAC1 (digital to analog converter)	8
0x03D0–0x03FF	Reserved	48

SOFTWARE DEVELOPMENT

Software development requires the use of a compiler or an assembler supporting the HCS12(X) instruction set and a host PC running a debug interface. CodeWarrior Development Studio is supplied with this board for application development and debug. Refer to the supporting CodeWarrior documentation for details on use and capabilities.

NOTE:

OSBDM is not functional at this time and will provide power to the board only. Updated OSBDM firmware is expected in August 2010 to support the HCS12 target. An external BDM is required to program and debug the target MCU.

DEVELOPMENT SUPPORT

Application development and debug for the target TWR-S12 board is supported through the Open-Source Background Debug Mode (OSBDM) interface or an external BDM interface connector. The OSBDM is fully supported in CodeWarrior and provides direct, non-intrusive access to the target device internals. While in BDM mode, no internal resources are used. Code stepping and break-points are fully supported.

Connection between a host PC and the target device is provided via a mini-B, USB connector. The OSBDM is capable of providing power to the target board eliminating the need for external power. Please note that power supplied by the OSBDM is limited by the USB specification. When powered through the OSBDM, total current draw, including the OSBDM, TWR-S12 board, and Tower System must remain less that 500mA. Otherwise, the USB bus will cause the host PC to disconnect the board. Damage to the host PC, target board, or Tower System may result if this current limit is violated.

NOTE:

OSBDM is not functional at this time and will provide power to the board only. Updated OSBDM firmware is expected in August 2010 to support the HCS12 target. An external BDM is required to program and debug the target MCU.

CAUTION:

When powered from the USB bus, do not exceed the 500mA maximum allowable current drain. Damage to the target board or host PC may result

OSBDM Bootloader

The OSBDM is pre-programmed with a bootloader application to allow field updates. The USB bootloader communicates with a GUI application running on a host PC. The GUI application allows the user to update OSBDM firmware easily and quickly. Option jumper JP401 enables the bootloader at startup. This option header is not populated in default configuration. Refer to Freescale Application Note AN3561 for details on using the GUI application and bootloader. The application note may be found at www.freescale.com or at www.axman.com/support.

BDM_PORT Header

A compatible HCS12 BDM cable can also be attached to the 6-pin BDM interface header at J3. This header allows the use of external programming/debug cables. Refer to the external programming/debug cable documentation for details on use. The figure below shows the pin-out for the DEBUG header.

NOTE:

OSBDM is not functional at this time and will provide power to the board only. Updated OSBDM firmware is expected in August 2010 to support the HCS12 target. An external BDM is required to program and debug the target MCU.

Figure 2: BDM_PORT Header

J400

BKGD	1	2	GND
	3	4	RESET*
	5	6	VDD

See the associated RM for complete DEBUG documentation

NOTE: This header is not installed in default configuration.

POWER

The TWR-S12 board may be powered from the OSBDM, from the Tower System, from the LIN +V input, or 2 input vias at E1 & E2. The LIN +V input accepts +12V from the LIN bus and uses an on-board regulator to create the board operating voltage. Input vias at E1 & E2 allow connecting external power to the board if desired. An on-board regulator is used to create the board operating voltage from this input.

Use of the on-board regulator requires input voltage between +7.V and +27V. However, input voltage should be kept as low as possible to reduce device self-heating.

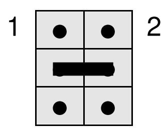
> **CAUTION:**
>
> This boards does not apply reverse polarity protection on inputs E1 & E2. Polarity for each input is clearly marked. Reverse input polarity will damage the board.

Power Select

Option headers PWR_SEL selects the input power source for the target board. When powered from the Tower System, the OSBDM voltage output is disabled.

Figure 3: PWR_SEL Option Header

JP5
PWR_SEL



Select TWR voltage input
Select OSBDM voltage input (default)
Select on-board regulator input

RESET SWITCH

The RESET switch applies an asynchronous RESET input to the MCU. The RESET switch is connected directly to the RESET* input on the MCU. Pressing the RESET switch applies a low voltage level to the RESET* input. A pull-up bias resistor allows normal MCU operation.

LOW VOLTAGE RESET

The MC9S12G128 applies a Power-On Reset (POR) circuit and an internal Low Voltage Reset (LVR) circuit to ensure proper device operation. The POR circuit holds the MCU in reset until applied voltage reaches an appropriate level. The LVR forces the device into reset if input voltage falls too low, protecting against brown-out conditions. A user configurable Low-Voltage Detect (LVD) with interrupt output is also available. Consult the MC9S12G128 reference manual for details of POR, LVR, and LVD operation.

TIMING

The TWR-S12G128 internal timing source is active from RESET by default. An external 8MHz crystal oscillator, configured for low-power operation, is also installed. Refer to the target device RM for details on selecting and configuring the desired timing source.

COMMUNICATIONS

Communications options for the TWR-S12G128 include serial RS-232, LIN, and CAN. Serial RS-232 communications is supported through a RS-232 physical layer device (PHY) and a 2x5 pin header. A high-speed, enhanced, LIN PHY provides LIN bus communications through a 2x2 Molex connector (pn 39-29-1048). A high-speed CAN PHY provides CAN bus communications through a 1 x 4 Molex connector (pn 39-30-3045).

Connecting LIN cables require Molex housing, pn 39-01-2040 and pins, pn 39-00-0217. Connecting CAN cables require Molex housing, pn 39-01-4040, and pins, pn 39-00-0217.

The COM_SEL option header connects the MCU SCI signal to either the LIN PHY or the RS-232 PHY. See Figure 6 below for jumper position options. See Figure 4 below for jumper position options.

RS-232

The TWR-S12G128 applies the MAX3387E, RS-232 transceiver to support serial communications. A standard 2x5 "Berg" pin-header on 0.1" centers and an IDC to DB9 cable supports connecting standard serial cables to the target board. Figure 4 below shows the SCI signal connections.

Figure 4: Serial Connections

MCU Port Signal	Transceiver Signal	COM CONNECTOR	COMMENTS
	+5V	J5-1	
PS1//TXD0	TXD	J5-3	pull-up
PS0//RXD0	RXD	J5-5	
PAD9/KWAD9/AN9	DTR	J5-7	CT2 (NC)
	GND	J5-9	
PD2	DSR	J5-2	pull-up
PD1	CTS	J5-4	CT3 (NC), pull-up
PAD10/KWAD10/AN10	RTS	J5-6	pull-up
	TP2	J5-8	
PAD8/KWAD8/AN8	INVALID*		CT4 (NO)
PAD15/KWAD15/AN15	FORCEOFF*		CT5 (NC)

NOTE: For normal RS-232 operation, FORCEOFF* should be actively driven to the high level. Alternately, open CT5 to allow FORCEOFF* to float high.

COM Connectcor

A 2x5, 0.1", standard "Berg" pin-header provides external connections for the SCI port. Figure 5 below shows the COM1 pin-out.

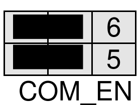
Figure 5: COM1 Connector

2, 7	1	2	1, 7
TXD	3	4	CTS
RXD	5	6	RTS
1, 2	7	8	TP2
GND	9	10	NC

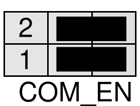
COM_EN

The COM_EN option header connects the MCU SCI port to either the SCI PHY or the LIN PHY. Figure 6 below shows the option jumper configuration for the COM_EN option header.

Figure 6: COM_EN Option Header



Connects target MCU SCI port to LIN PHY to enable LIN bus communications

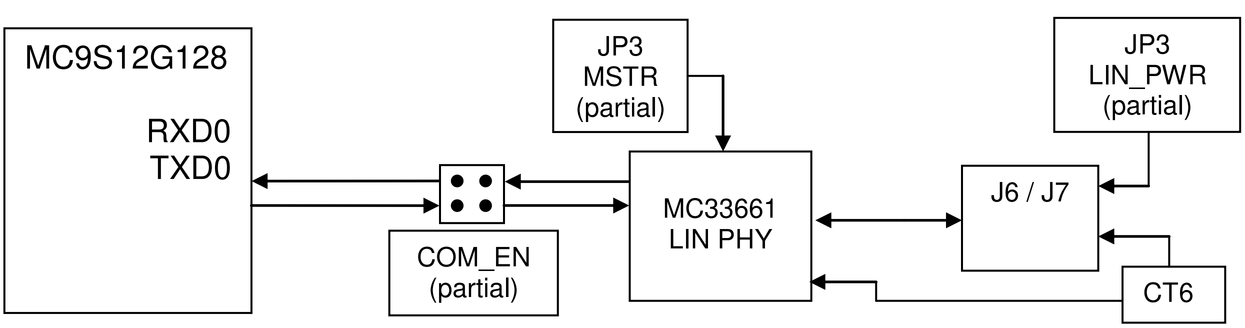


Connects target MCU SCI port to RS-232 PHY to enable serial communications

LIN Port

The TWR-S12G128 applies the MC33661 LIN bus physical layer device (transceiver) to support LIN communications. The PHY may be configured as a Master or Slave node on the LIN bus. LIN connectors J9 & J10 are configured in parallel to support pass-thru signaling. Figure 7 shows the LIN block diagram.

Figure 7: LIN Block Diagram



The LIN interface provides optional features of slew rate control, network supply, and wake up option. Refer to the MC33661 Reference Manual for detail on PHY functionality. The following sections detail functionality for LIN option jumpers.

LIN Enable

The LIN PHY is enabled by default. Disable the PHY by connecting the test point, TP3, to GND.

LIN COM Input

LIN inputs RX and TX are selectable using the COM_EN option header. Refer to Figure 6 above for details on configuring this header.

LIN_PWR Option

The LIN_PWR option jumper connects pin 1 of both LIN connectors to the +V input. In Master mode, this option may be used to power LIN slave devices. This option requires +12V be applied at E1/E2 inputs. In Slave mode, this option allows slave device to draw power from the LIN network. For Slave mode configuration, external power should not be applied to the target board. LIN_PWR is enabled by installing a shunt from JP3-1 to JP3-2. Refer to Figure 8 below.

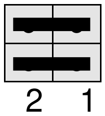
> **CAUTION:**
>
> If the target board draws power from the LIN bus in Slave mode, do not apply external power at E1/E2 inputs. Damage to the board may result.

> **NOTE:**
>
> If the target board powers the LIN bus in Master mode, +12V must be applied externally at E1/E2 inputs.

MSTR Option

The MSTR option jumper allows the LIN transceiver to be configured for Master mode functionality. Master mode may also be set using the INH pin on the PHY. Refer to the MC33661 device datasheet for details on use and configuration. Refer to Figure 8 below.

Figure 8: JP6 Option Header



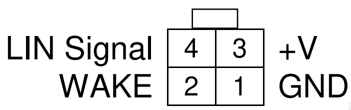
JP3	Connects LIN bus to +V input (default)
LIN_PWR	Enables LIN Master mode functionality (default)

NOTE: LIN PHY may also be configured as a Master Node using the INH pin. Refer to the LIN PHY data sheet for details.

LIN-J1 Connector

The TWR-S12G128 supports two, 2 x 2 Molex connectors to interface to the LIN bus. Figure 9 below details the pin-out of the LIN bus connector.

Figure 9: LIN Connector



Front View – Looking into Connector

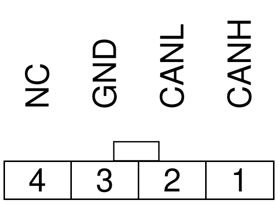
NOTE: LIN Port Connector – Molex 39-29-1048
Mates with; Housing – Molex 39-01-2040, Pin – Molex 39-00-0036

CAN Port

One, TJA1040T, High-Speed CAN physical-layer transceiver (PHY) is applied to support CAN bus communications. A 4-pos, 4.22mm MOLEX connector interfaces to external CAN cabling.

Differential input CAN signals, are terminated with 120 ohms. Option headers, JP13 and JP15 allow the user to optionally disconnect signal termination. Avalanche diodes protect the CAN PHY from voltage surges on the input differential signal lines. Figure 10 below shows the CAN connector pin-out.

Figure 10: CAN_PORT



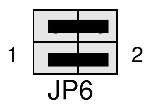
Front View – Looking into Connector

NOTE: CAN Port Connector – Molex 39-30-3045
Mates with; Housing – Molex 39-01-4040, Pin – Molex 39-00-0217

CAN Termination Enable

CAN bus termination of 120 ohm with virtual ground is applied to the differential CAN signals on both channels. The SPLIT output from each PHY is connected to the virtual ground providing common-mode stabilization. The differential CAN bus signal termination may be removed using option header JP13 or JP15. To prevent signal corruption, both option jumpers **must** be installed or both option jumpers **must** be removed. The CAN bus should not be operated with only 1 signal termination applied. Figure 11 below details the option header shunt positions.

Figure 11: CAN Termination Enable



Enables CANL termination
Enables CANH termination

Standby Mode

The CAN PHY is configured for normal mode by default. To enable standby (STB) mode, apply a high logic level at test point TP1. Refer to the TJA1040T Reference Manual for use and capabilities of the Standby Mode.

USER PERIPHERALS

User I/O includes 1 potentiometer, 4 push button switches, and 4 green LEDs for user I/O. The USER (JP14) option header enables or disables each User I/O function individually. The sections below provide details on user I/O. Figure 12 below shows the USER jumper settings.

Potentiometer

The TWR-S12G128 target board applies a single-turn, 5K, ohm potentiometer (POT) to simulate analog input. The POT is connected to an ATD input on the target MCU and is decoupled to minimize noise transients during adjustment. Figure 12 below shows the USER jumper settings.

User LED's

The TWR-S12G128 target board applies 4, green, LEDs for output indication. Each LED is configured for active-low operation. A series, current-limit resistor prevents excessive diode current. Each LED is connected to a timer channel on the target MCU. Figure 12 below shows the USER jumper settings.

Pushbutton Switches

The TWR-S12G128 provides 4 push-button switches for user input. Each push-button switch is configured for active-low operation and is connected to a key-wakeup input on the target MCU. No bias is applied to these push-button inputs and use of target MCU internal pull-ups is required for proper operation. Figure 12 below shows the USER jumper settings.

Figure 12: JP1 Option Header

	JP1	Signal	ON	OFF
SW1		PAD4/KWAD4/AN4	Enabled	Disabled
SW2		PAD5/KWAD5/AN5	Enabled	Disabled
SW3		PAD6/KWAD6/AN6	Enabled	Disabled
SW4		PAD7/KWAD7/AN7	Enabled	Disabled
POT		PAD0/KWAD0/AN0	Enabled	Disabled
LED1		PT4/IOC4	Enabled	Disabled
LED2		PT5/IOC5	Enabled	Disabled
LED3		PT6/IOC6	Enabled	Disabled
LED4		PT7/IOC7	Enabled	Disabled

NOTE: User peripheral input/output is enabled by default.

EDGE CONNECTOR PINOUT

The TWR-S12 board connects to the Freescale Tower System using the 2 PCIe Edge Connectors. Following the PCIe specification, the Bx signals are located on the top of the board and the Ax signals are located on bottom. Pin B1 for the primary and secondary connectors are at opposite ends of the board. The figures below show the pin-out of each edge connector.

Figure 13: Primary Edge Connector

5.0V Power	Pri_B01	Pri_A01	**5.0V Power**
Ground	Pri_B02	Pri_A02	**Ground**
	Pri_B03	Pri_A03	
Elevator Power Sense	Pri_B04	Pri_A04	
Ground	Pri_B05	Pri_A05	**Ground**
Ground	Pri_B06	Pri_A06	**Ground**
PS6/SCK0	Pri_B07	Pri_A07	
	Pri_B08	Pri_A08	
PS7/API_EXTCLK/SS0	Pri_B09	Pri_A09	PD3
PS5/MOSI0	Pri_B10	Pri_A10	PD4
PS4/MISO0	Pri_B11	Pri_A11	PD5
	Pri_B11A		
	Pri_B12	Pri_A12	
	Pri_B13	Pri_A13	
	Pri_B14	Pri_A14	
	Pri_B15	Pri_A15	
	Pri_B16	Pri_A16	
	Pri_B17	Pri_A17	
	Pri_B18	Pri_A18	
	Pri_B19	Pri_A19	
	Pri_B20	Pri_A20	
PD6	Pri_B21	Pri_A21	
PD7	Pri_B22	Pri_A22	
PB3	Pri_B23	Pri_A23	
	Pri_B24	Pri_A24	
	Pri_B25	Pri_A25	
Ground	Pri_B26	Pri_A26	**Ground**
PAD7/KWAD7/AN7	Pri_B27	Pri_A27	PAD3/KWAD3/AN3
PAD6/KWAD6/AN6	Pri_B28	Pri_A28	PAD2/KWAD2/AN2
PAD5/KWAD5/AN5	Pri_B29	Pri_A29	PAD1/KWAD1/AN1
PAD4/KWAD4/AN4	Pri_B30	Pri_A30	PAD0/KWAD0/AN0
Ground	Pri_B31	Pri_A31	**Ground**
	Pri_B32	Pri_A32	
IOC3/PT3	Pri_B33	Pri_A33	IOC1/PT1
IOC2/PT2	Pri_B34	Pri_A34	IOC0/PT0
PB6	Pri_B35	Pri_A35	PB7

3.3V Power	Pri_B36	Pri_A36	**3.3V Power**
PWM7/KWP7/PP7	Pri_B37	Pri_A37	PWM3/ETRIG3/KWP3/PP3
PWM6/KWP6/PP6	Pri_B38	Pri_A38	PWM2/ETRIG2/KWP2/PP2
PWM5/KWP5/PP5	Pri_B39	Pri_A39	PWM1/ETRIG1/KWP1/PP1
PWM4/KWP4/PP4	Pri_B40	Pri_A40	PWM0/ETRIG0/KWP0/PP0
PM0/RXCAN	Pri_B41	Pri_A41	PS0/RXD0
PM1/TXCAN	Pri_B42	Pri_A42	PS1/TXD0
	Pri_B43	Pri_A43	PS2/RXD1
MISO2/KWJ4/PJ4	Pri_B44	Pri_A44	PS3/TXD1
MOSI2/KWJ5/PJ5	Pri_B45	Pri_A45	VSSA (w/ NC CT)
SS2/KWJ7/PJ7	Pri_B46	Pri_A46	VDDA (w/ NC CT)
	Pri_B47	Pri_A47	PA0
SCK2/KWJ6/PJ6	Pri_B48	Pri_A48	PA1
Ground	Pri_B49	Pri_A49	**Ground**
	Pri_B50	Pri_A50	PA2
	Pri_B51	Pri_A51	PA3
	Pri_B52	Pri_A52	PA4
	Pri_B53	Pri_A53	PA5
	Pri_B54	Pri_A54	PA6
	Pri_B55	Pri_A55	PA7
	Pri_B56	Pri_A56	
	Pri_B57	Pri_A57	
	Pri_B58	Pri_A58	IOC7/PT7
	Pri_B59	Pri_A59	IOC6/PT6
	Pri_B60	Pri_A60	IOC5/PT5
XIRQ/PB5	Pri_B61	Pri_A61	IOC4/PT4
IRQ/PB4	Pri_B62	Pri_A62	RESET
	Pri_B63	Pri_A63	
	Pri_B64	Pri_A64	ECLK/PB0
Ground	Pri_B65	Pri_A65	**Ground**
	Pri_B66	Pri_A66	
	Pri_B67	Pri_A67	
	Pri_B68	Pri_A68	
	Pri_B69	Pri_A69	
	Pri_B70	Pri_A70	
	Pri_B71	Pri_A71	
	Pri_B72	Pri_A72	
	Pri_B73	Pri_A73	
	Pri_B74	Pri_A74	
	Pri_B75	Pri_A75	
	Pri_B76	Pri_A76	
	Pri_B77	Pri_A77	
	Pri_B78	Pri_A78	
	Pri_B79	Pri_A79	
	Pri_B80	Pri_A80	
Ground	Pri_B81	Pri_A81	**Ground**
3.3V Power	Pri_B82	Pri_A82	**3.3V Power**

Figure 14: Secondary Edge Connector

5.0V Power	Sec_B01	Sec_A01	**5.0V Power**
Ground	Sec_B02	Sec_A02	**Ground**
	Sec_B03	Sec_A03	
Elevator Power Sense	Sec_B04	Sec_A04	
Ground	Sec_B05	Sec_A05	**Ground**
Ground	Sec_B06	Sec_A06	**Ground**
SCK1/KWJ2/PJ2	Sec_B07	Sec_A07	
	Sec_B08	Sec_A08	
SS1/KWJ3/PJ3	Sec_B09	Sec_A09	PC0
MOSI1/KWJ1/PJ1	Sec_B10	Sec_A10	
MISO1/KWJ0/PJ0	Sec_B11	Sec_A11	
	Sec_B11A		
	Sec_B12	Sec_A12	
	Sec_B13	Sec_A13	
	Sec_B14	Sec_A14	
	Sec_B15	Sec_A15	
PC1	Sec_B16	Sec_A16	
PC2	Sec_B17	Sec_A17	PC3
PC4	Sec_B18	Sec_A18	PC5
	Sec_B19	Sec_A19	
	Sec_B20	Sec_A20	
	Sec_B21	Sec_A21	
	Sec_B22	Sec_A22	
	Sec_B23	Sec_A23	
	Sec_B24	Sec_A24	
	Sec_B25	Sec_A25	
Ground	Sec_B26	Sec_A26	**Ground**
	Sec_B27	Sec_A27	PAD11/KWAD11/AN11
	Sec_B28	Sec_A28	PAD10/KWAD10/AN10
PAD13/KWAD13/AN13	Sec_B29	Sec_A29	PAD9/KWAD9/AN9
PAD12/KWAD12/AN12	Sec_B30	Sec_A30	PAD8/KWAD8/AN8
Ground	Sec_B31	Sec_A31	**Ground**
	Sec_B32	Sec_A32	
	Sec_B33	Sec_A33	
	Sec_B34	Sec_A34	
PC6	Sec_B35	Sec_A35	PC7
3.3V Power	Sec_B36	Sec_A36	**3.3V Power**
	Sec_B37	Sec_A37	
	Sec_B38	Sec_A38	
	Sec_B39	Sec_A39	
	Sec_B40	Sec_A40	
	Sec_B41	Sec_A41	PM2/RXD2
	Sec_B42	Sec_A42	PM3/TXD2
PD0	Sec_B43	Sec_A43	
	Sec_B44	Sec_A44	
	Sec_B45	Sec_A45	

	Sec_B46	Sec_A46	
	Sec_B47	Sec_A47	
	Sec_B48	Sec_A48	
Ground	Sec_B49	Sec_A49	**Ground**
PD1	Sec_B50	Sec_A50	
PD2	Sec_B51	Sec_A51	
	Sec_B52	Sec_A52	
	Sec_B53	Sec_A53	
	Sec_B54	Sec_A54	
	Sec_B55	Sec_A55	
	Sec_B56	Sec_A56	
	Sec_B57	Sec_A57	
	Sec_B58	Sec_A58	
	Sec_B59	Sec_A59	
	Sec_B60	Sec_A60	
	Sec_B61	Sec_A61	
	Sec_B62	Sec_A62	
	Sec_B63	Sec_A63	
	Sec_B64	Sec_A64	
Ground	Sec_B65	Sec_A65	**Ground**
	Sec_B66	Sec_A66	
	Sec_B67	Sec_A67	
	Sec_B68	Sec_A68	
	Sec_B69	Sec_A69	
	Sec_B70	Sec_A70	
	Sec_B71	Sec_A71	
	Sec_B72	Sec_A72	
	Sec_B73	Sec_A73	
	Sec_B74	Sec_A74	
	Sec_B75	Sec_A75	
	Sec_B76	Sec_A76	
	Sec_B77	Sec_A77	
	Sec_B78	Sec_A78	
	Sec_B79	Sec_A79	
	Sec_B80	Sec_A80	
Ground	Sec_B81	Sec_A81	**Ground**
3.3V Power	Sec_B82	Sec_A82	**3.3V Power**