

## Description

The DGD2181M is a high-voltage / high-speed gate driver capable of driving N-Channel MOSFETs and IGBTs in a half-bridge configuration. High-voltage processing techniques enable the DGD2181M's high-side to switch to 600V in a bootstrap operation.

The DGD2181M logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) for easy interfacing with controlling devices. The driver outputs feature high-pulse current buffers designed for minimum driver cross conduction.

The DGD2181M is offered in SO-8 package and the operating temperature extends from -40°C to +125°C.

## Applications

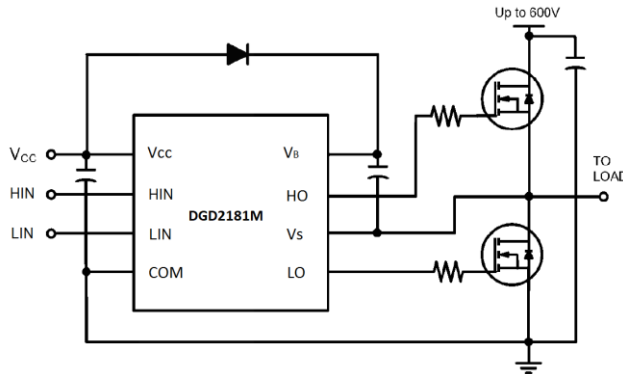
- DC-DC Converters
- DC-AC Inverters
- AC-DC Power Supplies
- Motor Controls
- Class D Power Amplifiers

## Features

- Floating High-Side Driver in Bootstrap Operation to 600V
- Drives Two N-Channel MOSFETs or IGBTs in a Half Bridge Configuration
- 1.9A Source / 2.3A Sink Output Current Capability
- Outputs Tolerant to Negative Transients
- Wide Low-Side Gate Driver and Logic Supply: 10V to 20V
- Logic Input (HIN and LIN) 3.3V Capability
- Schmitt Triggered Logic Inputs with Internal Pull Down
- Undervoltage Lockout for High and Low Side Drivers
- Extended Temperature Range: -40°C to +125°C
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q101, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](mailto:contact@diodes.com) or your local Diodes representative.**
- <https://www.diodes.com/quality/product-definitions/>

## Mechanical Data

- Case: SO-8 (Type TH)
- Case Material: Molded Plastic. "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 3 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads. Solderable per MIL-STD-202, Method 208 ③
- Weight: 0.075 grams (Approximate)



Typical Configuration



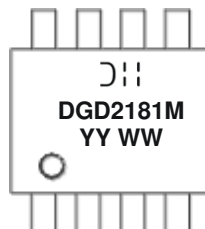
Top View

## Ordering Information (Note 4)

Part Number	Marking	Reel Size (inches)	Tape Width (mm)	Quantity per Reel
DGD2181MS8-13	DGD2181M	13	12	2,500

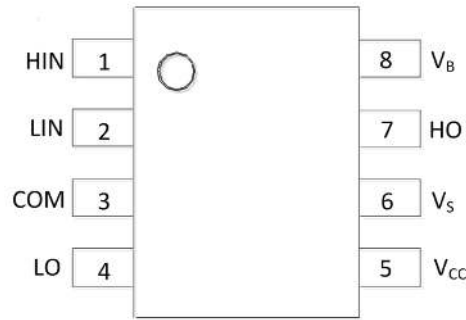
- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
  2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

## Marking Information



D = Manufacturer's Marking  
 DGD2181M = Product Type Marking Code  
 YY = Year (ex: 19 = 2019)  
 WW = Week (01 to 53)

## Pin Diagrams

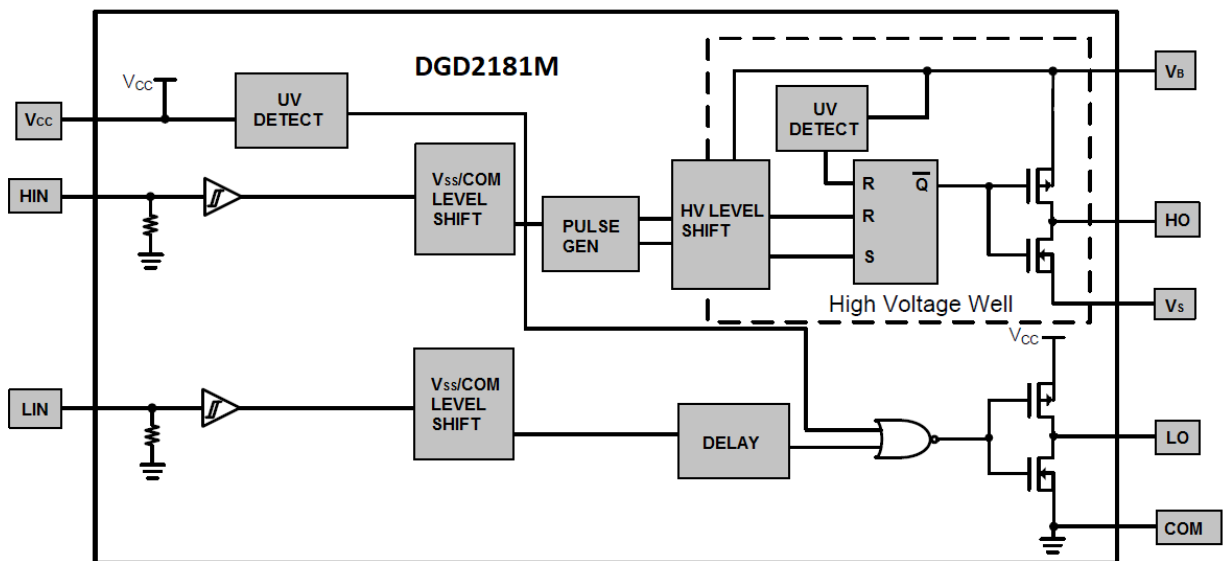


Top View SO-8

## Pin Descriptions

Pin Number	Pin Name	Function
1	HIN	Logic input for high-side gate driver output, in phase with HO
2	LIN	Logic input for low-side gate driver output, in phase with LO
3	COM	Low-side and logic return
4	LO	Low-side gate drive output
5	V <sub>CC</sub>	Low-side and logic fixed supply
6	V <sub>S</sub>	High-side floating supply return
7	HO	High-side gate drive output
8	V <sub>B</sub>	High-side floating supply

## Functional Block Diagram



**Absolute Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
High-Side Floating Supply Voltage	V <sub>B</sub>	-0.3 to +624	V
High-Side Floating Supply Offset Voltage	V <sub>S</sub>	V <sub>B</sub> -24 to V <sub>B</sub> +0.3	V
High-Side Floating Output Voltage	V <sub>HO</sub>	V <sub>S</sub> -0.3 to V <sub>B</sub> +0.3	V
Offset Supply Voltage Transient	dV <sub>S</sub> /dt	50	V/ns
Low-Side Fixed Supply Voltage	V <sub>CC</sub>	-0.3 to +24	V
Low-Side Output Voltage	V <sub>LO</sub>	-0.3 to V <sub>CC</sub> +0.3	V
Logic Input Voltage (HIN and LIN)	V <sub>IN</sub>	-0.3 to V <sub>CC</sub> +0.3	V

**Thermal Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Power Dissipation Linear Derating Factor (Note 5)	P <sub>D</sub>	0.625	W
Thermal Resistance, Junction to Ambient (Note 5)	R <sub>θJA</sub>	200	°C/W
Operating Temperature	T <sub>J</sub>	+150	°C
Lead Temperature (Soldering, 10s)	T <sub>L</sub>	+300	
Storage Temperature Range	T <sub>STG</sub>	-55 to +150	

Note: 5. When mounted on a standard JEDEC 2-layer FR-4 board.

**Recommended Operating Conditions**

Parameter	Symbol	Min	Max	Unit
High-Side Floating Supply Absolute Voltage	V <sub>B</sub>	V <sub>S</sub> + 10	V <sub>S</sub> + 20	V
High-Side Floating Supply Offset Voltage	V <sub>S</sub>	(Note 6)	600	V
High-Side Floating Output Voltage	V <sub>HO</sub>	V <sub>S</sub>	V <sub>B</sub>	V
Low-Side Fixed Supply Voltage	V <sub>CC</sub>	10	20	V
Low-Side Output Voltage	V <sub>LO</sub>	0	V <sub>CC</sub>	V
Logic Input Voltage (HIN and LIN)	V <sub>IN</sub>	0	5	V
Ambient Temperature	T <sub>A</sub>	-40	+125	°C

Note: 6. Logic operation for V<sub>S</sub> of -5V to +600V.

**DC Electrical Characteristics** ( $V_{BIAS} (V_{CC}, V_{BS}) = 15V, @T_A = +25^{\circ}C$ , unless otherwise specified.) (Note 7)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Logic "1" Input Voltage (Note 8)	$V_{IH}$	2.5	—	—	V	$V_{CC} = 10V$ to $20V$
Logic "0" Input Voltage (Note 8)	$V_{IL}$	—	—	0.8	V	$V_{CC} = 10V$ to $20V$
High Level Output Voltage, $V_{BIAS} - V_O$	$V_{OH}$	—	—	1.4	V	$I_O = 0mA$
Low Level Output Voltage, $V_O$	$V_{OL}$	—	—	0.2	V	$I_O = 20mA$
Offset Supply Leakage Current	$I_{LK}$	—	—	50	$\mu A$	$V_B = V_S = 600V$
Quiescent $V_{BS}$ Supply Current	$I_{BSQ}$	20	60	150	$\mu A$	$V_{IN} = 0V$ or $5V$
Quiescent $V_{CC}$ Supply Current	$I_{CCQ}$	50	120	240	$\mu A$	$V_{IN} = 0V$ or $5V$
Logic "1" Input Bias Current	$I_{IN+}$	—	25	60	$\mu A$	$V_{IN} = 5V$
Logic "0" Input Bias Current	$I_{IN-}$	—	—	5.0	$\mu A$	$V_{IN} = 0V$
$V_{BS}$ Supply Undervoltage Positive Going Threshold	$V_{BSUV+}$	8.0	8.9	9.8	V	—
$V_{BS}$ Supply Undervoltage Negative Going Threshold	$V_{BSUV-}$	7.4	8.2	9.0	V	—
$V_{CC}$ Supply Undervoltage Positive Going Threshold	$V_{CCUV+}$	8.0	8.9	9.8	V	—
$V_{CC}$ Supply Undervoltage Negative Going Threshold	$V_{CCUV-}$	7.4	8.2	9.0	V	—
Output High Short Circuit Pulsed Current	$I_{O+}$	1.4	1.9	—	A	$V_O = 0V, PW \leq 10\mu s$
Output Low Short Circuit Pulsed Current	$I_{O-}$	1.7	2.3	—	A	$V_O = 15V, PW \leq 10\mu s$

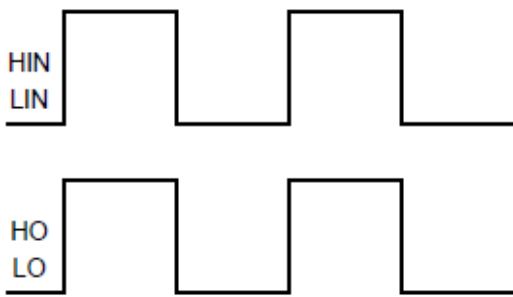
Note: 7. The  $V_{IN}$  and  $I_{IN}$  parameters are applicable to the two logic input pins: LIN and HIN. The  $V_O$  and  $I_O$  parameters are applicable to the respective output pins: HO and LO.

8. For optimal operation, it is recommended that the input pulses (HIN and LIN) should have a minimum amplitude of 2.5V with a minimum pulse width of 360ns.

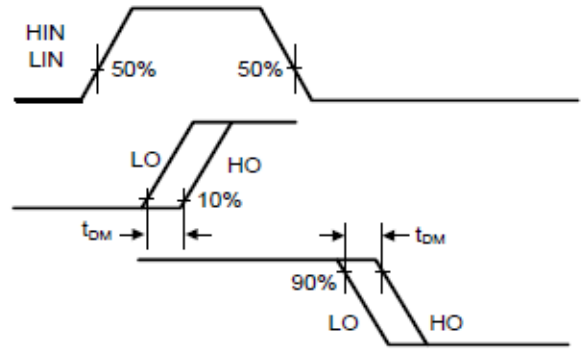
**AC Electrical Characteristics** ( $V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000pF, @T_A = +25^{\circ}C$ , unless otherwise specified.)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Turn-On Propagation Delay	$t_{ON}$	—	180	270	ns	$V_S = 0V$
Turn-Off Propagation Delay	$t_{OFF}$	—	220	330	ns	$V_S = 0V$ or $600V$
Delay Matching, HO & LO Turn-On/Off	$t_{DM}$	—	—	35	ns	—
Turn-On Rise Time	$t_R$	—	40	60	ns	$V_S = 0V$
Turn-Off Fall Time	$t_F$	—	20	35	ns	$V_S = 0V$

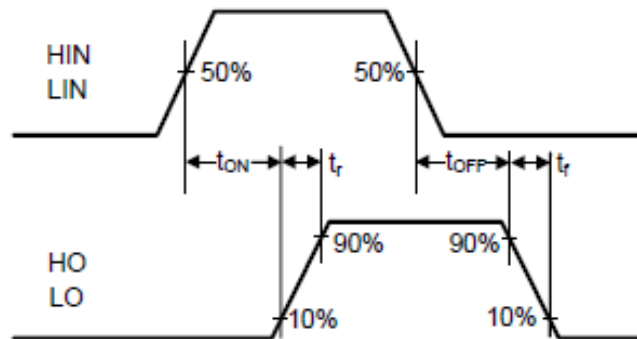
**Timing Waveforms**



**Figure 1.** Input / Output Timing Diagram

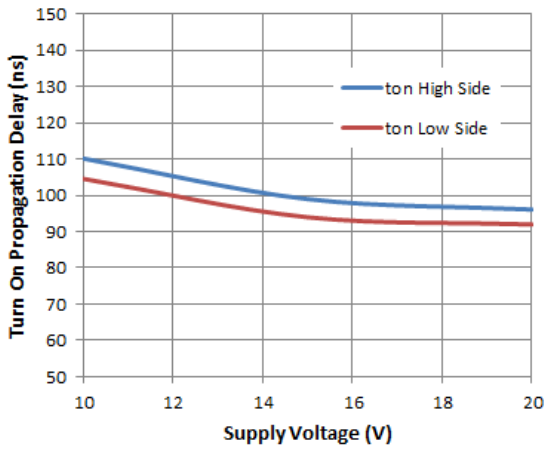


**Figure 2.** Delay Matching Waveform Definitions

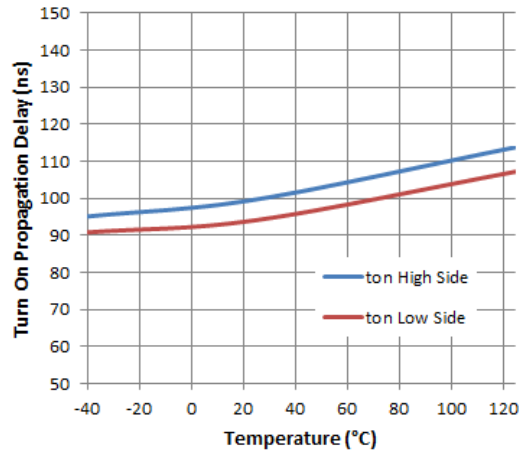


**Figure 3.** Switching Time Waveform Definitions

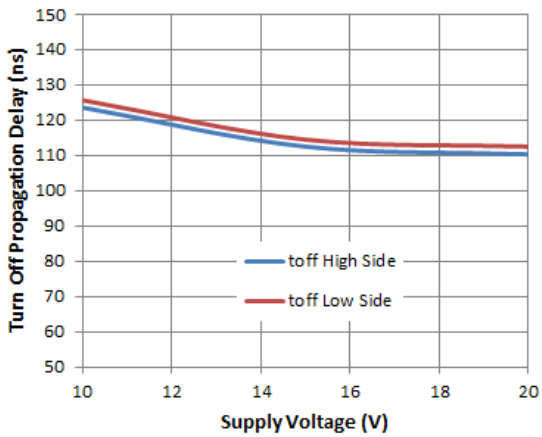
**Typical Performance Characteristics** (@ $T_A = +25^\circ\text{C}$ ,  $V_{CC} = 15\text{V}$ , unless otherwise specified.)



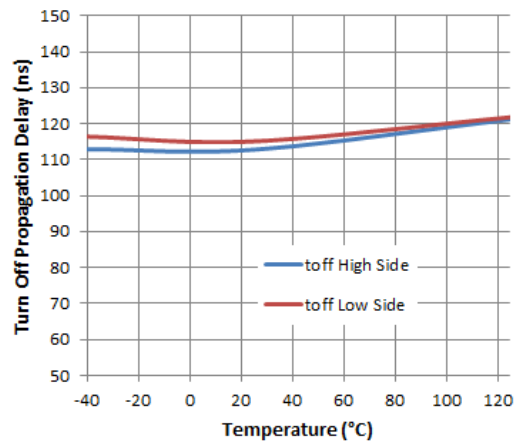
**Figure 4.** Turn-on Propagation Delay vs. Supply Voltage



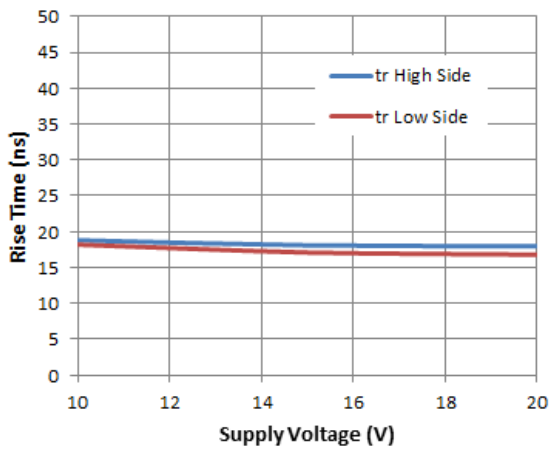
**Figure 5.** Turn-on Propagation Delay vs. Temperature



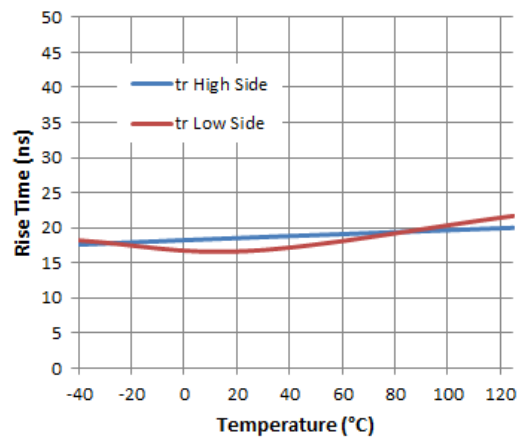
**Figure 6.** Turn-off Propagation Delay vs. Supply Voltage



**Figure 7.** Turn-off Propagation Delay vs. Temperature

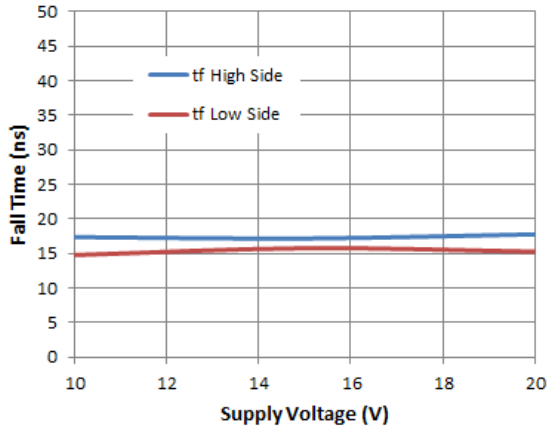


**Figure 8.** Rise Time vs. Supply Voltage

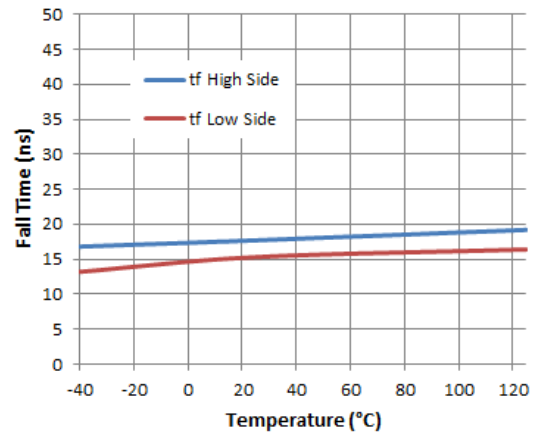


**Figure 9.** Rise Time vs. Temperature

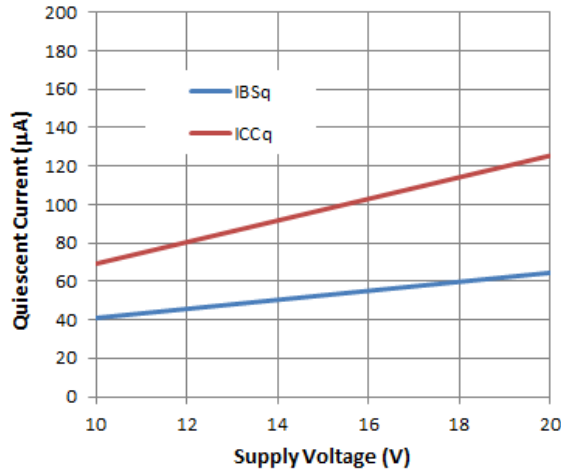
**Typical Performance Characteristics** (continued)



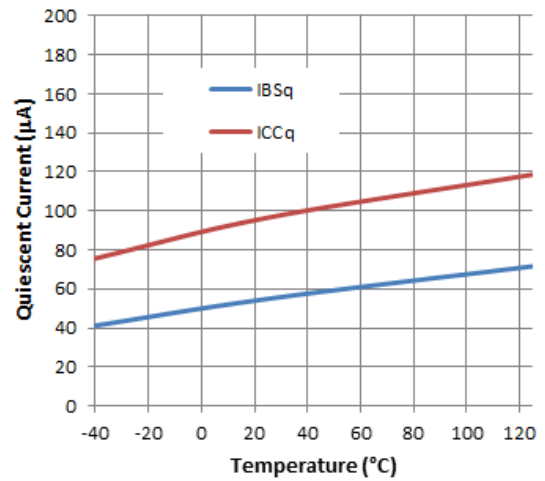
**Figure 10.** Fall Time vs. Supply Voltage



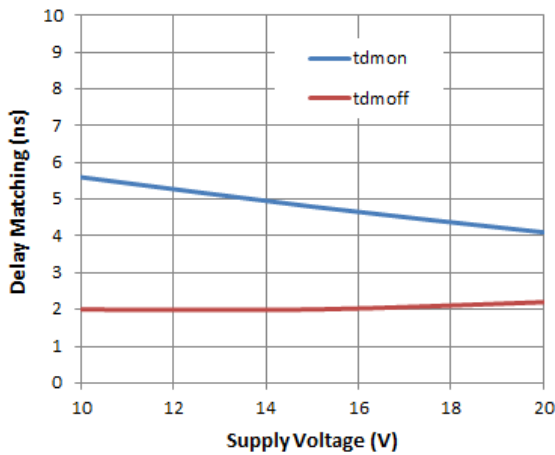
**Figure 11.** Fall Time vs. Temperature



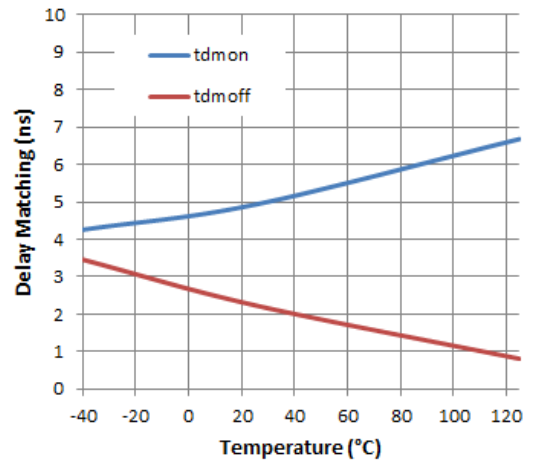
**Figure 12.** Quiescent Current vs. Supply Voltage



**Figure 13.** Quiescent Current vs. Temperature

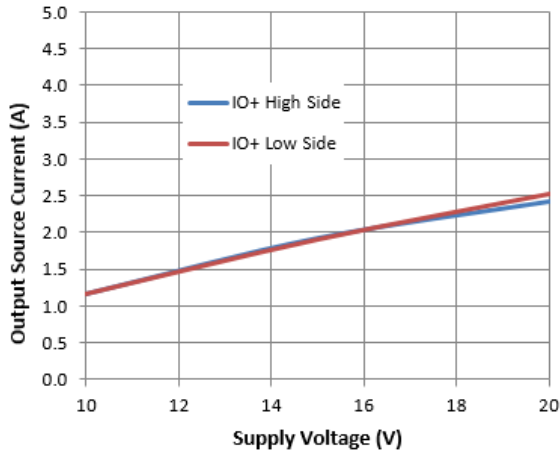


**Figure 14.** Delay Matching vs. Supply Voltage

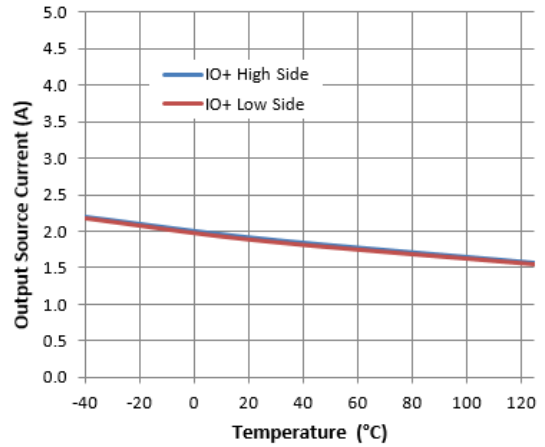


**Figure 15.** Delay Matching vs. Temperature

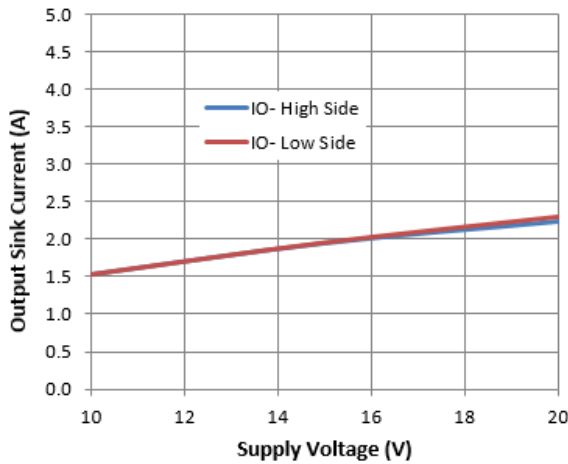
**Typical Performance Characteristics** (continued)



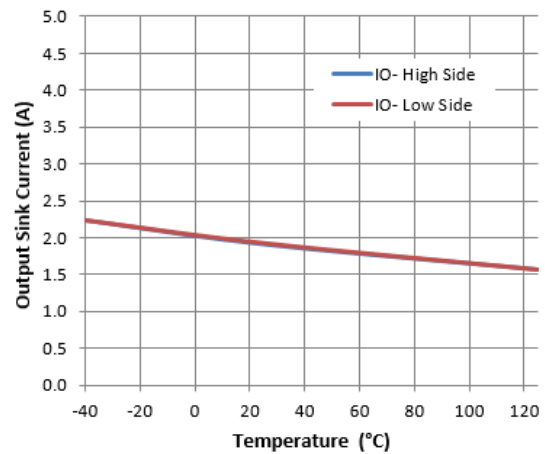
**Figure 16.** Output Source Current vs. Supply Voltage



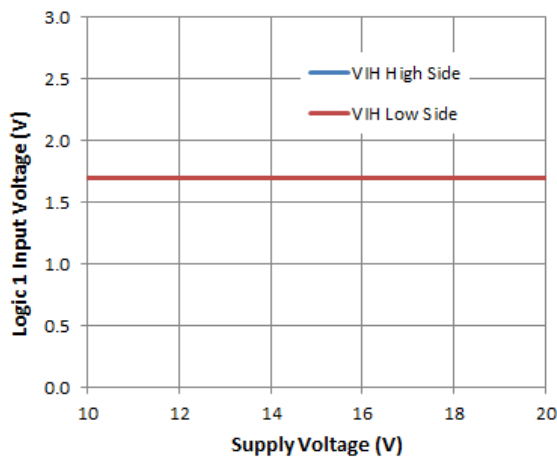
**Figure 17.** Output Source Current vs. Temperature



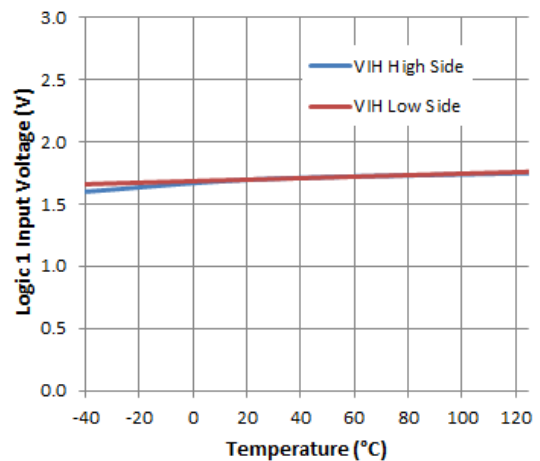
**Figure 18.** Output Sink Current vs. Supply Voltage



**Figure 19.** Output Sink Current vs. Temperature



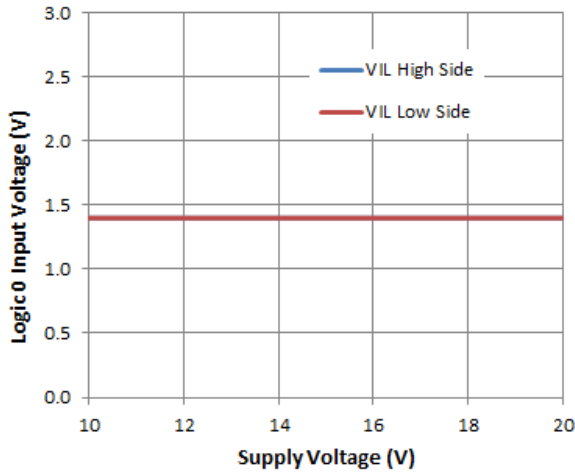
**Figure 20.** Logic 1 Input Voltage vs. Supply Voltage



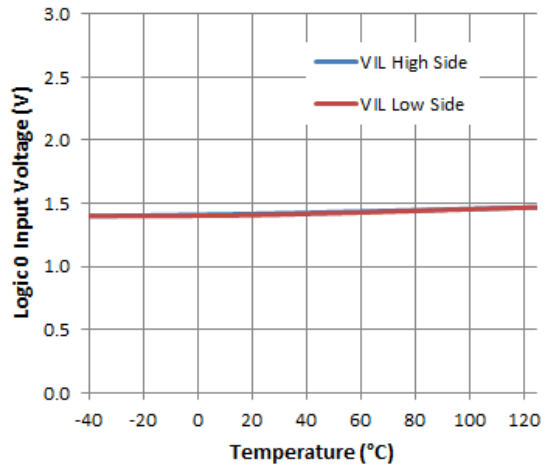
**Figure 21.** Logic 1 Input Voltage vs. Temperature



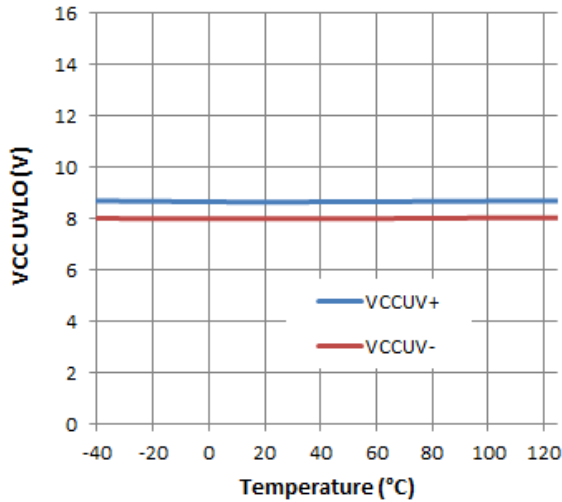
**Typical Performance Characteristics** (continued)



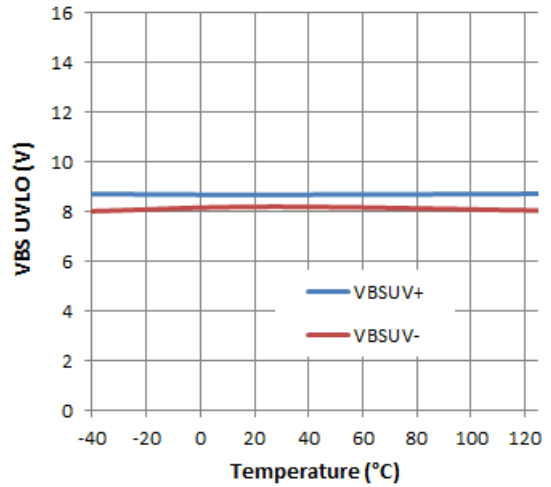
**Figure 22.** Logic 0 Input Voltage vs. Supply Voltage



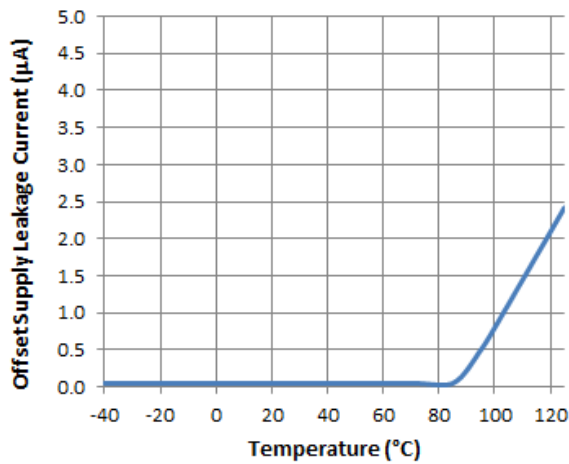
**Figure 23.** Logic 0 Input Voltage vs. Temperature



**Figure 24.** VCC UVLO vs. Temperature



**Figure 25.** VBS UVLO vs. Temperature

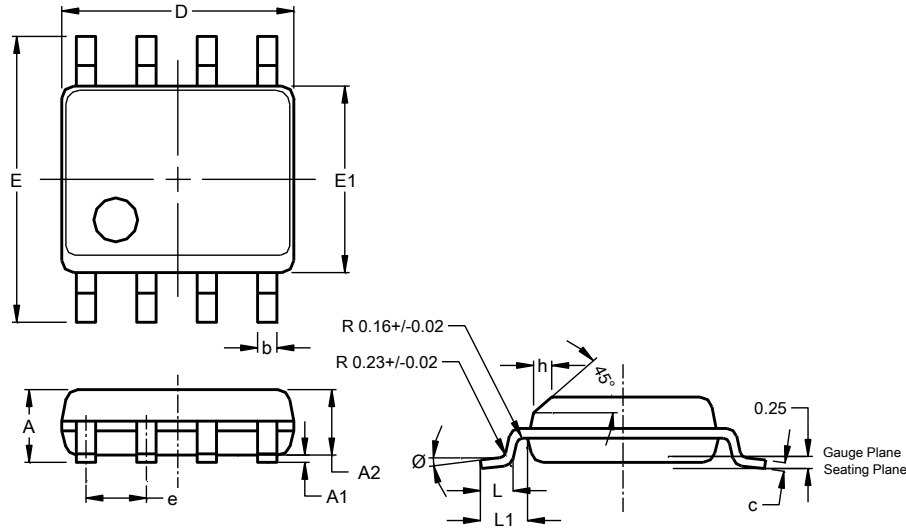


**Figure 26.** Offset Supply Leakage Current vs. Temperature

**Package Outline Dimensions**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**SO-8 (Type TH)**

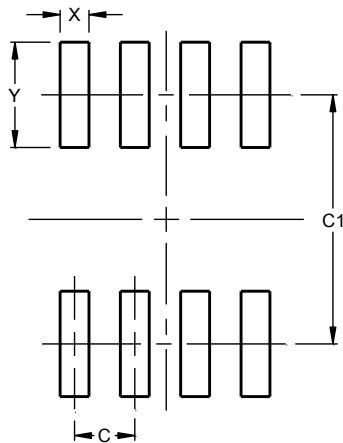


SO-8 (Type TH)			
Dim	Min	Max	Typ
A	1.35	1.75	--
A1	0.10	0.25	--
A2	--	--	1.45
b	0.35	0.51	--
c	0.190	0.248	--
D	4.80	5.00	4.90
E	5.80	6.20	6.00
E1	3.80	4.00	3.90
e	--	--	1.27
h	0.25	0.50	--
L	0.41	1.27	--
L1	--	--	1.04
Ø	0°	8°	--
All Dimensions in mm			

**Suggested Pad Layout**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**SO-8 (Type TH)**



Dimensions	Value (in mm)
C	1.27
C1	5.20
X	0.60
Y	2.20

Note: For high voltage applications, the appropriate industry sector guidelines should be considered with regards to creepage and clearance distances between device Terminals and PCB tracking.

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