DVD/MPEG CLOCK SOURCE

MK2746

Description

The MK2746 is a low cost, low jitter, high performance clock synthesizer for DVD and other MPEG2 based applications. Using analog Phase Locked Loop (PLL) techniques, the device accepts a 27 MHz fundamental mode crystal or clock input to produce multiple output clocks including the processor clock, audio clock, bus driver clock, SDRAM clock and a Video clock. The audio clocks are frequency locked to the 27 MHz input using our patented zero ppm error techniques, allowing audio and video to track exactly, thereby eliminating the need for large buffer memory.

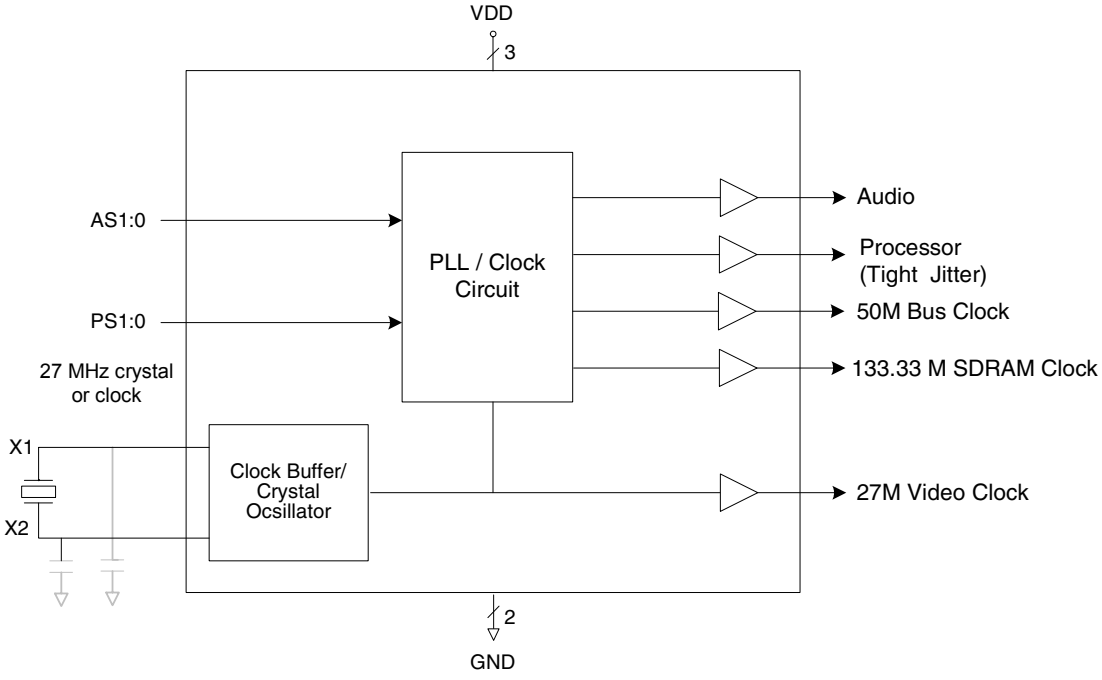
IDT manufacturers the largest variety of DVD, set top box, and multimedia clock synthesizers for all applications.

Features

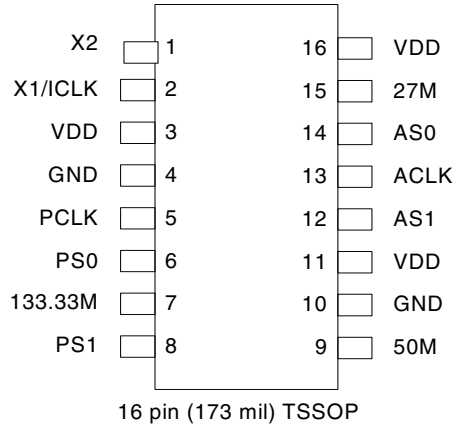
- Packaged in 16 pin TSSOP
- Operating voltage of 3.3 V
- Provides tight jitter controlled selectable processor clock per table.
- Provides selectable audio clock per table.
- Provides fixed outputs of 27 MHz (Video), 50 MHz (DSP/Bus clock) and 133.33 MHz (SDRAM).
- Advanced, low power, sub-micron CMOS process

NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01

Block Diagram



Pin Assignment



16 pin (173 mil) TSSOP

Clock Output Select Table in MHz

AS1	AS0	Audio CLK
0	0	12.288
0	1	11.2896
1	0	18.432
1	1	8.192

PS1	PS0	Processor CLK
0	0	66.66
0	1	41.66
1	0	50
1	1	58.33

0 = connect directly to GND

1 = connect directly to VDD

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X2	Input	Connect to a 27 MHz fundamental mode crystal. Leave open for clock input.
2	X1/ICLK	Input	Connect to a 27 MHz fundamental mode crystal or clock.
3	VDD	Power	Connect to +3.3 V.
4	GND	Power	Connect to ground
5	PCLK	Output	Processor clock output. Determined by the status of PS1, PS0 per table above.
6	PS0	Input	Processor Clock select 0. Selects processor clock per table above.
7	133.33M	Output	SDRAM clock output.
8	PS1	Input	Processor Clock select 1. Selects processor clock per table above.
9	50M	Output	50 MHz clock output.
10	GND	Power	Connect to ground.
11	VDD	Power	Connect to +3.3 V.
12	AS1	Input	Audio clock select 1. Selects audio clock per table above.
13	ACLK	Output	Audio clock output determined by the status of PS1, PS0.
14	AS0	Input	Audio clock select 0. Selects audio clock per table above.
15	27M	Output	27 MHz clock output.
16	VDD	Power	Connect to +3.3 V.

External Component Selection

The MK2746 requires a minimum number of external components for proper operation.

Decoupling Capacitors

Decoupling capacitors of 0.01µF should be connected between VDD and GND as close to the MK2746 as possible. For optimum device performance, the decoupling capacitors should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

Series Termination Resistor

When the PCB traces between the clock outputs and the loads are over 1 inch, series termination should be used. To series terminate a 50Ω trace (a commonly used trace impedance) place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

Crystal Tuning Load Capacitors

For a crystal input, a parallel resonant fundamental mode crystal should be used. Crystal capacitors must be connected between each of the pins X1 and X2 to ground. The value (in pF) of these crystal caps should equal (CL-6)*2. In this equation CL is equal to the crystal load capacitance in pF. As an example, for a crystal with an 18 pF load capacitance, each crystal capacitor would be 24 pF [(18-6)*2=24].

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The 0.01µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.

2) The external crystal should be mounted just next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.

3) To minimize EMI the 33Ω series termination resistor, if needed, should be placed close to the clock output.

4) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (the ferrite bead and bulk decoupling capacitor can be mounted on the back). Other signal traces should be routed away from the MK2746. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK2746. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70° C
Storage Temperature	-65 to +150° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	°C
Power Supply Voltage (measured in respect to GND)	+3.0		+3.6	V

DC Electrical Characteristics

VDD=3.3 V ±10% , Ambient temperature 0 to +70° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0		3.6	V
Input High Voltage	V_{IH}	input selects	2.0			V
Input Low Voltage	V_{IL}	input selects			0.8	V
Input High Voltage	V_{IH}	ICLK	(VDD/2)-1	VDD/2		V
Input Low Voltage	V_{IL}	ICLK		VDD/2	(VDD/2)+1	V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.4	V
Output High Voltage (CMOS Level)	V_{OH}	I_{OH} = -4 mA	VDD-0.4			V
Operating Supply Current	IDD	No load		40		mA
Short Circuit Current	I_{OS}			±70		mA
Input Capacitance	C_{IN}			5		pF
Nominal Output Impedance	Z_{OUT}			20		Ω
On Chip Pull-up Resistor	R_{PU}	AS1, AS0 pins		120		kΩ
		PS1 pin		510		kΩ

AC Electrical Characteristics

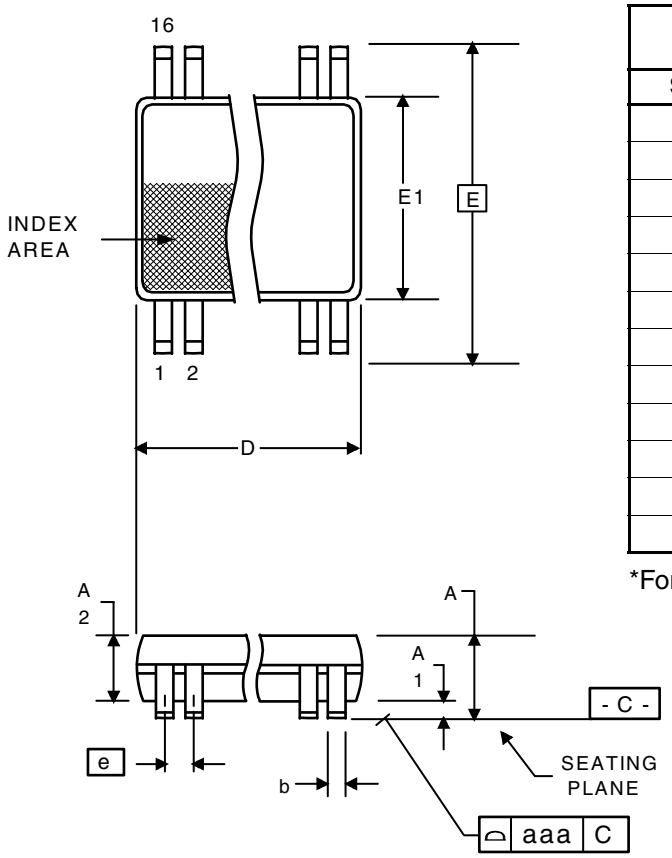
VDD = 3.3 V ±10%, Ambient Temperature 0 to +70° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency				27		MHz
Output Rise Time	t_{OR}	20% to 80% of VDD, Note 1		1.0	1.8	ns
Output Fall Time	t_{OF}	80% to 20% of VDD, Note 1		1.0	1.8	ns
Output Clock Duty Cycle	t_D	at VDD/2, Note 1	40	50	60	%
Maximum Output Jitter, short term, peak to peak	t_J	PCLK output, Note 1		±100		ps
Maximum Output Jitter, short term, peak to peak	t_J	All clocks, except PCLK, Note 1		±200		ps
Maximum Output Jitter, long term, peak to peak	t_J	1000 cycles, except ACLK, Note 1		750		ps

Note 1: Measured with 15 pF Load.

Package Outline and Package Dimensions (16-pin TSSOP, 4.40 mm Body, 0.65 mm Pitch)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches*	
Symbol	**Min**	**Max**	**Min**	**Max**
A	--	1.20	--	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	4.90	5.1	0.193	0.201
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	0.169	0.177
e	0.65 Basic		0.0256 Basic	
L	0.45	0.75	0.018	0.030
α	0°	8°	0°	8°
aaa	--	0.10	--	0.004

*For reference only. Controlling dimensions in mm.

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
MK2746G*	MK2746G	Tubes	16-pin TSSOP	0 to +70° C
MK2746GT*	MK2746G	Tape and Reel	16-pin TSSOP	0 to +70° C
MK2746GLF	MK2746GL	Tubes	16-pin TSSOP	0 to +70° C
MK2746GLFT	MK2746GL	Tape and Reel	16-pin TSSOP	0 to +70° C

***NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01**

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