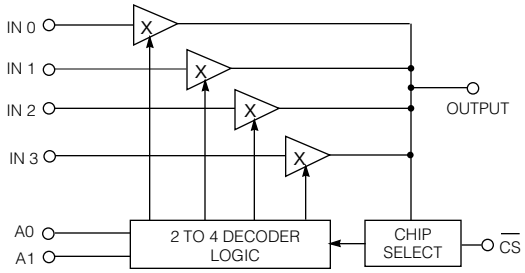
GX414A Monolithic 4x1 Video Multiplexer

DATA SHEET

FEATURES

- **low disabled power consumption: 5.2 mW**
- **low differential gain: 0.03% typ. at 4.43 MHz**
- **low differential phase: 0.012° typ. at 4.43 MHz**
- **bandwidth (-3dB) 100 MHz with 30 pF load**
- **all hostile crosstalk at 5 MHz -97dB typ.**
- **low insertion loss 0.05 dB max at 100 kHz**
- **off-isolation 110 dB at 10 MHz**
- **fast make before break switching: 200 ns typ.**
- **TTL and 5 volt CMOS compatible logic inputs**
- **for NTSC, PAL and SECAM applications**
- **low cost 14 pin DIP and16 pin SOIC packages**

FUNCTIONAL SCHEMATIC



TRUTH TABLE

$\overline{CS}$	A1	A0	OUTPUT
0	0	0	IN 0
0	0	1	IN 1
0	1	0	IN 2
0	1	1	IN 3
1	X	X	HI - Z

X = DON'T CARE

CAUTION
ELECTROSTATIC
SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION

CIRCUIT DESCRIPTION

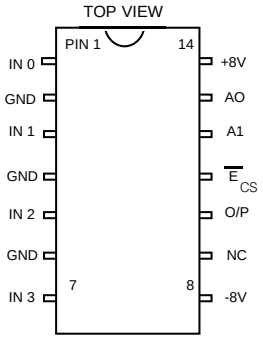
The GX414A is high performance low cost monolithic 4x1 video multiplexer incorporating four analog video switches and a 2 to 4 address decoder. An enabled input allows paralleled GX414As to be operated in a switching matrix with multiple inputs and a common output. Unlike similar devices using MOS bilateral switching elements, the GX414A represents a fully buffered unilateral trans-mission path when enabled. The GX414A requires ±8V and is designed for use in video switching applications. Logic inputs are TTL and 5V CMOS compatible, providing input select and output enable functions.

APPLICATIONS

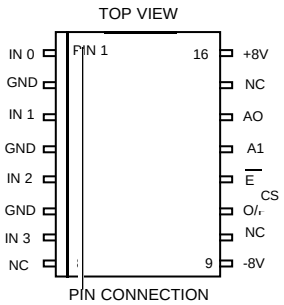
Glitch free analog switching for...

- High quality video routing
- A/D input multiplexing
- Sample and hold circuits
- TV/ CATV/ monitor switching
- Instrumentation and communication equipment

PIN CONNECTIONS



PIN CONNECTION
14 PIN DIP



PIN CONNECTION
16 PIN SOIC

ORDERING INFORMATION

Part Number	Package Type	Temperature Range
GX414 - ACDB	14 Pin DIP	0° to 70° C
GX414 - ACKC	16 Pin SOIC	0° to 70° C
GX414 - ACTC	Tape 16 Pin SOIC	0° to 70° C

ABSOLUTE MAXIMUM RATINGS

Parameter	Value
Supply Voltage	±13.5V
Operating Temperature Range	$0°C \le T_A \le 70° C$
Storage Temperature Range	$-65°C \le T_S \le 150° C$
Lead Temperature (Soldering, 10 Sec)	260° C

Parameter	Value
Analog Input Voltage	$-4V \le V_{IN} \le +2.4V$
Analog Input Current	50µA AVG, 10 mA peak
Logic Input Voltage	$-4V \le V_L \le +5.5V$

ELECTRICAL CHARACTERISTICS (V_S = ±8V DC, 0°C < T_A < 70°C, R_L = 10K, C_L = 30 pF, unless otherwise shown.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current	$\overline{CS}$ = 0 V+		-	11	14	mA
	V-		-	10.5	14	
	$\overline{CS}$ = 1 V+		-	0.4	0.58	
	V-		-	0.25	0.38	
Analog Output Voltage Swing	Extremes before clipping occurs		-	+2.0	-	V
			-	-1.2	-	
Output Offset voltage	75Ω on each input ground		-2	5	12	mV
Output Offset Drift	$\Delta V_{OSC} / \Delta T$		-	+50	+200	µV / °C
Address Logic Delay	Control input to appearance of signal on output		130	200	270	ns
Chip Selection Delay	Control input to appearance of signal on output		200	300	400	ns
Logic Input Threshold	1		-	-	1.1	V
	0		2	-	-	V
Logic Input Current	A0, A1 = 1		-	-	5.0	µA
	A0, A1 = 0		-	-	0.1	nA
	$\overline{CS}$ = 1		-	-	1.0	nA
	$\overline{CS}$ = 0		-	-	30.0	µA
Insertion Loss	1V p-p sine or sq.wave at 100 kHz		0.02	0.03	0.05	dB
Gain Spread at 8 MHz			-	-	±0.25	dB
Bandwidth (-3dB)			90	100	-	MHz
Differential Gain	at 3.58 or 4.43 MHz		-	0.03	0.05	%
Differential Phase	at 3.58 or 4.43 MHz		-	0.012	0.025	degrees
Input to Output Delay Matching (chip-chip)	75Ω source impedance at 3.579545 MHz	T_A = 25°	-	-	±0.6	degrees
		Full temp.	-	-	±1.0	degrees
All Hostile Crosstalk	Sweep on 3 inputs 1V p-p 4th input 10 Ω to gnd at 5 MHz		94	97	-	dB
Chip Disabled Crosstalk	14Ω on output to gnd at 10 MHz		100	110	-	dB
Input Resistance	$\overline{CS}$ = 0		-	960	-	kΩ
Input Capacitance	$\overline{CS}$ = 0		-	2.0	-	pF
	$\overline{CS}$ = 1		-	2.4	-	pF
Output Resistance	$\overline{CS}$ = 0		-	14	-	Ω
Output Capacitance	$\overline{CS}$ = 1		-	15	-	pF
Slew Rate	V_{IN} = 3V p-p (C_L = 0 pF)	+SR	-	40	-	V/µs
		-SR	-	40	-	V/µs

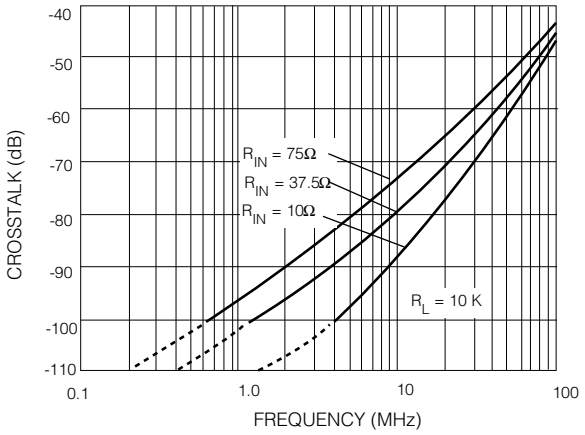


Fig. 1 Typical All Hostile Crosstalk Performance (14 pin DIP)

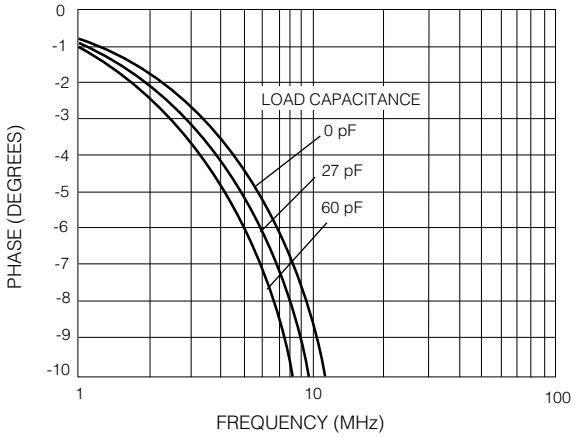


Fig. 2 Phase vs Frequency

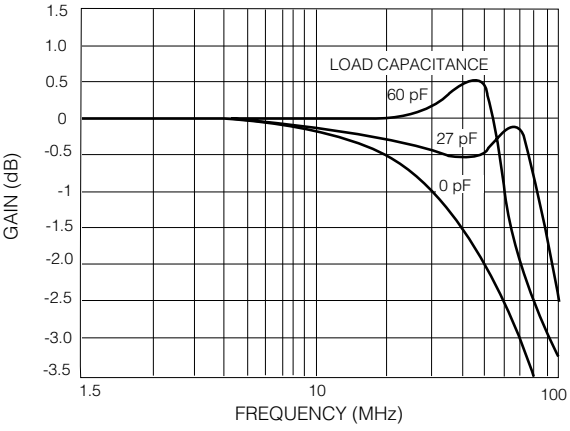


Fig. 3 Gain vs Frequency

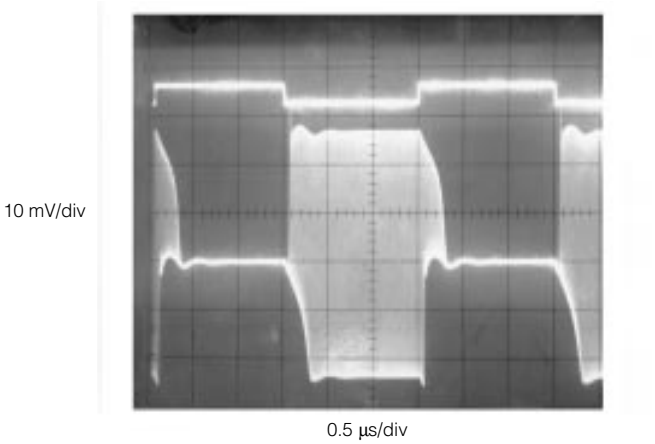


Fig. 4 Switching Transient (crosspoint-to-crosspoint)

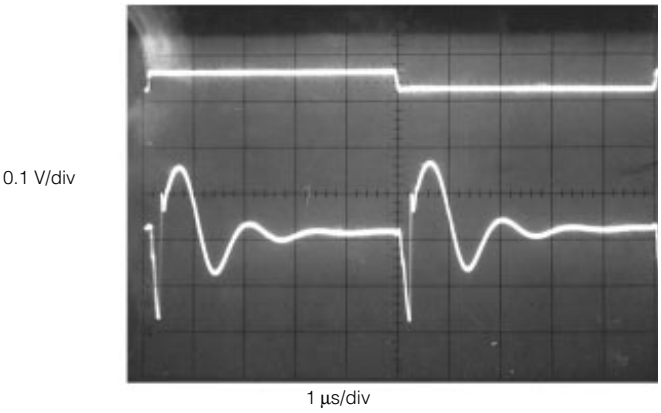


Fig. 5 Switching Envelope (crosspoint-to-crosspoint)

APPLICATION INFORMATION

As expected with any wide bandwidth circuit, the layout is critical. Good power supply regulation and bypassing are necessary, along with good high frequency design practice. Proper lead dress, component placement and PC board layout must be exercised for optimum performance.

The GX414A is non-inverting. Frequency peaking is compensated on-chip and optimised for a 60 pF load. The inputs are buffered and require 75Ω line terminating resistors when driven from 75Ω cable. The output must be buffered to drive 75Ω lines. The addition of an amplifier/buffer also allows adjustments to be made to the gain, offset and frequency response of the circuit. By reducing the load capacitance from 60 pF, the GX414A can be used to compensate for the frequency peaking of the buffer.

A typical application is shown in Figure 6 on the next page . Two GX414A devices are paralleled to form an 8x1 multiplexer switch. The three address lines make use of the A0, A1 and $\overline{CS}$ inputs. If more than two devices are used in parallel, a decoder will be necessary to generate the extra address inputs. Depending on the application and the speed of the logic family employed, latches may be required for synchronization where timing and delays are important.

The active switching circuitry of the GX414A will ensure low crosstalk and high performance over an input voltage range of -1.2 V to +2.0 V.

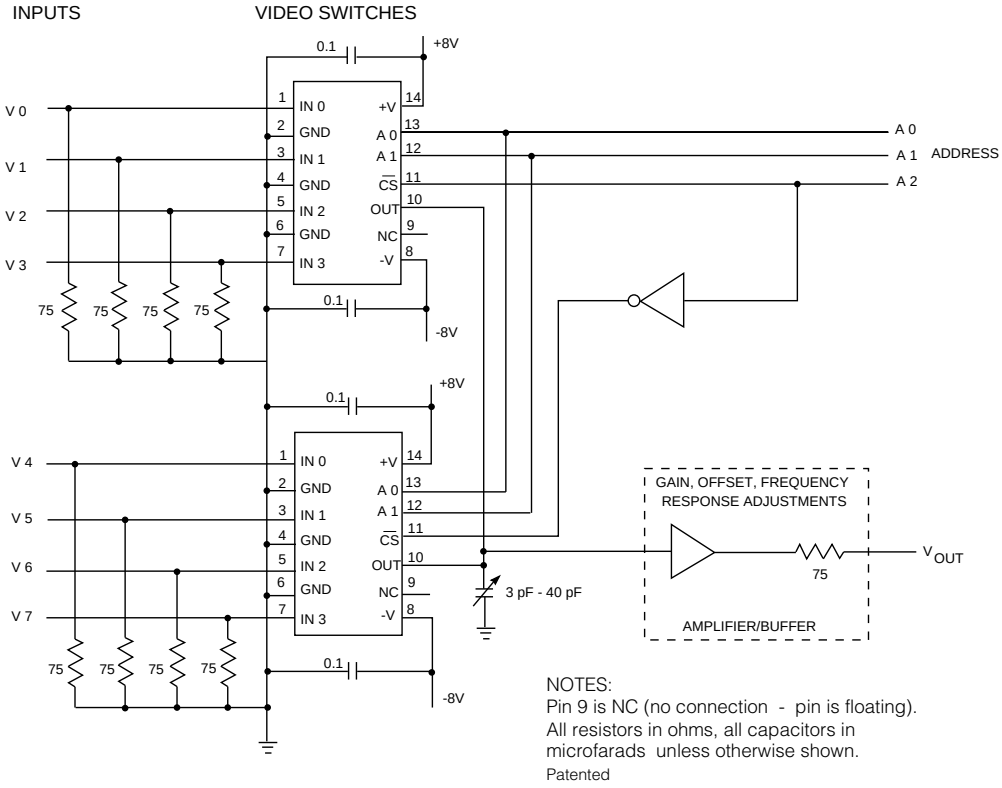


Fig. 6 Video Multiplexer Incorporating Two GX414As