

# BTA12-600BW3G, BTA12-800BW3G



**ON Semiconductor®**

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## Triacs Silicon Bidirectional Thyristors

Designed for high performance full-wave ac control applications where high noise immunity and high commutating di/dt are required.

### Features

- Blocking Voltage to 800 V
- On-State Current Rating of 12 A RMS at 25°C
- Uniform Gate Trigger Currents in Three Quadrants
- High Immunity to dV/dt – 2000 V/μs minimum at 125°C
- Minimizes Snubber Networks for Protection
- Industry Standard TO-220AB Package
- High Commutating dI/dt – 2.5 A/ms minimum at 125°C
- Internally Isolated (2500 V<sub>RMS</sub>)
- These Devices are Pb-Free and are RoHS Compliant\*

### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

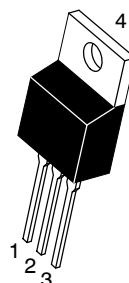
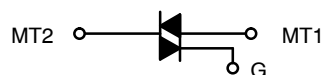
Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (Note 1) (T <sub>J</sub> = -40 to 125°C, Sine Wave, 50 to 60 Hz, Gate Open) BTA12-600BW3G BTA12-800BW3G	V <sub>DRM</sub> , V <sub>RRM</sub>	600 800	V
On-State RMS Current (Full Cycle Sine Wave, 60 Hz, T <sub>C</sub> = 80°C)	I <sub>T(RMS)</sub>	12	A
Peak Non-Repetitive Surge Current (One Full Cycle Sine Wave, 60 Hz, T <sub>C</sub> = 25°C)	I <sub>TSM</sub>	105	A
Circuit Fusing Consideration (t = 8.3 ms)	I <sup>2</sup> t	46	A <sup>2</sup> sec
Non-Repetitive Surge Peak Off-State Voltage (T <sub>J</sub> = 25°C, t = 10ms)	V <sub>DSM</sub> / V <sub>RSM</sub>	V <sub>DSM</sub> /V <sub>RSM</sub> +100	V
Peak Gate Current (T <sub>J</sub> = 125°C, t = 20ms)	I <sub>GM</sub>	4.0	A
Peak Gate Power (Pulse Width ≤ 1.0 μs, T <sub>C</sub> = 80°C)	P <sub>GM</sub>	20	W
Average Gate Power (T <sub>J</sub> = 125°C)	P <sub>G(AV)</sub>	1.0	W
Operating Junction Temperature Range	T <sub>J</sub>	-40 to +125	°C
Storage Temperature Range	T <sub>stg</sub>	-40 to +150	°C
RMS Isolation Voltage (t = 300 ms, R.H. ≤ 30%, T <sub>A</sub> = 25°C)	V <sub>iso</sub>	2500	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. V<sub>DRM</sub> and V<sub>RRM</sub> for all types can be applied on a continuous basis. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

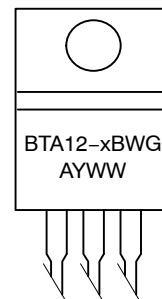
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## TRIACS 12 AMPERES RMS 600 thru 800 VOLTS



**TO-220AB  
CASE 221A  
STYLE 12**

### MARKING DIAGRAM



- x = 6 or 8
- A = Assembly Location (Optional)\*
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\* The Assembly Location code (A) is optional. In cases where the Assembly Location is stamped on the package the assembly code may be blank.

### PIN ASSIGNMENT

Pin	Assignment
1	Main Terminal 1
2	Main Terminal 2
3	Gate
4	No Connection

### ORDERING INFORMATION

Device	Package	Shipping
BTA12-600BW3G	TO-220AB (Pb-Free)	50 Units / Rail
BTA12-800BW3G	TO-220AB (Pb-Free)	50 Units / Rail

# BTA12-600BW3G, BTA12-800BW3G

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case (AC)	$R_{\theta JC}$	2.5	$^{\circ}\text{C}/\text{W}$
Junction-to-Ambient	$R_{\theta JA}$	60	
Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 10 seconds	$T_L$	260	$^{\circ}\text{C}$

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^{\circ}\text{C}$ unless otherwise noted; Electricals apply in both directions)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Peak Repetitive Blocking Current ( $V_D = \text{Rated } V_{DRM}, V_{RRM}; \text{ Gate Open}$ )	$I_{DRM}, I_{RRM}$	-	-	0.005 2.0	mA
					$T_J = 25^{\circ}\text{C}$
					$T_J = 125^{\circ}\text{C}$

### ON CHARACTERISTICS

Peak On-State Voltage (Note 2) ( $I_{TM} = \pm 17 \text{ A Peak}$ )	$V_{TM}$	-	-	1.55	V
Gate Trigger Current (Continuous dc) ( $V_D = 12 \text{ V}, R_L = 30 \Omega$ )	$I_{GT}$	2.5	-	50	mA
MT2(+), G(+)		2.5	-	50	
MT2(+), G(-)		2.5	-	50	
MT2(-), G(-)		2.5	-	50	
Holding Current ( $V_D = 12 \text{ V}, \text{ Gate Open}, \text{ Initiating Current} = \pm 100 \text{ mA}$ )	$I_H$	-	-	50	mA
Latching Current ( $V_D = 12 \text{ V}, I_G = 60 \text{ mA}$ )	$I_L$	-	-	70	mA
MT2(+), G(+)		-	-	80	
MT2(+), G(-)		-	-	70	
MT2(-), G(-)		-	-	70	
Gate Trigger Voltage ( $V_D = 12 \text{ V}, R_L = 30 \Omega$ )	$V_{GT}$	0.5	-	1.7	V
MT2(+), G(+)		0.5	-	1.1	
MT2(+), G(-)		0.5	-	1.1	
MT2(-), G(-)		0.5	-	1.1	
Gate Non-Trigger Voltage ( $T_J = 125^{\circ}\text{C}$ )	$V_{GD}$	0.2	-	-	V
MT2(+), G(+)		0.2	-	-	
MT2(+), G(-)		0.2	-	-	
MT2(-), G(-)		0.2	-	-	

### DYNAMIC CHARACTERISTICS

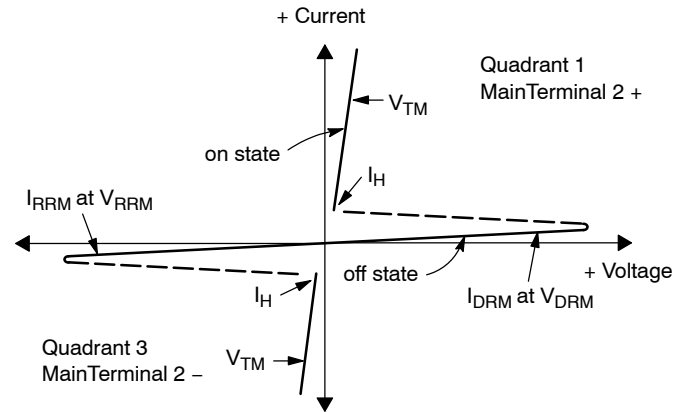
Rate of Change of Commutating Current, See Figure 10. (Gate Open, $T_J = 125^{\circ}\text{C}$ , No Snubber)	$(di/dt)_c$	2.5	-	-	A/ms
Critical Rate of Rise of On-State Current ( $T_J = 125^{\circ}\text{C}, f = 120 \text{ Hz}, I_G = 2 \times I_{GT}, tr \leq 100 \text{ ns}$ )	$di/dt$	-	-	50	A/ $\mu\text{s}$
Critical Rate of Rise of Off-State Voltage ( $V_D = 0.66 \times V_{DRM}, \text{ Exponential Waveform}, \text{ Gate Open}, T_J = 125^{\circ}\text{C}$ )	$dV/dt$	2000	-	-	V/ $\mu\text{s}$

2. Indicates Pulse Test: Pulse Width  $\leq 2.0 \text{ ms}$ , Duty Cycle  $\leq 2\%$ .

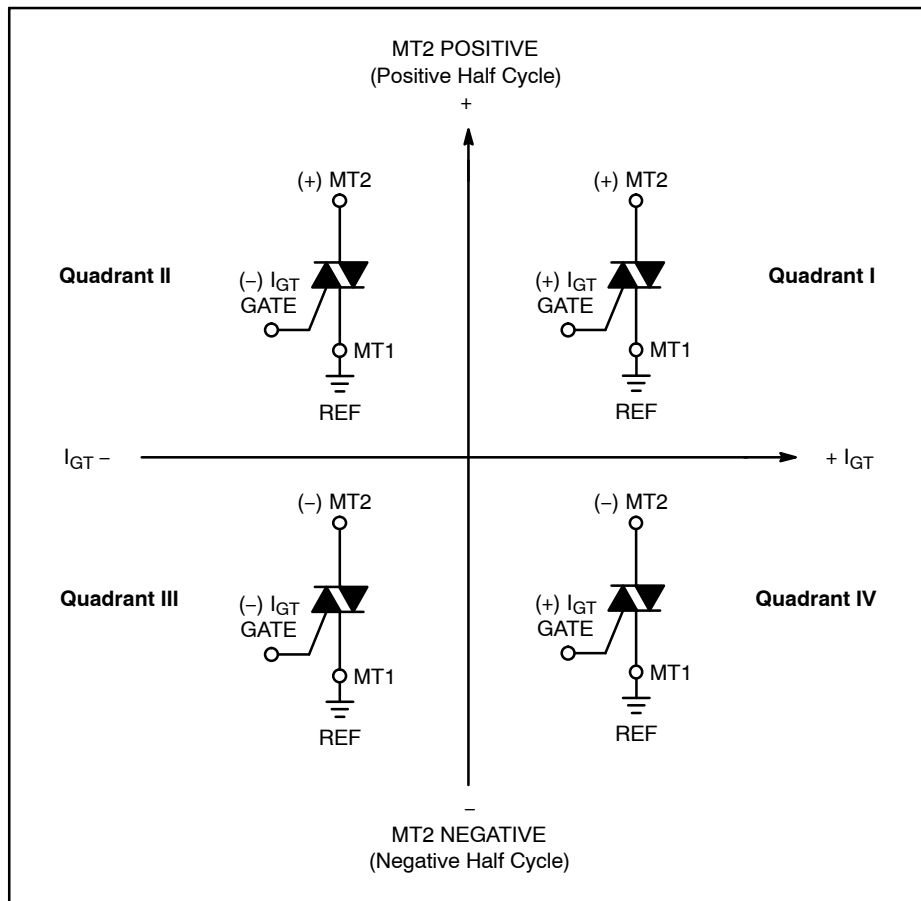
# BTA12-600BW3G, BTA12-800BW3G

## Voltage Current Characteristic of Triacs (Bidirectional Device)

Symbol	Parameter
$V_{DRM}$	Peak Repetitive Forward Off State Voltage
$I_{DRM}$	Peak Forward Blocking Current
$V_{RRM}$	Peak Repetitive Reverse Off State Voltage
$I_{RRM}$	Peak Reverse Blocking Current
$V_{TM}$	Maximum On State Voltage
$I_H$	Holding Current



### Quadrant Definitions for a Triac



All polarities are referenced to MT1.

With in-phase signals (using standard AC lines) quadrants I and III are used.

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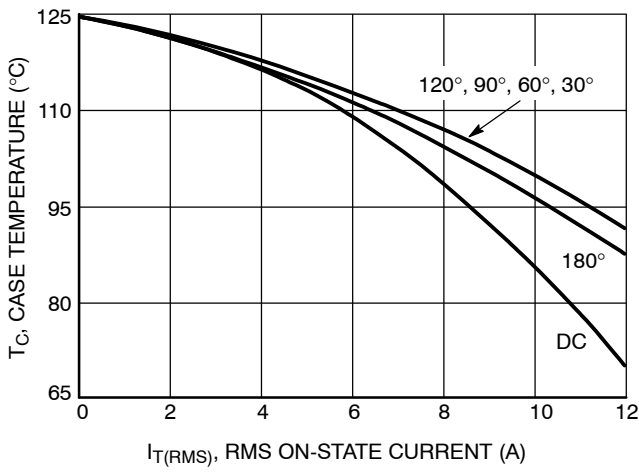


Figure 1. RMS Current Derating

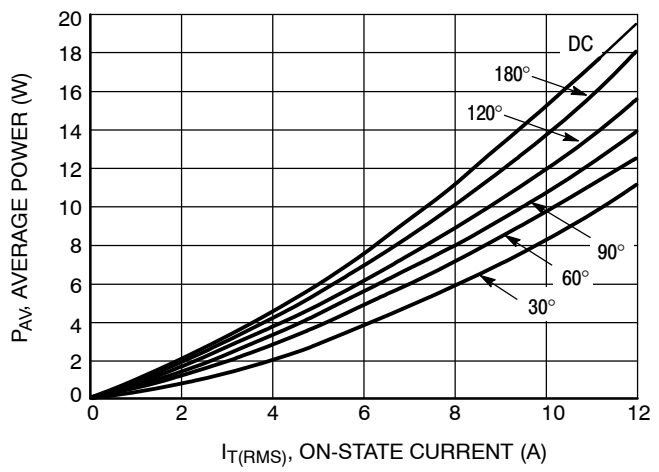


Figure 2. On-State Power Dissipation

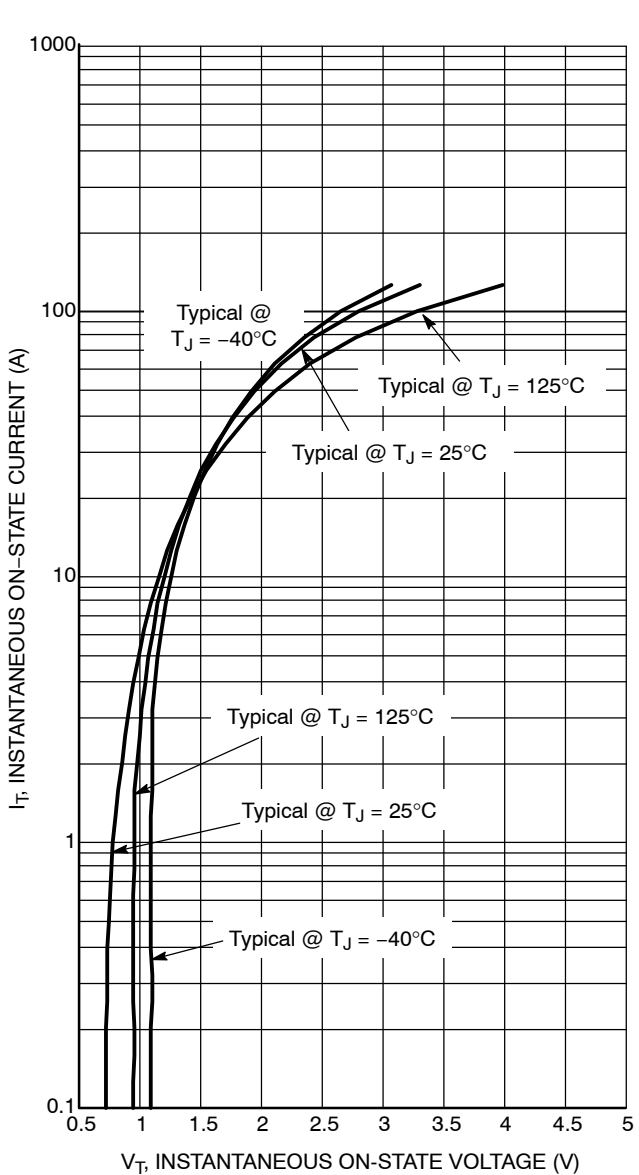


Figure 3. On-State Characteristics

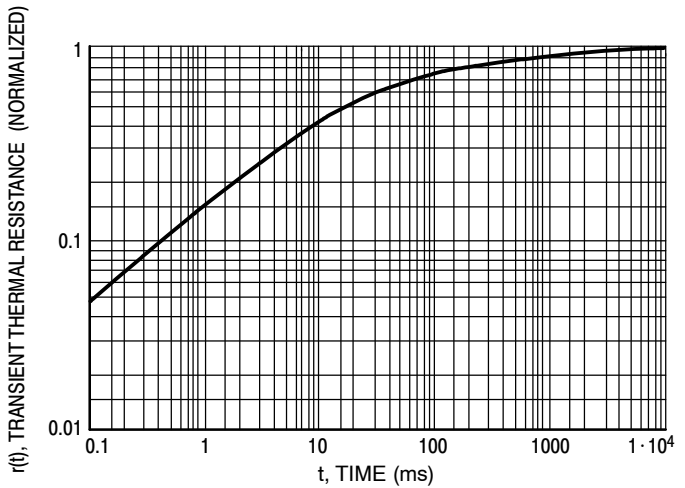


Figure 4. Thermal Response

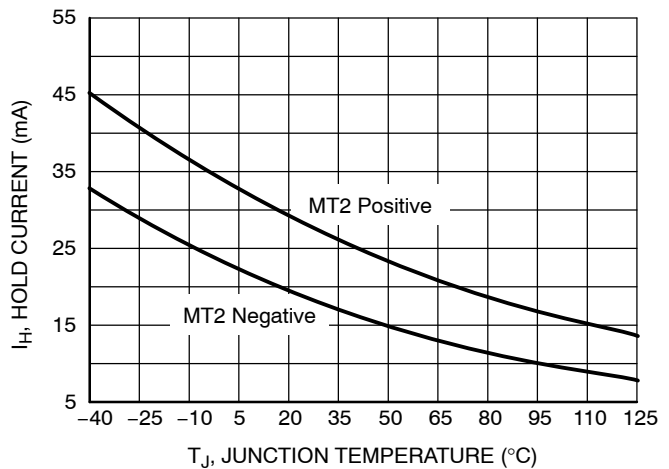


Figure 5. Hold Current Variation

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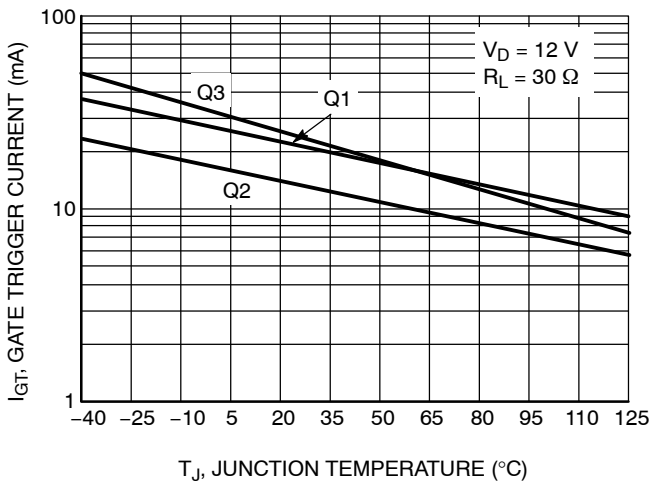


Figure 6. Gate Trigger Current Variation

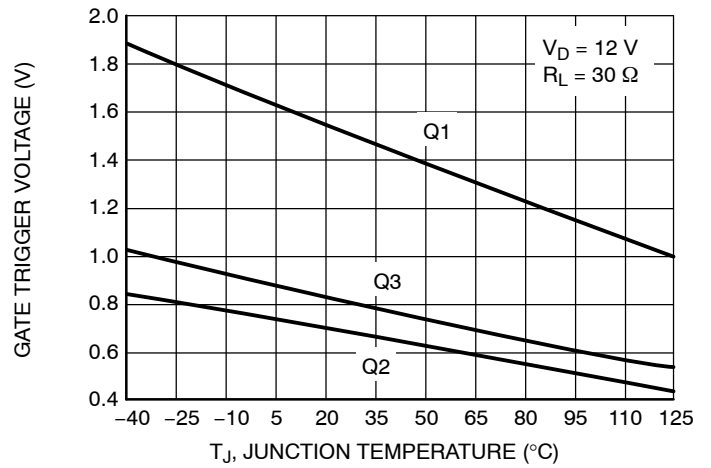


Figure 7. Gate Trigger Voltage Variation

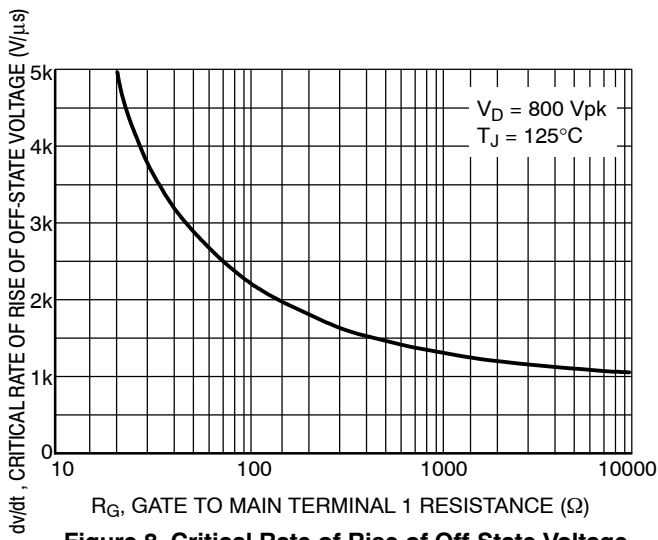


Figure 8. Critical Rate of Rise of Off-State Voltage (Exponential Waveform)

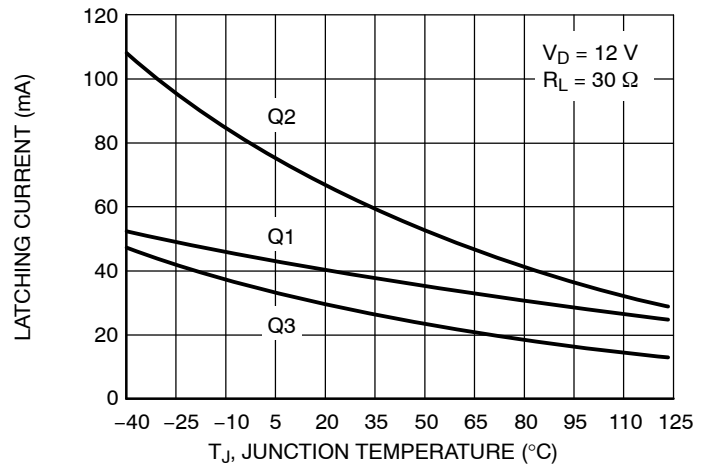
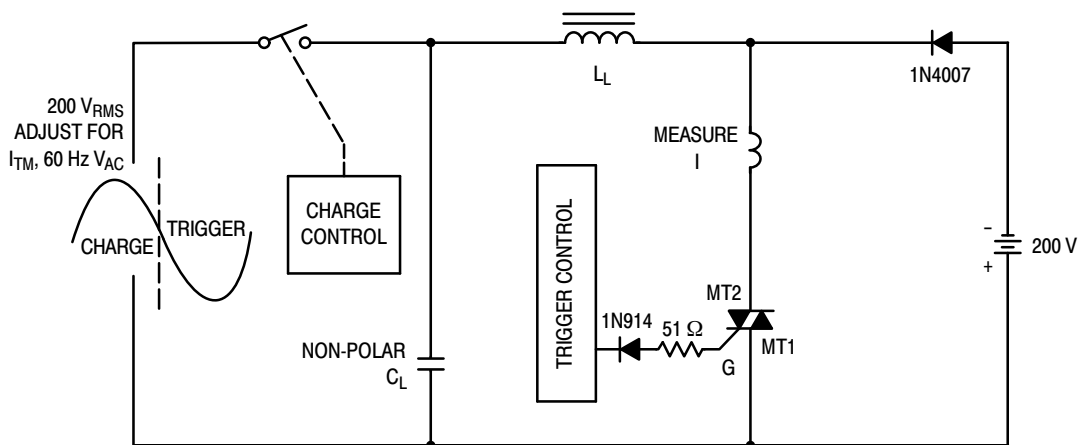


Figure 10. Latching Current Variation



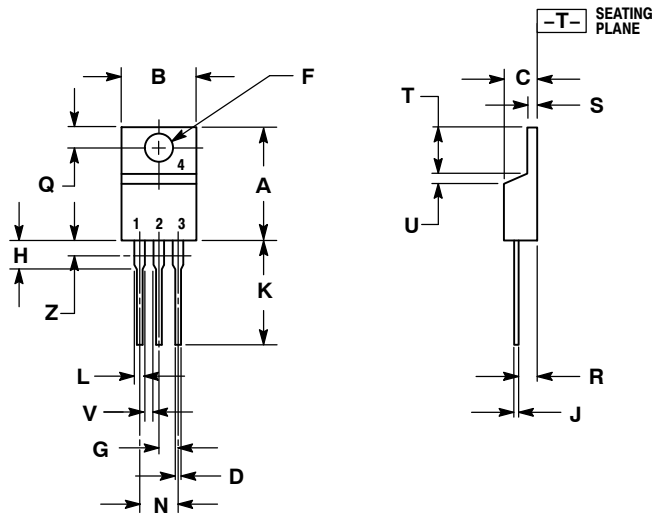
Note: Component values are for verification of rated  $(di/dt)_c$ . See AN1048 for additional information.

Figure 9. Simplified Test Circuit to Measure the Critical Rate of Rise of Commutating Current  $(di/dt)_c$

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## PACKAGE DIMENSIONS

TO-220  
CASE 221A-07  
ISSUE AA




### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.014	0.022	0.36	0.55
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

### STYLE 12:

1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. NOT CONNECTED

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