19-1467; Rev 2; 12/05

MAXIM

+3.3V, 2.488Gbps, SDH/SONET 1:16 Deserializer with Clock Recovery

General Description

The MAX3880 deserializer with clock recovery is ideal for converting 2.488Gbps serial data to 16-bit-wide, 155Mbps parallel data for SDH/SONET applications. Operating from a single +3.3V supply, this device accepts high-speed serial-data inputs and delivers low-voltage differential-signal (LVDS) parallel clock and data outputs for interfacing with digital circuitry.

The MAX3880 includes a low-power clock recovery and data retiming function for 2.488Gbps applications. The fully integrated phase-locked loop (PLL) recovers a synchronous clock signal from the serial NRZ data input; the signal is then retimed by the recovered clock. The MAX3880's jitter performance exceeds all SDH/SONET specifications. An additional 2.488Gbps serial input is available for system loopback diagnostic testing. The device also includes a TTL-compatible loss-of-lock ($\overline{LOL}$) monitor and LVDS synchronization inputs that enable data realignment and reframing.

The MAX3880 is available in the extended temperature range (-40°C to +85°C) in a 64-pin TQFP-EP (exposed pad) package.

Applications

2.488Gbps SDH/SONET Transmission Systems

Add/Drop Multiplexers

Digital Cross-Connects

Features

- **Single +3.3V Supply**
- **910mW Operating Power**
- **Fully Integrated Clock Recovery and Data Retiming**
- **Exceeds ANSI, ITU, and Bellcore Specifications**
- **Additional High-Speed Input Facilitates System Loopback Diagnostic Testing**
- **2.488Gbps Serial to 155Mbps Parallel Conversion**
- **LVDS Data Outputs and Synchronization Inputs**
- **Tolerates >2000 Consecutive Identical Digits**
- **Loss-of-Lock Indicator**

Ordering Information

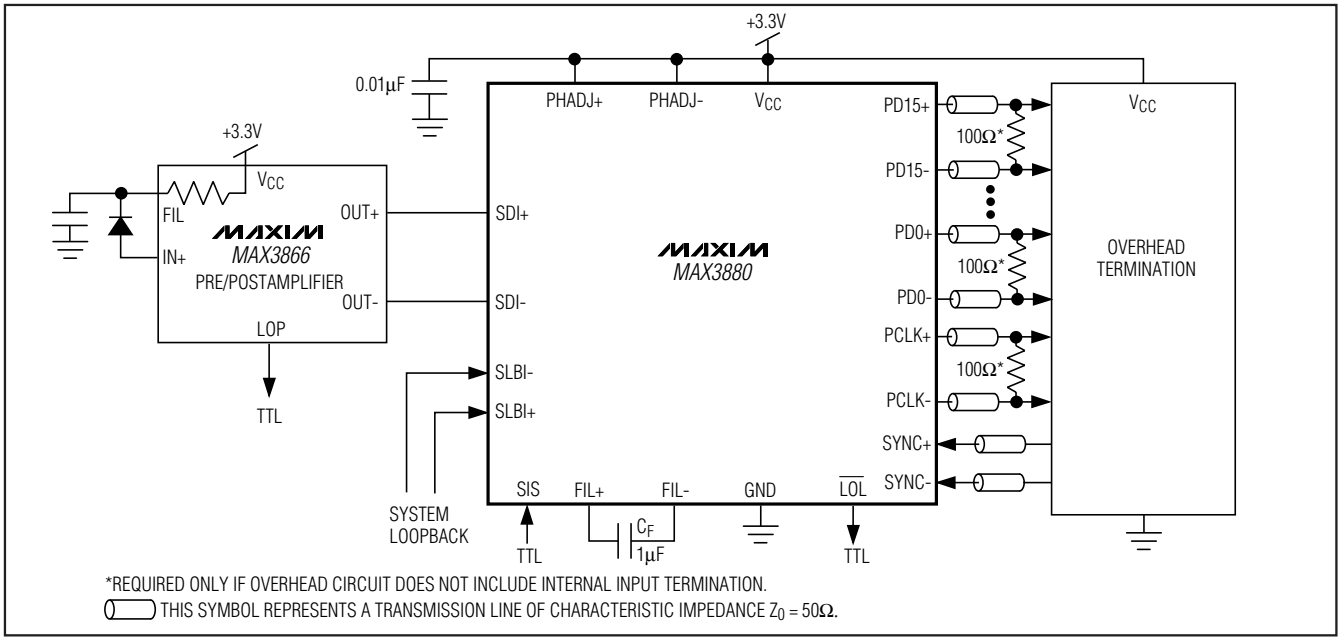
PART	TEMP. RANGE	PIN-PACKAGE
MAX3880ECB	-40°C to +85°C	64 TQFP-EP*
MAX3880ECB+	-40°C to +85°C	64 TQFP-EP*

Exposed pad

+Denotes lead-free package.

Pin Configuration appears at end of data sheet.

Typical Application Circuit



+3.3V, 2.488Gbps, SDH/SONET 1:16 Deserializer with Clock Recovery

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (V_{CC}).....-0.5V to +7.0V
Input Voltage Level (SDI+, SDI-, SLBI+, SLBI-, SYNC+, SYNC-)..... (V_{CC} - 0.5V) to (V_{CC} + 0.5V)
Input Current Level (SDI+, SDI-, SLBI+, SLBI-).....±10mA
Voltage at $\overline{LOL}$, SIS, PHADJ+, PHADJ-, FIL+, FIL-.....-0.5V to (V_{CC} + 0.5V)
Output Current LVDS Outputs 10mA
Continuous Power Dissipation (T_A = +85°C)
TQFP (derate 33.3mW/°C above +85°C).....1.44W
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-55°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, differential loads = 100Ω ±1%, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}			275	380	mA
SERIAL DATA INPUTS (SDI±, SLBI±)						
Differential Input Voltage	V_{ID}	Figure 1	50		800	mVp-p
Single-Ended Input Voltage	V_{IS}		V_{CC} - 0.4		V_{CC} + 0.2	V
Input Termination to Vcc	R_{IN}			50		Ω
LVDS INPUTS AND OUTPUTS (SYNC±, PCLK±, PD_±)						
Input Voltage Range	V_I	Differential input voltage = 100mV	0		2.4	V
Differential Input Threshold	V_{IDTH}	Common-mode voltage = 50mV	-100		100	mV
Threshold Hysteresis	V_{HYST}			78		mV
Differential Input Resistance	R_{IN}		85	100	115	Ω
Output High Voltage	V_{OH}				1.475	V
Output Low Voltage	V_{OL}		0.925			V
Differential Output Voltage	$\|V_{OD}\|$	Figure 2	250		400	mV
Change in Magnitude of Differential Output Voltage for Complementary States	$\Delta\|V_{OD}\|$				±25	mV
Output Offset Voltage	V_{OS}		1.125		1.275	V
Change in Magnitude of Output Offset Voltage for Complementary States	ΔV_{OS}				±25	mV
Single-Ended Output Resistance	R_O		40	95	140	Ω
Change in Magnitude of Single-Ended Output Resistance for Complementary Outputs	ΔR_O			±2.5	±10	%
TTL INPUTS AND OUTPUTS (SIS, $\overline{LOL}$)						
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.8	V
Input Current			-10		+10	µA
Output High Voltage	V_{OH}		2.4		V_{CC}	V
Output Low Voltage	V_{OL}				0.4	V

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, differential loads = 100Ω ±1%, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Data Rate	SDI			2.488		Gbps
Parallel Output Data Rate				155.52		Mbps
Parallel Clock-to-Data Output Delay	t_{CLK-Q}	Figure 5	200	450	900	ps
Jitter Tolerance		f = 70kHz (Note 2)	2.31	3.3		UIp-p
		f = 100kHz	1.74	2.41		
		f = 1MHz	0.38	0.57		
		f = 10MHz	0.28	0.46		
Tolerated Consecutive Identical Digits				>2,000		Bits
Input Return Loss (SDI±, SLBI±)		100kHz to 2.5GHz		-18		dB
		2.5GHz to 4.0GHz		-11		

Note 1: AC characteristics are guaranteed by design and characterization.

Note 2: At jitter frequencies <70kHz, the jitter tolerance characteristics exceed the ITU/Bellcore specifications. The low-frequency jitter tolerance outperforms the instrument's measurement capability.

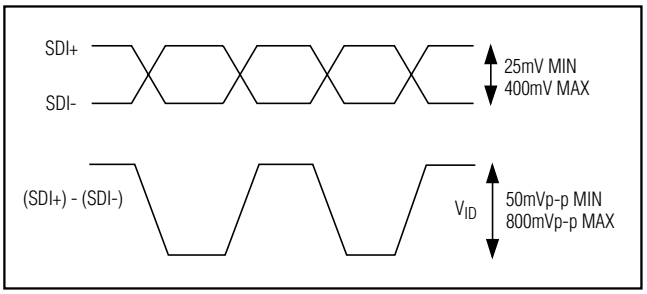


Figure 1. Input Amplitude

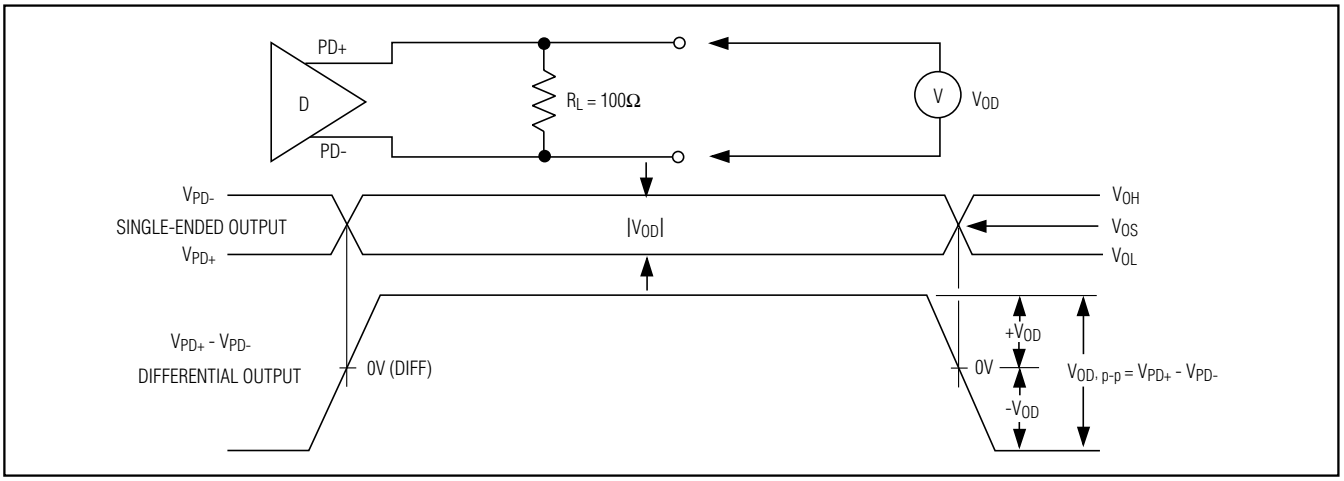


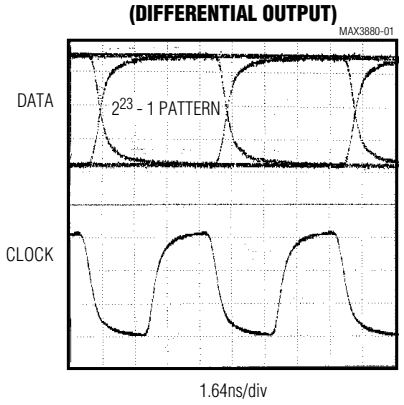
Figure 2. Driver Output Levels

+3.3V, 2.488Gbps, SDH/SONET 1:16 Deserializer with Clock Recovery

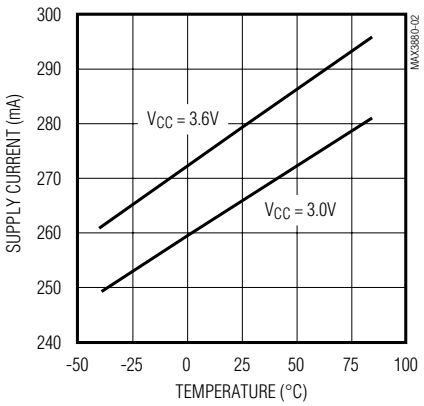
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

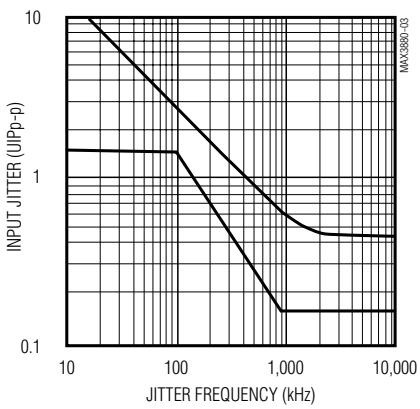
RECOVERED DATA AND CLOCK (DIFFERENTIAL OUTPUT)



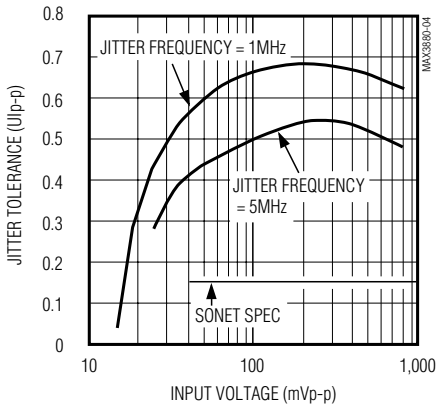
SUPPLY CURRENT vs. TEMPERATURE



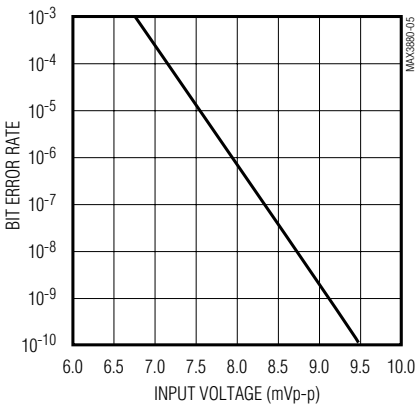
JITTER TOLERANCE



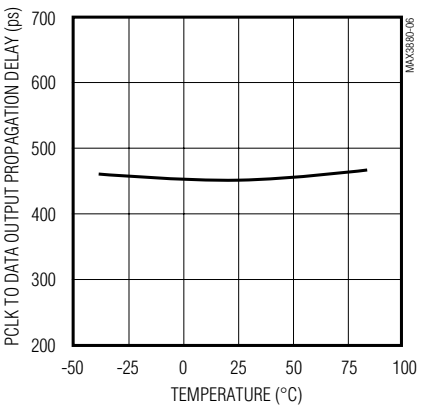
JITTER TOLERANCE vs. INPUT VOLTAGE



BIT ERROR RATE vs. INPUT VOLTAGE



PARALLEL CLOCK TO DATA OUTPUT PROPAGATION DELAY vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1, 17, 25, 33, 41, 49, 56, 62, 64	GND	Ground
2	FIL+	Positive Filter Input. PLL loop filter connection. Connect a 1.0µF capacitor between FIL+ and FIL-.
3	FIL-	Negative Filter Input. PLL loop filter connection. Connect a 1.0µF capacitor between FIL+ and FIL-.
4, 7, 10, 13, 24, 32, 40, 48, 57	V_{CC}	+3.3V Supply Voltage
5	PHADJ+	Positive Phase-Adjust Input. Used to optimally align internal PLL phase. Connect to V_{CC} if not used.
6	PHADJ-	Negative Phase-Adjust Input. Used to optimally align internal PLL phase. Connect to V_{CC} if not used.
8	SDI+	Positive Serial Data Input. 2.488Gbps data stream.
9	SDI-	Negative Serial Data Input. 2.488Gbps data stream.
11	SLBI+	Positive System Loopback Input. 2.488Gbps data stream.
12	SLBI-	Negative System Loopback Input. 2.488Gbps data stream.
14	SIS	Signal Input Selection. TTL low for normal data input (SDI). TTL high for system loopback input (SLBI).
15	SYNC-	Negative Synchronizing Pulse LVDS Input. Pulse the SYNC signal high for at least four serial-data bit periods (1.6ns) to shift the data alignment by dropping 1 bit.
16	SYNC+	Positive Synchronizing Pulse LVDS Input. Pulse the SYNC signal high for at least four serial-data bit periods (1.6ns) to shift the data alignment by dropping 1 bit.
18	PCLK-	Negative Parallel Clock LVDS Output
19	PCLK+	Positive Parallel Clock LVDS Output
20, 22, 26, 28, 30, 34, 36, 38, 42, 44, 46, 50, 52, 54, 58, 60	PD0- to PD15-	Negative Parallel Data LVDS Outputs. Data is updated on the negative transition of the PCLK signal (Figure 5).
21, 23, 27, 29, 31, 35, 37, 39, 43, 45, 47, 51, 53, 55, 59, 61	PD0+ to PD15+	Positive Parallel Data LVDS Outputs. Data is updated on the negative transition of the PCLK signal (Figure 5).
63	$\overline{LOL}$	Loss-of-Lock Output. PLL loss-of-lock monitor, TTL active low (internal 10kΩ pull-up resistor). The $\overline{LOL}$ monitor is valid only when a data stream is present on the inputs to the MAX3880.
EP	Exposed Pad	Ground. This must be soldered to a circuit board for proper thermal performance (see *Package Information*).

+3.3V, 2.488Gbps, SDH/SONET 1:16 Deserializer with Clock Recovery

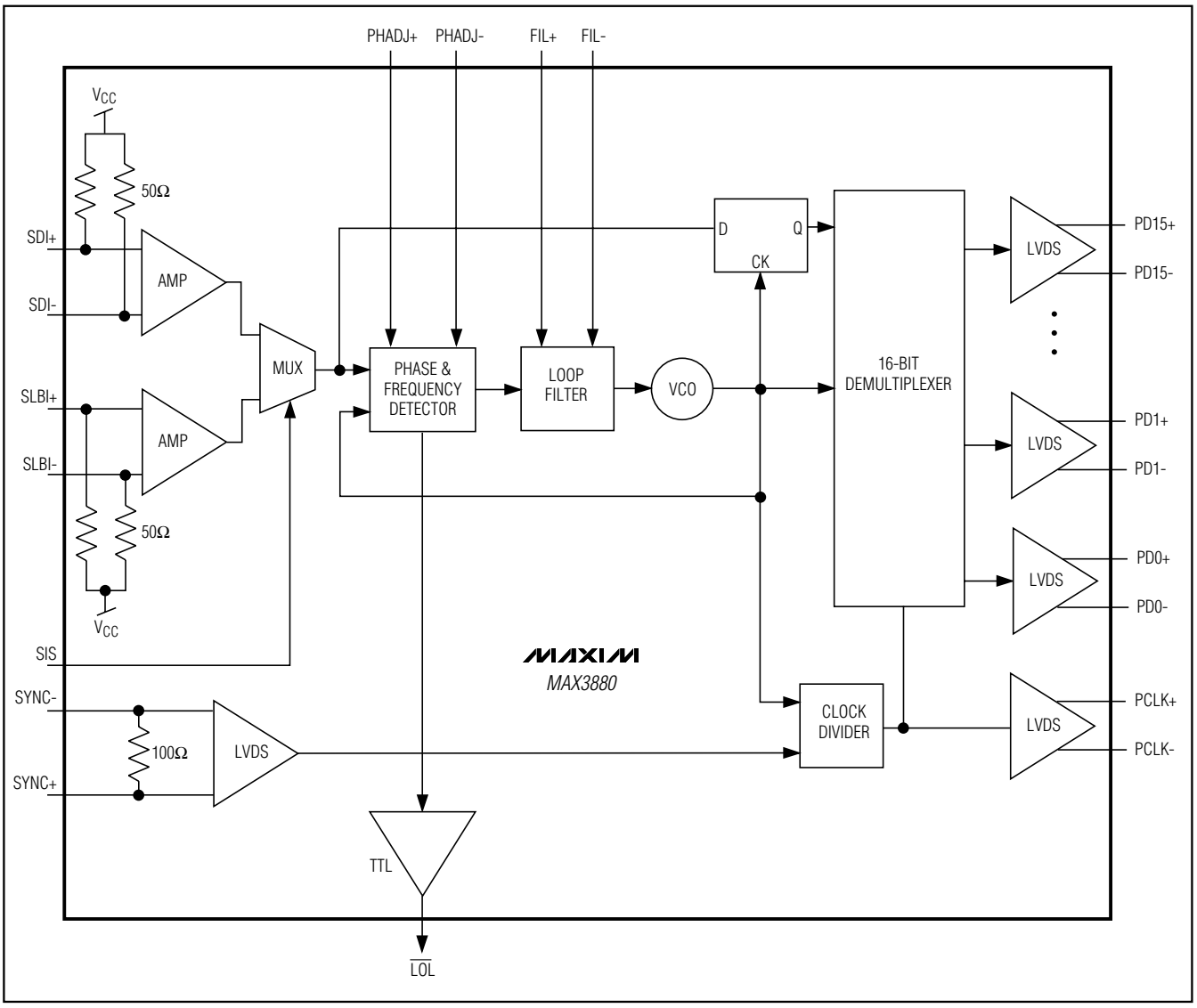


Figure 3. MAX3880 Functional Diagram

Detailed Description

The MAX3880 deserializer with clock recovery converts 2.488Gbps serial data to 16-bit-wide, 155Mbps parallel data. The device combines a fully integrated phase-locked loop (PLL), input amplifier, data retiming block, 16-bit demultiplexer, clock divider, and LVDS output buffer (Figure 3). The PLL consists of a phase/frequency detector (PFD), a loop filter, and a voltage-controlled oscillator (VCO). The MAX3880 is designed to deliver the best combination of jitter performance and power dissipation by using a fully differential signal architecture and low-noise design techniques. The PLL recovers the serial clock from the serial input data stream. The demultiplexer generates a 16-bit-wide 155Mbps parallel data output.

The synchronization inputs (SYNC+, SYNC-) realign the output data word. Realignment is guaranteed to occur within two complete PCLK cycles of the SYNC signal's positive transition. During synchronization, the first incoming bit of data during that PCLK cycle is

dropped, shifting the alignment between PCLK and data by 1 bit. The SYNC signal must be at least four serial bit periods wide (4 x 402ps). See Figure 4 for the timing diagram and Figure 5 for the timing parameters diagram.

Input Amplifier

The input amplifiers on both the main data and system loopback accept a differential input amplitude from 50mVp-p to 800mVp-p. The bit error rate (BER) is better than 1×10^{-10} for input signals as small as 9.5mVp-p, although the jitter tolerance performance will be degraded. For interfacing with PECL signal levels, see *Applications Information*.

Phase Detector

The phase detector in the MAX3880 produces a voltage proportional to the phase difference between the incoming data and the internal clock. Because of its feedback nature, the PLL drives the error voltage to zero, aligning the recovered clock to the center of the incoming data eye for retiming. The external phase adjust pins (PHADJ+, PHADJ-) allow the user to vary the internal phase alignment.

Frequency Detector

The digital frequency detector (FD) aids frequency acquisition during start-up conditions. The frequency difference between the received data and the VCO clock is derived by sampling the in-phase and quadrature VCO outputs on both edges of the data input signal. Depending on the polarity of the frequency difference, the FD drives the VCO until the frequency difference is reduced to zero. Once frequency acquisition is complete, the FD returns to a neutral state. False locking is completely eliminated by this digital frequency detector.

Loop Filter and VCO

The phase detector and frequency detector outputs are summed into the loop filter. A 1.0µF capacitor, C_F, is required to set the PLL damping ratio.

The loop filter output controls the on-chip LC VCO running at 2.488GHz. The VCO provides low phase noise and is trimmed to the correct frequency.

Loss-of-Lock Monitor

A loss-of-lock ($\overline{LOL}$) monitor is included in the MAX3880 frequency detector. A loss-of-lock condition is signaled immediately with a TTL low. When the PLL is frequency-locked, $\overline{LOL}$ switches to TTL high in approximately 800ns.

Note that the $\overline{LOL}$ monitor is only valid when a data stream is present on the inputs to the MAX3880. As a result, $\overline{LOL}$ does not detect a loss-of-power condition resulting from a loss of the incoming signal.

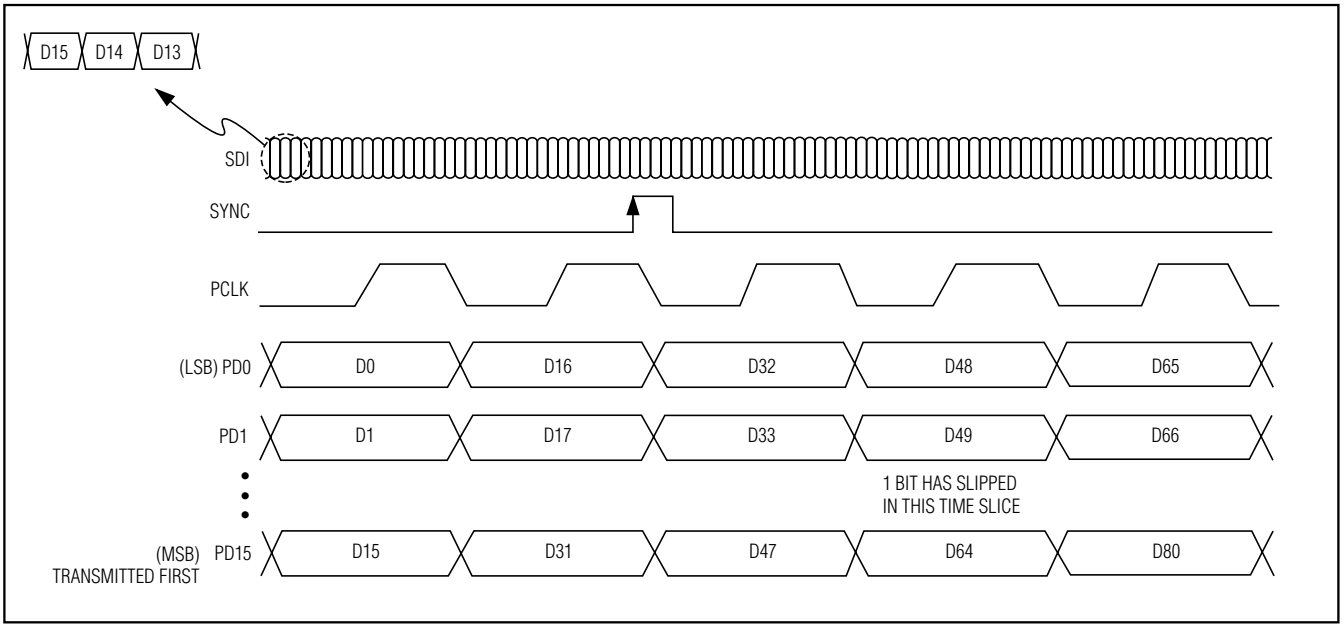


Figure 4. Timing Diagram

+3.3V, 2.488Gbps, SDH/SONET 1:16 Deserializer with Clock Recovery

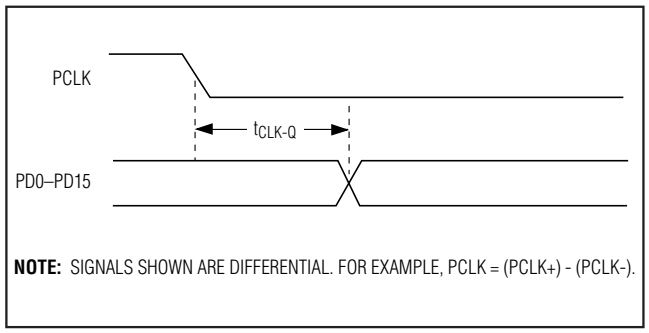


Figure 5. Timing Parameters

Low-Voltage Differential-Signal (LVDS) Inputs and Outputs

The MAX3880 features LVDS inputs and outputs for interfacing with high-speed digital circuitry. The LVDS standard is based on the IEEE 1596.3 LVDS specification. This technology uses 500mVp-p to 800mVp-p differential low-voltage swings to achieve fast transition times, minimize power dissipation, and improve noise immunity. For proper operation, the parallel clock and data LVDS outputs (PCLK+, PCLK-, PD_+, PD_-) require 100Ω differential DC termination between the positive and negative outputs. Do not terminate these outputs to ground. The synchronization LVDS inputs (SYNC+, SYNC-) are internally terminated with 100Ω differential input resistance and therefore do not require external termination.

Design Procedure

Jitter Tolerance and Input Sensitivity Trade-Offs

When the received data amplitude is higher than 50mVp-p, the MAX3880 provides a typical jitter tolerance of 0.46 UI at jitter frequencies greater than 10MHz. The SDH/SONET jitter tolerance specification is 0.15UI, leaving a jitter allowance of 0.31UI for receiver preamplifier and postamplifier design.

The BER is better than 1 x 10^{-10} for input signals greater than 9.5mVp-p. At 25mVp-p, jitter tolerance will be degraded, but will still be above the SDH/SONET requirement. Trade-offs can be made between jitter tolerance and input sensitivity according to the specific application. See the *Typical Operating Characteristics* for Jitter Tolerance and BER vs. Input Voltage graphs.

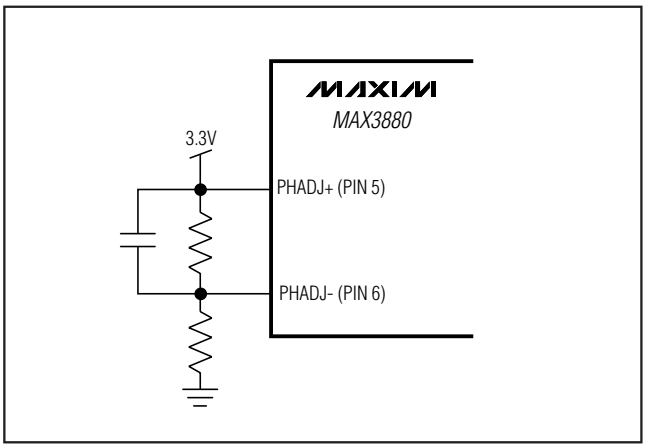


Figure 6. Phase-Adjust Resistor-Divider

Applications Information

Consecutive Identical Digits (CIDs)

The MAX3880 has a low phase and frequency drift in the absence of data transitions. As a result, long runs of consecutive zeros and ones can be tolerated while maintaining a BER of 1 x 10^{-10}. The CID tolerance is tested using a 2^{13} - 1 pseudorandom bit stream (PRBS), substituting a long run of zeros to simulate the worst case. A CID tolerance of greater than 2,000 bits is typical.

Phase Adjust

The internal clock is aligned to the center of the data eye. For specific applications, this sampling position can be shifted using the PHADJ inputs to optimize BER performance. The PHADJ inputs operate with differential input voltages up to ±1.5V. A simple resistor-divider with a bypass capacitor is sufficient to set these levels (Figure 6). When the PHADJ inputs are not used, they should be tied directly to V_{CC}.

System Loopback

The MAX3880 is designed to allow system loopback testing. The user can connect a serializer output (MAX3890) in a transceiver directly to the SLBI+ and SLBI- inputs of the MAX3880 for system diagnostics. To select the SLBI± inputs, apply a TTL logic high to the SIS pin.

Interfacing with PECL Input Levels

When interfacing with differential PECL input levels, it is important to attenuate the signal while still maintaining 50Ω termination (Figure 7). AC-coupling is also required to maintain the input common-mode level.

Layout Techniques

For best performance, use good high-frequency layout techniques. Filter voltage supplies, keep ground connections short, and use multiple vias where possible. Use controlled impedance transmission lines to interface with the MAX3880 high-speed inputs and outputs. Power-supply decoupling should be placed as close to V_{CC} as possible. To reduce feedthrough, take care to isolate the input signals from the output signals.

Chip Information

TRANSISTOR COUNT: 4102

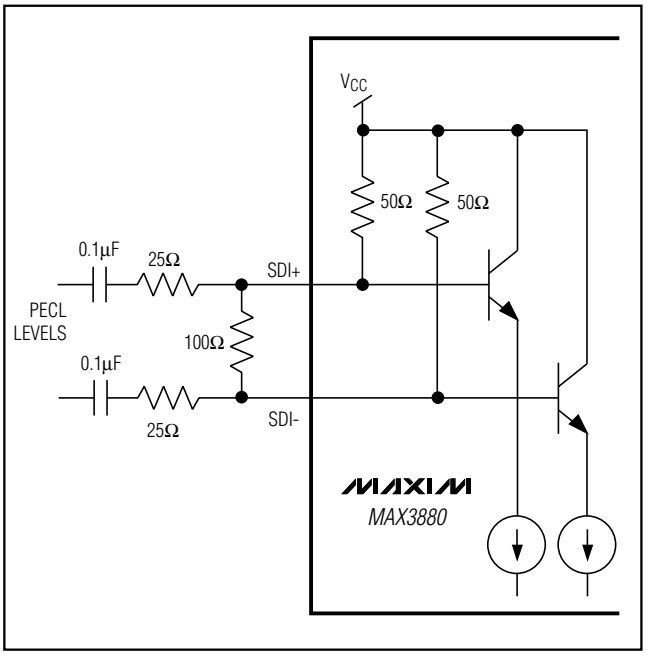
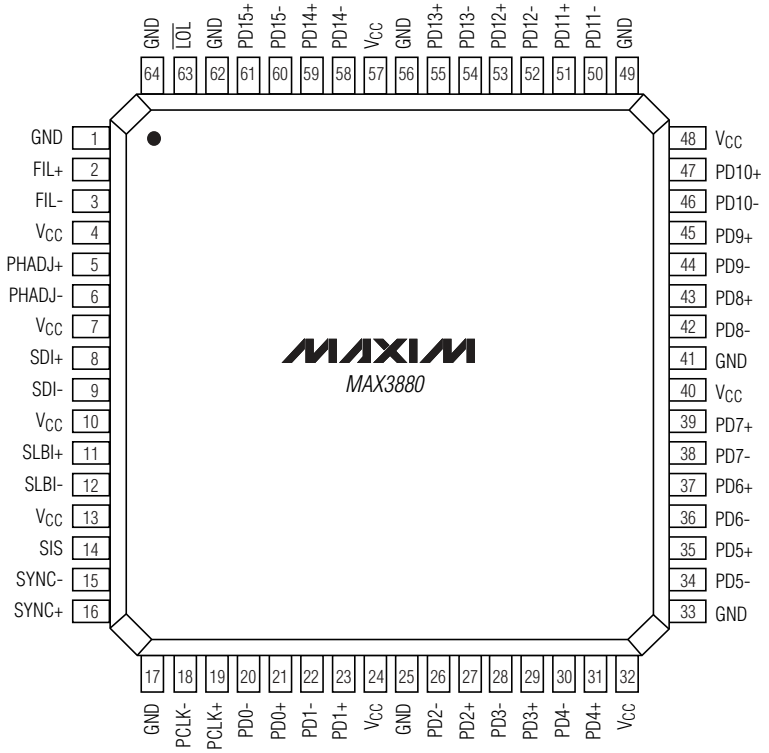


Figure 7. Interfacing with PECL Input Levels

+3.3V, 2.488Gbps, SDH/SONET 1:16 Deserializer with Clock Recovery

Pin Configuration



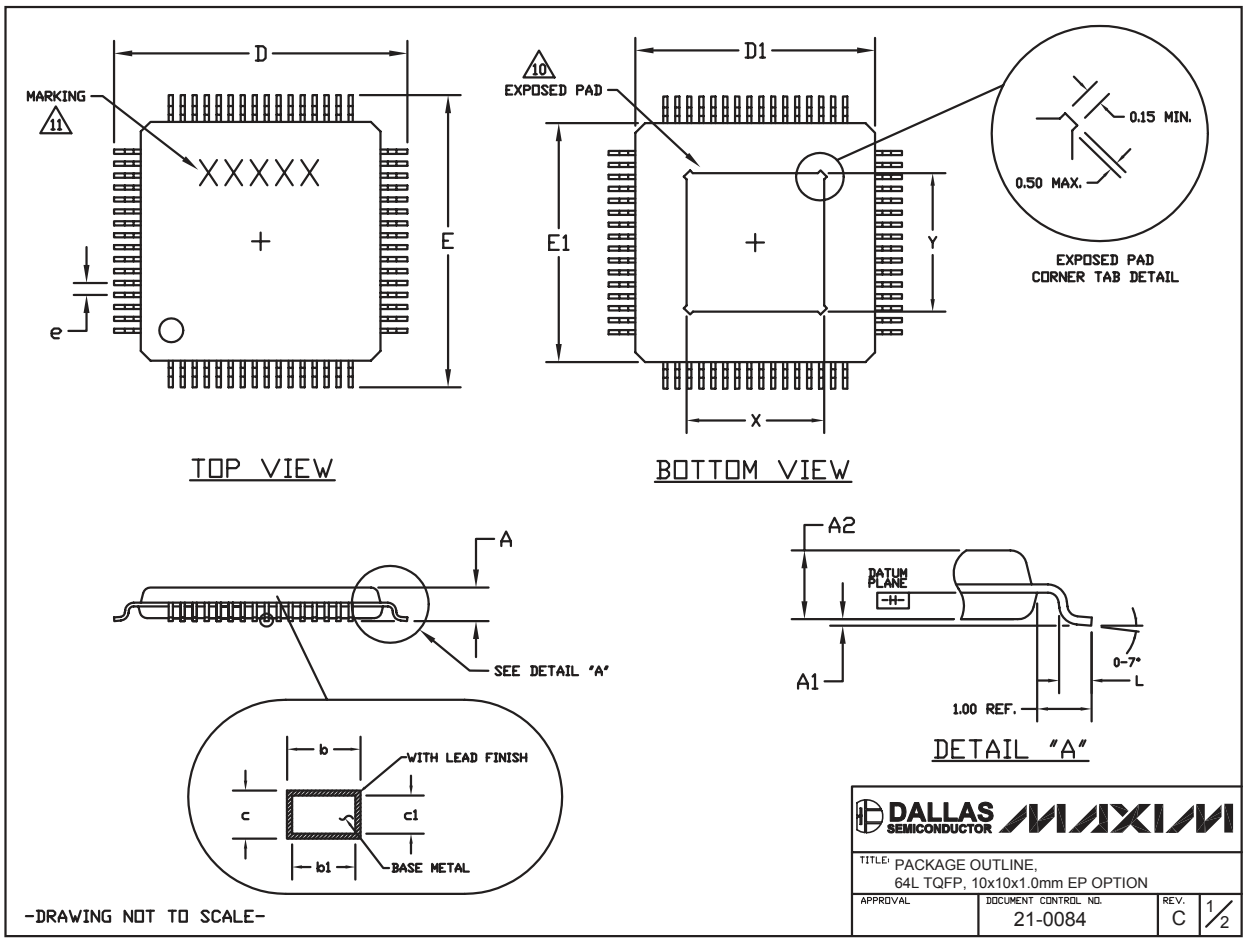
TQFP-EP

+3.3V, 2.488Gbps, SDH/SONET 1:16 Deserializer with Clock Recovery

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

64L, TQFP.EPS



+3.3V, 2.488Gbps, SDH/SONET 1:16 Deserializer with Clock Recovery

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

NOTES:
1. ALL DIMENSIONS AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE -H- IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. CONTROLLING DIMENSION: MILLIMETER.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-026, VARIATION ACD.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.
9. EXPOSED DIE PAD SHALL BE COPLANAR WITH BOTTOM OF PACKAGE WITHIN 2 MILS (.05 MM).
10. DIMENSIONS X & Y APPLY TO EXPOSED PAD (EP) VERSIONS ONLY. SEE INDIVIDUAL PRODUCT DATASHEET TO DETERMINE IF A PRODUCT USES EXPOSED PAD PACKAGE.
11. MARKING SHOWN IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

SYMBOL	JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS	
	ACD-HD	
	MIN.	MAX.
A		1.20
A_1	0.05	0.15
A_2	0.95	1.05
D	11.80	12.20
D_1	9.80	10.20
E	11.80	12.20
E_1	9.80	10.20
L	0.45	0.75
N	64	
e	0.50 BSC.	
b	0.17	0.27
b1	0.17	0.23
c	0.09	0.20
c1	0.09	0.16
X	4.70	5.30
Y	4.70	5.30

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 64L TQFP, 10x10x1.0mm EP OPTION

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0084	C	2/2