

## SN74AXC2T45-Q1 2-Bit Translating Transceiver with Configurable Level-Shifting

### 1 Features

- AEC-Q100 automotive qualified
- Fully configurable dual-rail design allows each port to operate with a power supply range from 0.65 V to 3.6 V
- Operating temperature from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Glitch-free power supply sequencing
- Up to 380 Mbps support when translating from 1.8 V to 3.3 V
- $V_{CC}$  isolation feature
  - If either  $V_{CC}$  input is below 100 mV, all I/Os outputs are disabled and become high-impedance
- $I_{off}$  supports partial-power-down mode operation
- Compatible with AVC family level shifters
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD protection exceeds JESD 22
  - 8000-V human-body model
  - 1000-V charged-device model

### 2 Applications

- [Enterprise and communications](#)
- [Industrial](#)
- [Personal electronics](#)
- [Wireless infrastructure](#)
- [Building automation](#)
- [Point-of-sale](#)

### 3 Description

The SN74AXC2T45-Q1 is a two-bit noninverting bus transceiver that uses two individually configurable power-supply rails. The device is operational with both  $V_{CCA}$  and  $V_{CCB}$  supplies as low as 0.65 V. The A port is designed to track  $V_{CCA}$ , which accepts any supply voltage from 0.65 V to 3.6 V. The B port is designed to track  $V_{CCB}$ , which also accepts any supply voltage from 0.65 V to 3.6 V. Additionally the SN74AXC2T45-Q1 is compatible with a single-supply system.

The SN74AXC2T45-Q1 device is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level of the direction-control input (DIR). The SN74AXC2T45-Q1 device is designed so the control pin (DIR) is referenced to  $V_{CCA}$ .

This device is fully specified for partial-power-down applications using the  $I_{off}$  current. The  $I_{off}$  protection circuitry ensures that no excessive current is drawn from or to an input, output, or combined I/O that is biased to a specific voltage while the device is powered down.

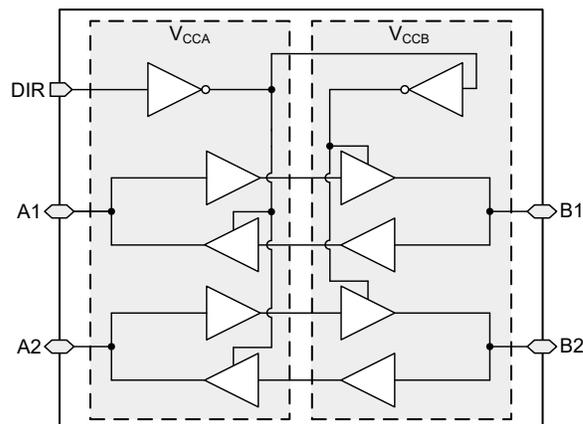
The  $V_{CC}$  isolation feature ensures that if either  $V_{CCA}$  or  $V_{CCB}$  is less than 100 mV, both I/O ports enter a high-impedance state by disabling their outputs.

Glitch-free power supply sequencing allows either supply rail to be powered on or off in any order while providing robust power sequencing performance.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AXC2T45DCU	VSSOP (8)	2.30 mm × 2.00 mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Block Diagram



## Table of Contents

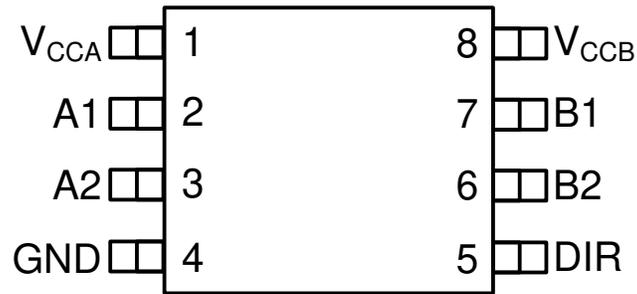
<b>1 Features</b> .....	1	7.1 Load Circuit and Voltage Waveforms.....	17
<b>2 Applications</b> .....	1	<b>8 Detailed Description</b> .....	19
<b>3 Description</b> .....	1	8.1 Overview.....	19
<b>4 Revision History</b> .....	2	8.2 Functional Block Diagram.....	19
<b>5 Pin Configuration and Functions</b> .....	3	8.3 Feature Description.....	19
<b>6 Specifications</b> .....	4	8.4 Device Functional Modes.....	20
6.1 Absolute Maximum Ratings.....	4	<b>9 Application and Implementation</b> .....	21
6.2 ESD Ratings.....	4	9.1 Application Information.....	21
6.3 Recommended Operating Conditions.....	5	9.2 Typical Application.....	21
6.4 Thermal Information.....	5	<b>10 Power Supply Recommendations</b> .....	23
6.5 Electrical Characteristics.....	6	<b>11 Layout</b> .....	23
6.6 Switching Characteristics, $V_{CCA} = 0.7 \pm 0.05$ V.....	7	11.1 Layout Guidelines.....	23
6.7 Switching Characteristics, $V_{CCA} = 0.8 \pm 0.04$ V.....	8	11.2 Layout Example.....	23
6.8 Switching Characteristics, $V_{CCA} = 0.9 \pm 0.045$ V.....	9	<b>12 Device and Documentation Support</b> .....	24
6.9 Switching Characteristics, $V_{CCA} = 1.2 \pm 0.1$ V.....	10	12.1 Documentation Support.....	24
6.10 Switching Characteristics, $V_{CCA} = 1.5 \pm 0.1$ V.....	11	12.2 Receiving Notification of Documentation Updates.....	24
6.11 Switching Characteristics, $V_{CCA} = 1.8 \pm 0.15$ V.....	12	12.3 Support Resources.....	24
6.12 Switching Characteristics, $V_{CCA} = 2.5 \pm 0.2$ V.....	13	12.4 Trademarks.....	24
6.13 Switching Characteristics, $V_{CCA} = 3.3 \pm 0.3$ V.....	14	12.5 Electrostatic Discharge Caution.....	24
6.14 Operating Characteristics: $T_A = 25^\circ\text{C}$ .....	15	12.6 Glossary.....	24
6.15 Typical Characteristics.....	16	<b>13 Mechanical, Packaging, and Orderable Information</b> .....	24
<b>7 Parameter Measurement Information</b> .....	17		

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (April 2021) to Revision A (September 2021)	Page
• Changed the status of the data sheet from: <i>Advance Information</i> to: <i>Production Data</i> .....	1

## 5 Pin Configuration and Functions



**Figure 5-1. DCU Package 8-Pin VSSOP Top View**

**Table 5-1. Pin Functions**

PIN	NO.	DESCRIPTION
NAME	DTM, DCU, DCT	
A1	2	Input/output A1. Referenced to $V_{CCA}$ .
A2	3	Input/output A2. Referenced to $V_{CCA}$ .
B1	7	Input/output B1. Referenced to $V_{CCB}$ .
B2	6	Input/output B2. Referenced to $V_{CCB}$ .
DIR	5	Direction-control in for both ports. Referenced to $V_{CCA}$
GND	4	Ground
$V_{CCA}$	1	A-port power supply voltage. $0.65\text{ V} \leq V_{CCA} \leq 3.6\text{ V}$
$V_{CCB}$	8	B-port power supply voltage. $0.65\text{ V} \leq V_{CCB} \leq 3.6\text{ V}$

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNITS
V <sub>CCA</sub>	Supply voltage A		-0.5	4.2	V
V <sub>CCB</sub>	Supply voltage B		-0.5	4.2	V
V <sub>I</sub>	Input Voltage <sup>(2)</sup>	I/O Ports (A Port)	-0.5	4.2	V
		I/O Ports (B Port)	-0.5	4.2	
		Control Inputs	-0.5	4.2	
V <sub>O</sub>	Voltage applied to any output in the high-impedance or power-off state <sup>(2)</sup>	A Port	-0.5	4.2	V
		B Port	-0.5	4.2	
V <sub>O</sub>	Voltage applied to any output in the high or low state <sup>(2) (3)</sup>	A Port	-0.5 V <sub>CCA</sub> + 0.2		V
		B Port	-0.5 V <sub>CCB</sub> + 0.2		
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0	-50		mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0	-50		mA
I <sub>O</sub>	Continuous output current		-50	50	mA
	Continuous current through V <sub>CC</sub> or GND		-100	100	
T <sub>J</sub>	Junction Temperature			150	°C
T <sub>stg</sub>	Storage temperature		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The output positive-voltage rating may be exceeded up to 4.2 V maximum if the output current rating is observed.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±8000	V
		Charged device model (CDM), per AEC Q100-011	±1000	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

			MIN	MAX	UNIT
V <sub>CCA</sub>	Supply voltage A		0.65	3.6	V
V <sub>CCB</sub>	Supply voltage B		0.65	3.6	V
V <sub>IH</sub>	High-level input voltage	Data Inputs	V <sub>CCI</sub> = 0.65 V – 0.75 V	V <sub>CCI</sub> × 0.70	V
			V <sub>CCI</sub> = 0.76 V – 1 V	V <sub>CCI</sub> × 0.70	
			V <sub>CCI</sub> = 1.1 V – 1.95 V	V <sub>CCI</sub> × 0.65	
			V <sub>CCI</sub> = 2.3 V – 2.7 V	1.6	
			V <sub>CCI</sub> = 3 V – 3.6 V	2	
	Control Input (DIR), Referenced to V <sub>CCA</sub>	V <sub>CCA</sub> = 0.65 V – 0.75 V	V <sub>CCA</sub> × 0.70		
		V <sub>CCA</sub> = 0.76 V – 1 V	V <sub>CCA</sub> × 0.70		
		V <sub>CCA</sub> = 1.1 V – 1.95 V	V <sub>CCA</sub> × 0.65		
		V <sub>CCA</sub> = 2.3 V – 2.7 V	1.6		
		V <sub>CCA</sub> = 3 V – 3.6 V	2		
V <sub>IL</sub>	Low-level input voltage	Data Inputs	V <sub>CCI</sub> = 0.65 V – 0.75 V	V <sub>CCI</sub> × 0.30	
			V <sub>CCI</sub> = 0.76 V – 1 V	V <sub>CCI</sub> × 0.30	
			V <sub>CCI</sub> = 1.1 V – 1.95 V	V <sub>CCI</sub> × 0.35	
			V <sub>CCI</sub> = 2.3 V – 2.7 V	0.7	
			V <sub>CCI</sub> = 3 V – 3.6 V	0.8	
	Control Input (DIR), Referenced to V <sub>CCA</sub>	V <sub>CCA</sub> = 0.65 V – 0.75 V	V <sub>CCA</sub> × 0.30		
		V <sub>CCA</sub> = 0.76 V – 1 V	V <sub>CCA</sub> × 0.30		
		V <sub>CCA</sub> = 1.1 V – 1.95 V	V <sub>CCA</sub> × 0.35		
		V <sub>CCA</sub> = 2.3 V – 2.7 V	0.7		
		V <sub>CCA</sub> = 3 V – 3.6 V	0.8		
V <sub>I</sub>	Input voltage		0	3.6	V
V <sub>O</sub>	Output voltage	Active State	0	V <sub>CCO</sub>	V
		Tri-State	0	3.6	
Δt/Δv <sup>(2)</sup>	Input transition rise and fall time			10	ns/V
Δt/Δv <sup>(3)</sup>	Single channel input transition rise and fall time			100	ns/V
T <sub>A</sub>	Operating free-air temperature		–40	125	°C

(1) V<sub>CCI</sub> is the V<sub>CC</sub> associated with the input port. V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.

(2) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, [Implications of Slow or Floating CMOS Inputs](#), SCBA004.

(3) Input transition rate of a single channel while the other channels are at a valid logic state and not switching.

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74AXC2T45-Q1			UNIT
		DCT (SM8)	DCU (VSSOP)	DTM (X2SON)	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	223.5	242.9	225.9	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	120.7	96.2	131.6	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	138.0	153.3	141.3	°C/W
Y <sub>JT</sub>	Junction-to-top characterization parameter	47.5	38.2	12.7	°C/W
Y <sub>JB</sub>	Junction-to-board characterization parameter	136.7	152.5	140.9	°C/W

(1) For more information about thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted) (1) (2) (3)

PARAMETER	TEST CONDITIONS	$V_{CCA}$	$V_{CCB}$	Operating free-air temperature ( $T_A$ )						UNIT		
				-40°C to 85°C			-40°C to 125°C					
				MIN	TYP	MAX	MIN	TYP	MAX			
$V_{OH}$	High-level output voltage	$V_I = V_{IH}$	$I_{OH} = -100 \mu A$	0.7 V – 3.6 V	0.7 V – 3.6 V	$V_{CCO} - 0.1$			$V_{CCO} - 0.1$			V
			$I_{OH} = -50 \mu A$	0.65 V	0.65 V	0.55			0.55			
			$I_{OH} = -200 \mu A$	0.76 V	0.76 V	0.58			0.58			
			$I_{OH} = -500 \mu A$	0.85 V	0.85 V	0.65			0.65			
			$I_{OH} = -3 \text{ mA}$	1.1 V	1.1 V	0.85			0.85			
			$I_{OH} = -6 \text{ mA}$	1.4 V	1.4 V	1.05			1.05			
			$I_{OH} = -8 \text{ mA}$	1.65 V	1.65 V	1.2			1.2			
			$I_{OH} = -9 \text{ mA}$	2.3 V	2.3 V	1.75			1.75			
$V_{OL}$	Low-level output voltage	$V_I = V_{IL}$	$I_{OL} = 100 \mu A$	0.7 V – 3.6 V	0.7 V – 3.6 V				0.1			V
			$I_{OL} = 50 \mu A$	0.65 V	0.65 V				0.1			
			$I_{OL} = 200 \mu A$	0.76 V	0.76 V				0.18			
			$I_{OL} = 500 \mu A$	0.85 V	0.85 V				0.2			
			$I_{OL} = 3 \text{ mA}$	1.1 V	1.1 V				0.25			
			$I_{OL} = 6 \text{ mA}$	1.4 V	1.4 V				0.35			
			$I_{OL} = 8 \text{ mA}$	1.65 V	1.65 V				0.45			
			$I_{OL} = 9 \text{ mA}$	2.3 V	2.3 V				0.55			
$I_I$	Input leakage current	Control input (DIR): $V_I = V_{CCA}$ or GND		0.65 V – 3.6 V	0.65 V – 3.6 V	-0.5			0.5			$\mu A$
		Data Inputs (Ax, Bx), $V_I = V_{CCI}$ or GND		0.65 V – 3.6 V	0.65 V – 3.6 V	-4			4			
$I_{off}$	Partial power down current	A Port: $V_I$ or $V_O = 0 \text{ V} - 3.6 \text{ V}$		0 V	0 V – 3.6 V	-4			4			$\mu A$
		B Port: $V_I$ or $V_O = 0 \text{ V} - 3.6 \text{ V}$		0 V – 3.6 V	0 V	-4			4			
$I_{CCA}$	$V_{CCA}$ supply current	$V_I = V_{CCI}$ or GND	$I_O = 0$	0.65 V – 3.6 V	0.65 V – 3.6 V				8			$\mu A$
				0 V	3.6 V	-2			-12			
				3.6 V	0 V				4			
$I_{CCB}$	$V_{CCB}$ supply current	$V_I = V_{CCI}$ or GND	$I_O = 0$	0.65 V – 3.6 V	0.65 V – 3.6 V				8			$\mu A$
				0 V	3.6 V	4			8			
				3.6 V	0 V	-2			-12			
$I_{CCA} + I_{CCB}$	Combined supply current	$V_I = V_{CCI}$ or GND	$I_O = 0$	0.65 V – 3.6 V	0.65 V – 3.6 V				16			$\mu A$
$C_i$	Control Input (DIR) Capacitance	$V_I = 3.3 \text{ V}$ or GND		3.3 V	3.3 V	3.3			3.3			pF
$C_{io}$	Data I/O Capacitance	$V_O = 1.65 \text{ V DC} + 1 \text{ MHz}$ -16 dBm sine wave		3.3 V	3.3 V	5.4			5.4			pF

- (1)  $V_{CCI}$  is the  $V_{CC}$  associated with the input port.  
(2)  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.  
(3) All typical data is taken at 25°C.

## 6.6 Switching Characteristics, $V_{CCA} = 0.7 \pm 0.05 \text{ V}$

See [Figure 5](#) and [Table 1](#) for test circuit and loading. See [Figure 6](#), [Figure 7](#), and [Figure 8](#) for measurement waveforms.

PARAMETER	FROM	TO	Test Conditions	B-Port Supply Voltage ( $V_{CCB}$ )														UNIT			
				0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V			3.3 ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		MIN	MAX	
$t_{pd}$	Propagation delay	A	B	-40°C to 85°C	0.5	170	0.5	115	0.5	84	0.5	50	0.5	50	0.5	56	0.5	71	0.5	106	ns
				-40°C to 125°C	0.5	170	0.5	115	0.5	84	0.5	50	0.5	50	0.5	56	0.5	71	0.5	106	
	B	A	-40°C to 85°C	0.5	170	0.5	149	0.5	122	0.5	83	0.5	79	0.5	78	0.5	77	0.5	76		
			-40°C to 125°C	0.5	170	0.5	149	0.5	122	0.5	83	0.5	79	0.5	78	0.5	77	0.5	76		
$t_{dis}$	Disable time	DIR	A	-40°C to 85°C	0.5	140	0.5	140	0.5	140	0.5	140	0.5	140	0.5	140	0.5	140	0.5	140	ns
				-40°C to 125°C	0.5	140	0.5	140	0.5	140	0.5	140	0.5	140	0.5	140	0.5	140	0.5	140	
	DIR	B	-40°C to 85°C	0.5	143	0.5	105	0.5	84	0.5	41	0.5	39	0.5	42	0.5	56	0.5	107		
			-40°C to 125°C	0.5	143	0.5	105	0.5	84	0.5	41	0.5	39	0.5	42	0.5	56	0.5	107		
$t_{en}$	Enable time	DIR	A	-40°C to 85°C	0.5	311	0.5	311	0.5	311	0.5	311	0.5	311	0.5	311	0.5	311	0.5	311	ns
				-40°C to 125°C	0.5	311	0.5	311	0.5	311	0.5	311	0.5	311	0.5	311	0.5	311	0.5	311	
	DIR	B	-40°C to 85°C	0.5	306	0.5	247	0.5	216	0.5	186	0.5	182	0.5	183	0.5	194	0.5	228		
			-40°C to 125°C	0.5	306	0.5	247	0.5	216	0.5	186	0.5	182	0.5	183	0.5	194	0.5	228		

## 6.7 Switching Characteristics, $V_{CCA} = 0.8 \pm 0.04 \text{ V}$

See Figure 5 and Table 1 for test circuit and loading. See Figure 6, Figure 7, and Figure 8 for measurement waveforms.

PARAMETER	FROM	TO	Test Conditions	B-Port Supply Voltage ( $V_{CCB}$ )														UNIT			
				0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V			3.3 ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		MIN	MAX	
$t_{pd}$	Propagation delay	A	B	-40°C to 85°C	0.5	150	0.5	94	0.5	63	0.5	33	0.5	28	0.5	27	0.5	28	0.5	34	ns
				-40°C to 125°C	0.5	150	0.5	94	0.5	63	0.5	33	0.5	28	0.5	27	0.5	28	0.5	34	
	B	A	-40°C to 85°C	0.5	115	0.5	94	0.5	76	0.5	50	0.5	41	0.5	40	0.5	38	0.5	38		
			-40°C to 125°C	0.5	115	0.5	94	0.5	76	0.5	50	0.5	41	0.5	40	0.5	38	0.5	38		
$t_{dis}$	Disable time	DIR	A	-40°C to 85°C	0.5	96	0.5	96	0.5	96	0.5	96	0.5	96	0.5	96	0.5	96	0.5	96	ns
				-40°C to 125°C	0.5	96	0.5	96	0.5	96	0.5	96	0.5	96	0.5	96	0.5	96	0.5	96	
	DIR	B	-40°C to 85°C	0.5	136	0.5	97	0.5	76	0.5	33	0.5	27	0.5	26	0.5	28	0.5	35		
			-40°C to 125°C	0.5	136	0.5	97	0.5	76	0.5	33	0.5	27	0.5	26	0.5	28	0.5	35		
$t_{en}^{(1)}$	Enable time	DIR	A	-40°C to 85°C	0.5	246	0.5	246	0.5	246	0.5	246	0.5	246	0.5	246	0.5	246	0.5	246	ns
				-40°C to 125°C	0.5	246	0.5	246	0.5	246	0.5	246	0.5	246	0.5	246	0.5	246	0.5	246	
	DIR	B	-40°C to 85°C	0.5	243	0.5	188	0.5	157	0.5	128	0.5	123	0.5	122	0.5	123	0.5	125		
			-40°C to 125°C	0.5	243	0.5	188	0.5	157	0.5	128	0.5	123	0.5	122	0.5	123	0.5	125		

(1) The enable time is a calculated value, derived using the formula shown in the Enable Times section.

## 6.8 Switching Characteristics, $V_{CCA} = 0.9 \pm 0.045 \text{ V}$

See [Figure 5](#) and [Table 1](#) for test circuit and loading. See [Figure 6](#), [Figure 7](#), and [Figure 8](#) for measurement waveforms.

PARAMETER	FROM	TO	Test Conditions	B-Port Supply Voltage ( $V_{CCB}$ )												UNIT					
				0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V			2.5 ± 0.2 V		3.3 ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX	
$t_{pd}$	Propagation delay	A	B	-40°C to 85°C	0.5	122	0.5	76	0.5	51	0.5	23	0.5	18	0.5	16	0.5	15	0.5	17	ns
				-40°C to 125°C	0.5	122	0.5	76	0.5	51	0.5	23	0.5	18	0.5	16	0.5	15	0.5	17	
	B	A	-40°C to 85°C	0.5	84	0.5	63	0.5	51	0.5	39	0.5	28	0.5	24	0.5	21	0.5	21		
			-40°C to 125°C	0.5	84	0.5	63	0.5	51	0.5	39	0.5	28	0.5	24	0.5	21	0.5	21		
$t_{dis}$	Disable time	DIR	A	-40°C to 85°C	0.5	74	0.5	74	0.5	74	0.5	74	0.5	74	0.5	74	0.5	74	0.5	74	ns
				-40°C to 125°C	0.5	74	0.5	74	0.5	74	0.5	74	0.5	74	0.5	74	0.5	74	0.5	74	
	DIR	B	-40°C to 85°C	0.5	133	0.5	94	0.5	73	0.5	30	0.5	23	0.5	22	0.5	20	0.5	22		
			-40°C to 125°C	0.5	133	0.5	94	0.5	73	0.5	31	0.5	24	0.5	22	0.5	20	0.5	20		
$t_{en}^{(1)}$	Enable time	DIR	A	-40°C to 85°C	0.5	211	0.5	211	0.5	211	0.5	211	0.5	211	0.5	211	0.5	211	0.5	211	ns
				-40°C to 125°C	0.5	211	0.5	211	0.5	211	0.5	211	0.5	211	0.5	211	0.5	211	0.5	211	
		DIR	B	-40°C to 85°C	0.5	192	0.5	146	0.5	120	0.5	93	0.5	88	0.5	86	0.5	85	0.5	87	
				-40°C to 125°C	0.5	192	0.5	146	0.5	120	0.5	93	0.5	88	0.5	86	0.5	85	0.5	87	

(1) The enable time is a calculated value, derived using the formula shown in the Enable Times section.

## 6.9 Switching Characteristics, $V_{CCA} = 1.2 \pm 0.1$ V

See Figure 5 and Table 1 for test circuit and loading. See Figure 6, Figure 7, and Figure 8 for measurement waveforms.

PARAMETER	FROM	TO	Test Conditions	B-Port Supply Voltage ( $V_{CCB}$ )														UNIT			
				0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V			3.3 ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		MIN	MAX	
$t_{pd}$	Propagation delay	A	B	-40°C to 85°C	0.5	84	0.5	51	0.5	38	0.5	15	0.5	10	0.5	9	0.5	7	0.5	8	ns
				-40°C to 125°C	0.5	84	0.5	51	0.5	38	0.5	15	0.5	11	0.5	9	0.5	8	0.5	8	
	B	A	-40°C to 85°C	0.5	50	0.5	33	0.5	23	0.5	15	0.5	12	0.5	10	0.5	8	0.5	7		
			-40°C to 125°C	0.5	50	0.5	33	0.5	23	0.5	15	0.5	12	0.5	10	0.5	8	0.5	7		
$t_{dis}$	Disable time	DIR	A	-40°C to 85°C	0.5	26	0.5	26	0.5	26	0.5	26	0.5	26	0.5	26	0.5	26	0.5	26	ns
				-40°C to 125°C	0.5	27	0.5	27	0.5	27	0.5	27	0.5	27	0.5	27	0.5	27	0.5	27	
	DIR	B	-40°C to 85°C	0.5	129	0.5	90	0.5	70	0.5	27	0.5	20	0.5	18	0.5	15	0.5	15		
			-40°C to 125°C	0.5	129	0.5	90	0.5	71	0.5	28	0.5	21	0.5	19	0.5	16	0.5	16		
$t_{en}^{(1)}$	Enable time	DIR	A	-40°C to 85°C	0.5	177	0.5	177	0.5	177	0.5	177	0.5	177	0.5	177	0.5	177	0.5	177	ns
				-40°C to 125°C	0.5	177	0.5	177	0.5	177	0.5	177	0.5	177	0.5	177	0.5	177	0.5	177	
	DIR	B	-40°C to 85°C	0.5	105	0.5	71	0.5	59	0.5	40	0.5	36	0.5	35	0.5	33	0.5	34		
			-40°C to 125°C	0.5	105	0.5	71	0.5	59	0.5	41	0.5	37	0.5	36	0.5	34	0.5	35		

(1) The enable time is a calculated value, derived using the formula shown in the Enable Times section.

## 6.10 Switching Characteristics, $V_{CCA} = 1.5 \pm 0.1 \text{ V}$

See Figure 5 and Table 1 for test circuit and loading. See Figure 6, Figure 7, and Figure 8 for measurement waveforms.

PARAMETER	FROM	TO	Test Conditions	B-Port Supply Voltage ( $V_{CCB}$ )												UNIT					
				0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V			2.5 ± 0.2 V		3.3 ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX	
$t_{pd}$	Propagation delay	A	B	-40°C to 85°C	0.5	79	0.5	41	0.5	28	0.5	12	0.5	9	0.5	7	0.5	6	0.5	6	ns
				-40°C to 125°C	0.5	79	0.5	41	0.5	28	0.5	12	0.5	9	0.5	8	0.5	6	0.5	6	
	B	A	-40°C to 85°C	0.5	50	0.5	28	0.5	18	0.5	10	0.5	9	0.5	8	0.5	6	0.5	5		
			-40°C to 125°C	0.5	50	0.5	28	0.5	18	0.5	11	0.5	9	0.5	8	0.5	6	0.5	5		
$t_{dis}$	Disable time	DIR	A	-40°C to 85°C	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	ns
				-40°C to 125°C	0.5	19	0.5	19	0.5	19	0.5	19	0.5	19	0.5	19	0.5	19	0.5	19	
	DIR	B	-40°C to 85°C	0.5	128	0.5	89	0.5	69	0.5	26	0.5	19	0.5	17	0.5	13	0.5	13		
			-40°C to 125°C	0.5	128	0.5	89	0.5	70	0.5	27	0.5	20	0.5	18	0.5	14	0.5	14		
$t_{en}^{(1)}$	Enable time	DIR	A	-40°C to 85°C	0.5	172	0.5	172	0.5	172	0.5	172	0.5	172	0.5	172	0.5	172	0.5	172	ns
				-40°C to 125°C	0.5	172	0.5	172	0.5	172	0.5	172	0.5	172	0.5	172	0.5	172	0.5	172	
	DIR	B	-40°C to 85°C	0.5	92	0.5	54	0.5	42	0.5	31	0.5	27	0.5	25	0.5	24	0.5	24		
			-40°C to 125°C	0.5	92	0.5	54	0.5	42	0.5	31	0.5	28	0.5	26	0.5	25	0.5	25		

(1) The enable time is a calculated value, derived using the formula shown in the Enable Times section.

## 6.11 Switching Characteristics, $V_{CCA} = 1.8 \pm 0.15 \text{ V}$

See [Figure 5](#) and [Table 1](#) for test circuit and loading. See [Figure 6](#), [Figure 7](#), and [Figure 8](#) for measurement waveforms.

PARAMETER	FROM	TO	Test Conditions	B-Port Supply Voltage ( $V_{CCB}$ )												UNIT					
				0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V			2.5 ± 0.2 V		3.3 ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX	
$t_{pd}$	Propagation delay	A	B	-40°C to 85°C	0.5	78	0.5	40	0.5	24	0.5	10	0.5	8	0.5	7	0.5	5	0.5	5	ns
				-40°C to 125°C	0.5	78	0.5	40	0.5	24	0.5	10	0.5	8	0.5	7	0.5	6	0.5	5	
	B	A	-40°C to 85°C	0.5	56	0.5	27	0.5	16	0.5	9	0.5	7	0.5	7	0.5	5	0.5	4		
			-40°C to 125°C	0.5	56	0.5	27	0.5	16	0.5	9	0.5	8	0.5	7	0.5	5	0.5	5		
$t_{dis}$	Disable time	DIR	A	-40°C to 85°C	0.5	16	0.5	16	0.5	16	0.5	16	0.5	16	0.5	16	0.5	16	0.5	16	ns
				-40°C to 125°C	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	
	DIR	B	-40°C to 85°C	0.5	127	0.5	88	0.5	69	0.5	25	0.5	18	0.5	16	0.5	12	0.5	12		
			-40°C to 125°C	0.5	127	0.5	88	0.5	70	0.5	26	0.5	19	0.5	17	0.5	13	0.5	13		
$t_{en}^{(1)}$	Enable time	DIR	A	-40°C to 85°C	0.5	171	0.5	171	0.5	171	0.5	171	0.5	171	0.5	171	0.5	171	0.5	171	ns
				-40°C to 125°C	0.5	171	0.5	171	0.5	171	0.5	171	0.5	171	0.5	171	0.5	171	0.5	171	
	DIR	B	-40°C to 85°C	0.5	89	0.5	50	0.5	36	0.5	26	0.5	23	0.5	22	0.5	21	0.5	20		
			-40°C to 125°C	0.5	89	0.5	50	0.5	36	0.5	27	0.5	24	0.5	23	0.5	22	0.5	21		

(1) The enable time is a calculated value, derived using the formula shown in the Enable Times section.

## 6.12 Switching Characteristics, $V_{CCA} = 2.5 \pm 0.2 \text{ V}$

See Figure 5 and Table 1 for test circuit and loading. See Figure 6, Figure 7, and Figure 8 for measurement waveforms.

PARAMETER	FROM	TO	Test Conditions	B-Port Supply Voltage ( $V_{CCB}$ )														UNIT			
				0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V			3.3 ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		MIN	MAX	
$t_{pd}$	Propagation delay	A	B	-40°C to 85°C	0.5	77	0.5	38	0.5	21	0.5	8	0.5	6	0.5	5	0.5	5	0.5	4	ns
				-40°C to 125°C	0.5	77	0.5	38	0.5	21	0.5	8	0.5	6	0.5	5	0.5	5	0.5	5	
	B	A	-40°C to 85°C	0.5	71	0.5	28	0.5	15	0.5	7	0.5	6	0.5	5	0.5	5	0.5	4		
			-40°C to 125°C	0.5	71	0.5	28	0.5	15	0.5	8	0.5	6	0.5	6	0.5	5	0.5	4		
$t_{dis}$	Disable time	DIR	A	-40°C to 85°C	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	ns
				-40°C to 125°C	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	
	DIR	B	-40°C to 85°C	0.5	127	0.5	88	0.5	68	0.5	25	0.5	18	0.5	15	0.5	12	0.5	11		
			-40°C to 125°C	0.5	127	0.5	88	0.5	69	0.5	26	0.5	19	0.5	16	0.5	12	0.5	12		
$t_{en}^{(1)}$	Enable time	DIR	A	-40°C to 85°C	0.5	182	0.5	182	0.5	182	0.5	182	0.5	182	0.5	182	0.5	182	0.5	182	ns
				-40°C to 125°C	0.5	182	0.5	182	0.5	182	0.5	182	0.5	182	0.5	182	0.5	182	0.5	182	
		DIR	B	-40°C to 85°C	0.5	84	0.5	46	0.5	29	0.5	18	0.5	17	0.5	16	0.5	15	0.5	15	
				-40°C to 125°C	0.5	84	0.5	46	0.5	29	0.5	19	0.5	18	0.5	17	0.5	16	0.5	16	

(1) The enable time is a calculated value, derived using the formula shown in the Enable Times section.

### 6.13 Switching Characteristics, $V_{CCA} = 3.3 \pm 0.3 \text{ V}$

See Figure 5 and Table 1 for test circuit and loading. See Figure 6, Figure 7, and Figure 8 for measurement waveforms.

PARAMETER	FROM	TO	Test Conditions	B-Port Supply Voltage ( $V_{CCB}$ )														UNIT			
				0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V			3.3 ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		MIN	MAX	
$t_{pd}$	Propagation delay	A	B	-40°C to 85°C	0.5	76	0.5	38	0.5	21	0.5	7	0.5	5	0.5	4	0.5	4	0.5	4	ns
				-40°C to 125°C	0.5	76	0.5	38	0.5	21	0.5	7	0.5	5	0.5	5	0.5	4	0.5	4	
	B	A	-40°C to 85°C	0.5	105	0.5	34	0.5	17	0.5	8	0.5	6	0.5	5	0.5	4	0.5	4		
			-40°C to 125°C	0.5	105	0.5	34	0.5	17	0.5	8	0.5	6	0.5	5	0.5	5	0.5	4		
$t_{dis}$	Disable time	DIR	A	-40°C to 85°C	0.5	10	0.5	10	0.5	10	0.5	10	0.5	10	0.5	10	0.5	10	0.5	10	ns
				-40°C to 125°C	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	
	DIR	B	-40°C to 85°C	0.5	128	0.5	88	0.5	68	0.5	24	0.5	17	0.5	15	0.5	11	0.5	11		
			-40°C to 125°C	0.5	128	0.5	88	0.5	69	0.5	26	0.5	19	0.5	16	0.5	12	0.5	11		
$t_{en}^{(1)}$	Enable time	DIR	A	-40°C to 85°C	0.5	218	0.5	218	0.5	218	0.5	218	0.5	218	0.5	218	0.5	218	0.5	218	ns
				-40°C to 125°C	0.5	218	0.5	218	0.5	218	0.5	218	0.5	218	0.5	218	0.5	218	0.5	218	
	DIR	B	-40°C to 85°C	0.5	83	0.5	45	0.5	28	0.5	17	0.5	15	0.5	14	0.5	14	0.5	14		
			-40°C to 125°C	0.5	83	0.5	45	0.5	28	0.5	18	0.5	16	0.5	15	0.5	15	0.5	15		

(1) The enable time is a calculated value, derived using the formula shown in the Enable Times section.

### 6.14 Operating Characteristics: T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS	V <sub>CCA</sub>	V <sub>CCB</sub>	MIN	TYP	MAX	UNIT
C <sub>pdA</sub>	Power Dissipation Capacitance per transceiver (A to B)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		2.2		pF
			0.8 V	0.8 V		2.0		
			0.9 V	0.9 V		2.0		
			1.2 V	1.2 V		2.0		
			1.5 V	1.5 V		2.0		
			1.8 V	1.8 V		2.1		
			2.5 V	2.5 V		2.5		
			3.3 V	3.3 V		3.0		
	Power Dissipation Capacitance per transceiver (B to A)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		10.6		pF
			0.8 V	0.8 V		10.7		
			0.9 V	0.9 V		10.6		
			1.2 V	1.2 V		10.8		
			1.5 V	1.5 V		11.1		
			1.8 V	1.8 V		12.2		
2.5 V			2.5 V		15.9			
3.3 V			3.3 V		19.6			
C <sub>pdB</sub>	Power Dissipation Capacitance per transceiver (A to B)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		10.6		pF
			0.8 V	0.8 V		10.7		
			0.9 V	0.9 V		10.6		
			1.2 V	1.2 V		10.8		
			1.5 V	1.5 V		11.1		
			1.8 V	1.8 V		12.2		
			2.5 V	2.5 V		15.8		
			3.3 V	3.3 V		19.3		
	Power Dissipation Capacitance per transceiver (B to A)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		2.2		pF
			0.8 V	0.8 V		2.0		
			0.9 V	0.9 V		2.0		
			1.2 V	1.2 V		2.0		
			1.5 V	1.5 V		2.0		
			1.8 V	1.8 V		2.1		
2.5 V			2.5 V		2.5			
3.3 V			3.3 V		3.0			

### 6.15 Typical Characteristics

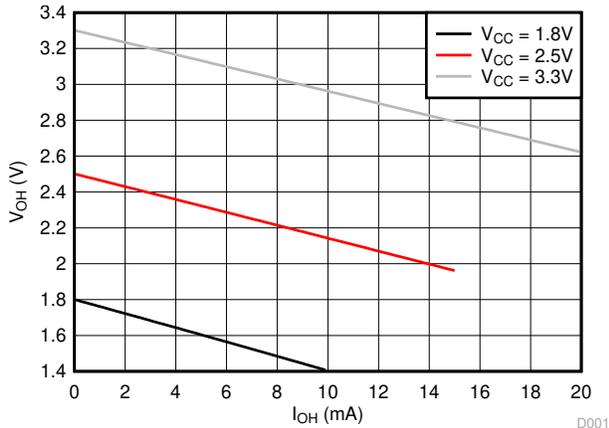


Figure 6-1. Typical ( $T_A=25^\circ\text{C}$ ) Output High Voltage ( $V_{OH}$ ) vs Source Current ( $I_{OH}$ )

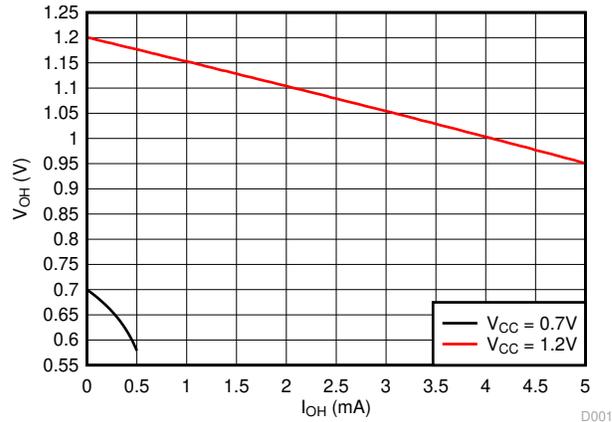


Figure 6-2. Typical ( $T_A=25^\circ\text{C}$ ) Output High Voltage ( $V_{OH}$ ) vs Source Current ( $I_{OH}$ )

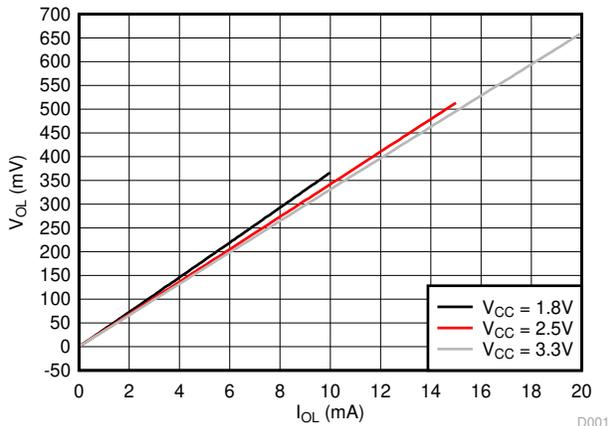


Figure 6-3. Typical ( $T_A=25^\circ\text{C}$ ) Output High Voltage ( $V_{OL}$ ) vs Sink Current ( $I_{OL}$ )

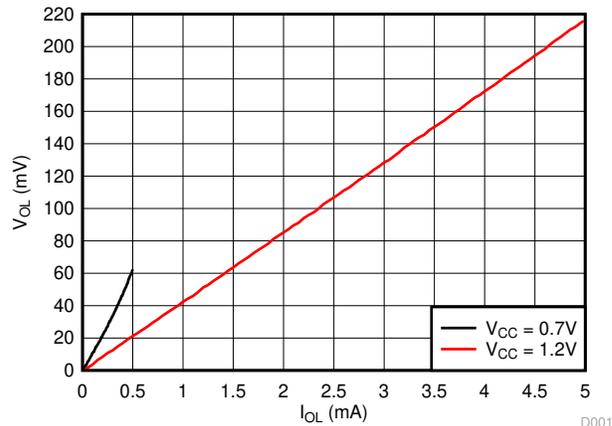


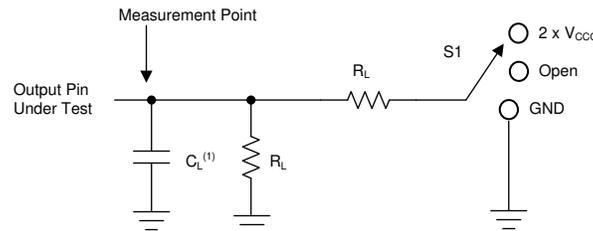
Figure 6-4. Typical ( $T_A=25^\circ\text{C}$ ) Output High Voltage ( $V_{OL}$ ) vs Sink Current ( $I_{OL}$ )

## 7 Parameter Measurement Information

### 7.1 Load Circuit and Voltage Waveforms

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- $f = 1 \text{ MHz}$
- $Z_O = 50 \Omega$
- $dv/dt \leq 1 \text{ ns/V}$

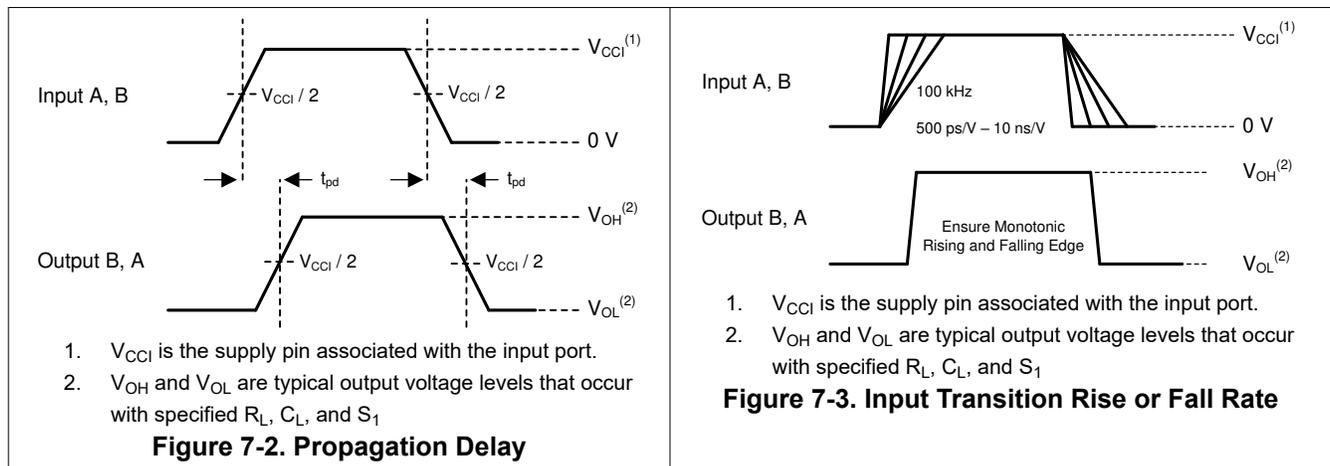


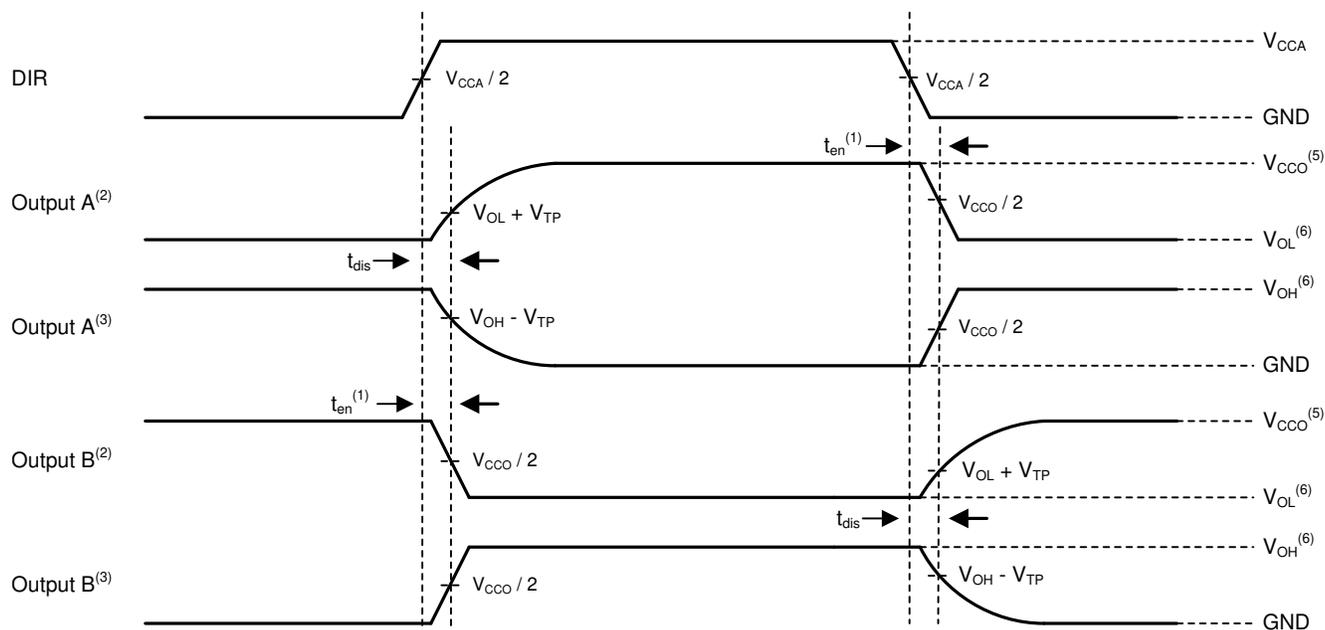
A.  $C_L$  includes probe and jig capacitance.

**Figure 7-1. Load Circuit**

**Table 7-1. Load Circuit Conditions**

Parameter	$V_{CCO}$	$R_L$	$C_L$	$S_1$	$V_{TP}$
$\Delta t/\Delta v$ Input transition rise or fall rate	0.65 V – 3.6 V	1 M $\Omega$	15 pF	Open	N/A
$t_{pd}$ Propagation (delay) time	1.1 V – 3.6 V	2 k $\Omega$	15 pF	Open	N/A
	0.65 V – 0.95 V	20 k $\Omega$	15 pF	Open	N/A
$t_{en}, t_{dis}$ Enable time, disable time	3 V – 3.6 V	2 k $\Omega$	15 pF	$2 \times V_{CCO}$	0.3 V
	1.65 V – 2.7 V	2 k $\Omega$	15 pF	$2 \times V_{CCO}$	0.15 V
	1.1 V – 1.6 V	2 k $\Omega$	15 pF	$2 \times V_{CCO}$	0.1 V
	0.65 V – 0.95 V	20 k $\Omega$	15 pF	$2 \times V_{CCO}$	0.1 V
$t_{en}, t_{dis}$ Enable time, disable time	3 V – 3.6 V	2 k $\Omega$	15 pF	GND	0.3 V
	1.65 V – 2.7 V	2 k $\Omega$	15 pF	GND	0.15 V
	1.1 V – 1.6 V	2 k $\Omega$	15 pF	GND	0.1 V
	0.65 V – 0.95 V	20 k $\Omega$	15 pF	GND	0.1 V





- A. Illustrative purposes only. Enable Time is a calculation as described in the Application Information section.
- B. Output waveform on the condition that input is driven to a valid Logic Low.
- C. Output waveform on the condition that input is driven to a valid Logic High.
- D.  $V_{CCI}$  is the supply pin associated with the input port.
- E.  $V_{CCO}$  is the supply pin associated with the output port.
- F.  $V_{OH}$  and  $V_{OL}$  are typical output voltage levels with specified  $R_L$ ,  $C_L$ , and  $S_1$ .

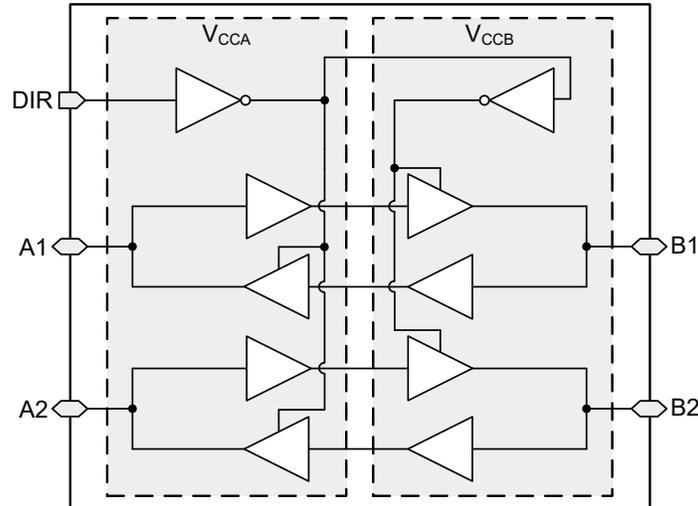
**Figure 7-4. Enable Time And Disable Time**

## 8 Detailed Description

### 8.1 Overview

The SN74AXC2T45-Q1 is a 2-bit, dual-supply non-inverting bidirectional voltage level translation device. Ax pins and the DIR pin are referenced to  $V_{CCA}$  logic levels, and Bx pins are referenced to  $V_{CCB}$  logic levels. The A port is able to accept I/O voltages ranging from 0.65 V to 3.6 V, while the B port can accept I/O voltages from 0.65 V to 3.6 V. A high on DIR enables data transmission from A to B and a low on DIR enables data transmission from B to A. See [Section 8.4](#) for a summary of the operation of the control logic.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in [Section 6.5](#). The worst case resistance is calculated with the maximum input voltage, given in [Section 6.1](#), and the maximum input leakage current, given in the [Section 6.5](#), using Ohm's law ( $R = V \div I$ ).

Signals applied to the inputs need to have fast edge rates, as defined by  $\Delta t/\Delta v$  in [Section 6.3](#) to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

#### 8.3.2 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. The electrical and thermal limits defined in [Section 6.1](#) must be followed at all times.

#### 8.3.3 Partial Power Down ( $I_{off}$ )

The inputs and outputs for this device enter a high-impedance state when the device is powered down, inhibiting current backflow into the device. The maximum leakage into or out of any input or output pin on the device is specified by  $I_{off}$  in [Section 6.5](#).

#### 8.3.4 $V_{CC}$ Isolation

The inputs and outputs for this device enter a high-impedance state when either supply is <100 mV.

#### 8.3.5 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in [Section 6.3](#).

### 8.3.6 Glitch-Free Power Supply Sequencing

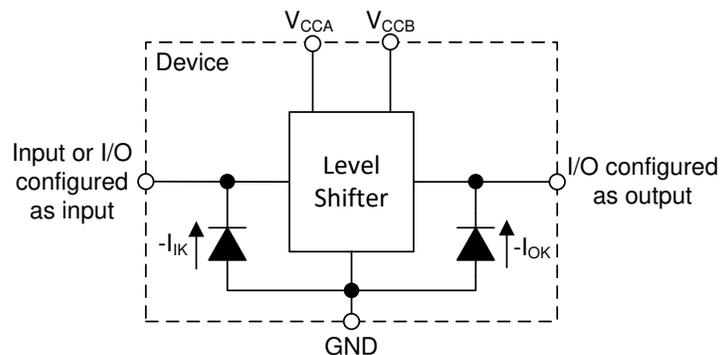
Either supply rail may be powered on or off in any order without producing a glitch on the I/Os (that is, where the output erroneously transitions to  $V_{CC}$  when it should be held low). Glitches of this nature can be misinterpreted by a peripheral as a valid data bit, which could trigger a false device reset of the peripheral, a false device configuration of the peripheral, or even a false data initialization by the peripheral. For more information regarding the power up glitch performance of the AXC family of level translators, see the [Glitch Free Power Sequencing With AXC Level Translators](#) application report.

### 8.3.7 Negative Clamping Diodes

The inputs and outputs to this device have negative clamping diodes as depicted in [Figure 8-1](#).

**CAUTION**

Voltages beyond the values specified in the [Absolute Maximum Ratings](#) table can cause damage to the device. The input negative voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



**Figure 8-1. Electrical Placement of Clamping Diodes for Each Input and Output**

### 8.3.8 Fully Configurable Dual-Rail Design

Both the  $V_{CCA}$  and  $V_{CCB}$  pins can be supplied at any voltage from 0.65 V to 3.6 V, making the device suitable for translating between any of the voltage nodes (0.7 V, 0.8 V, 0.9 V, 1.2 V, 1.8 V, 2.5 V, and 3.3 V).

### 8.3.9 Supports High-Speed Translation

The SN74AXC2T45-Q1 device can support high data-rate applications. The translated signal data rate can be up to 380 Mbps when the signal is translated from 1.8 V to 3.3 V.

## 8.4 Device Functional Modes

**Table 8-1. Function Table<sup>(1)</sup>**

CONTROL INPUT	Port Status		OPERATION
	A PORT	B PORT	
DIR			
L	Output (Enabled)	Input (Hi-Z)	B data to A bus
H	Input (Hi-Z)	Output (Enabled)	A data to B bus

(1) Input circuits of the data I/O's are always active.

## 9 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The SN74AXC2T45-Q1 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The SN74AXC2T45-Q1 device is ideal for use in applications where a push-pull driver is connected to the data I/Os. The maximum data rate can be up to 380 Mbps when device translates a signal from 1.8 V to 3.3 V.

Figure 9-1 shows one example application where the SN74AXC2T45-Q1 device is used to translate low voltage error signals from a CPU to a higher voltage signal to properly drive the inputs of a system controller, thus alerting the system of any CPU errors such as overheating or other catastrophic processor errors.

#### 9.1.1 Enable Times

Calculate the enable times for the SN74AXC2T45-Q1 using the following formulas:

$$t_{A\_en} \text{ (DIR to A)} = t_{dis} \text{ (DIR to B)} + t_{pd} \text{ (B to A)} \quad (1)$$

$$t_{B\_en} \text{ (DIR to A)} = t_{dis} \text{ (DIR to A)} + t_{pd} \text{ (A to B)} \quad (2)$$

In a bidirectional application, these enable times provide the maximum delay time from the time the DIR bit is switched until an output is expected. For example, if the SN74AXC2T45-Q1 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled ( $t_{dis}$ ) before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay ( $t_{pd}$ ). To avoid bus contention care should be taken to not apply an input signal prior to the output port being disabled ( $t_{dis}$  maximum).

### 9.2 Typical Application

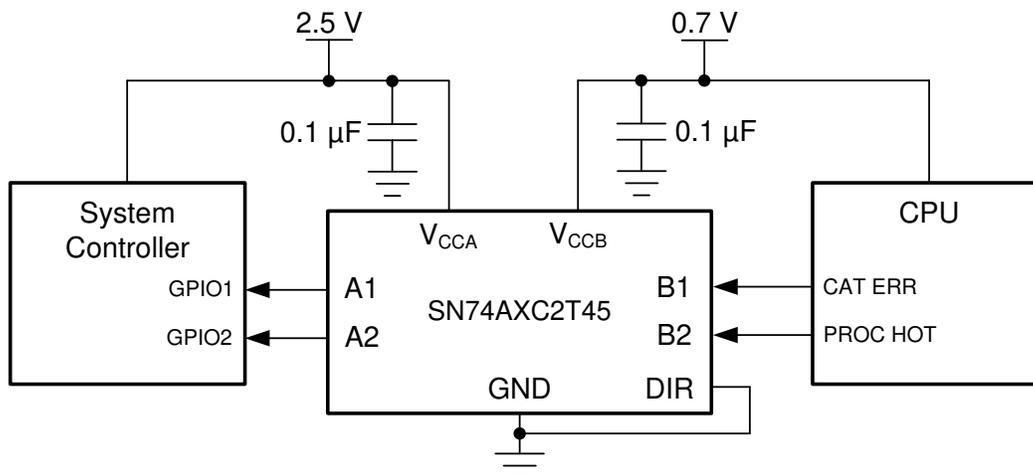


Figure 9-1. Processor Error Application

### 9.2.1 Design Requirements

For this design example, use the parameters listed in [Table 9-1](#).

**Table 9-1. Design Parameters**

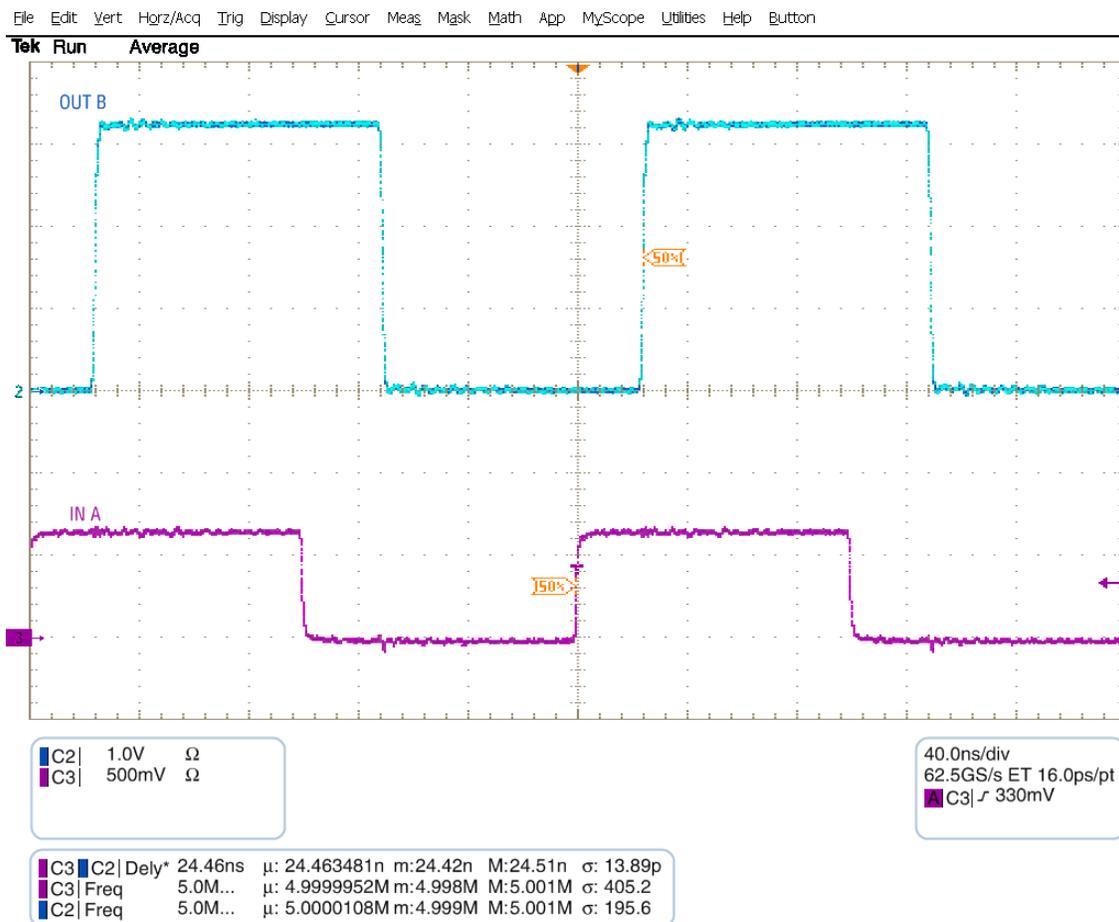
DESIGN PARAMETERS	EXAMPLE VALUES
Input voltage range	0.65 V to 3.6 V
Output voltage range	0.65 V to 3.6 V

### 9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74AXC2T45-Q1 device to determine the input voltage range. For a valid logic-high, the value must exceed the high-level input voltage ( $V_{IH}$ ) of the input port. For a valid logic low the value must be less than the low-level input voltage ( $V_{IL}$ ) of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74AXC2T45-Q1 device is driving to determine the output voltage range.

### 9.2.3 Application Curve



**Figure 9-2. Up Translation at 2.5 MHz (0.7 V to 3.3 V)**

## 10 Power Supply Recommendations

Always apply a ground reference to the GND pins first. This device is designed for glitch free power sequencing without any supply sequencing requirements such as ramp order or ramp rate.

This device is designed with various power supply sequencing methods in mind to help prevent unintended triggering of downstream devices. For more information regarding the power up glitch performance of the AXC family of level translators, see the [Glitch Free Power Sequencing With AXC Level Translators](#) application report.

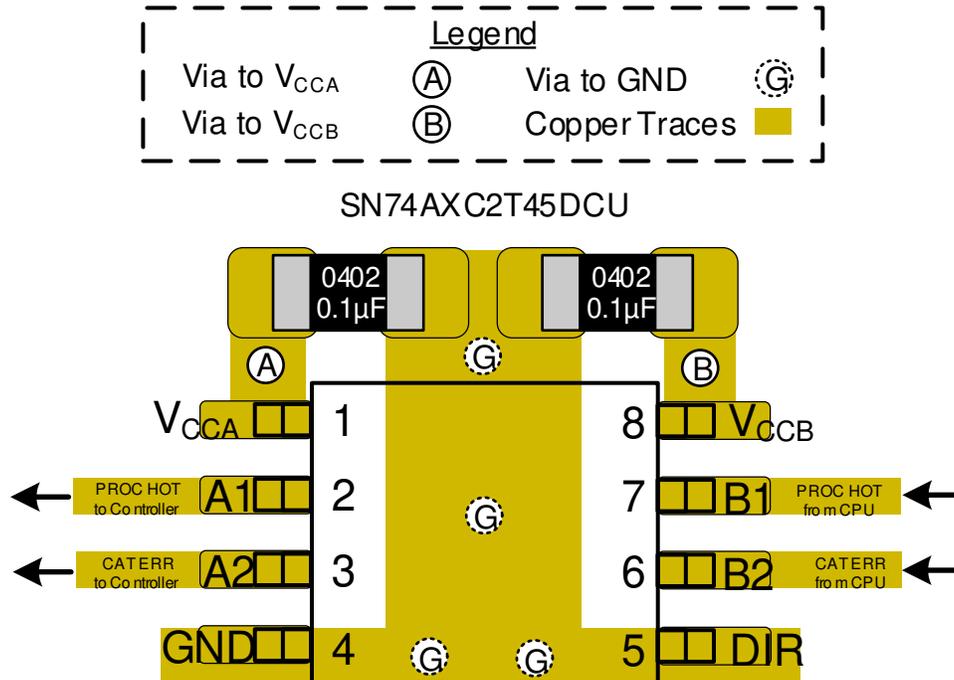
## 11 Layout

### 11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines are recommended:

- Use bypass capacitors on the power supply pins and place them as close to the device as possible. A 0.1  $\mu\text{F}$  capacitor is recommended, but transient performance can be improved by having both 1  $\mu\text{F}$  and 0.1  $\mu\text{F}$  capacitors in parallel as bypass capacitors.
- Use short trace lengths to avoid excessive loading.

### 11.2 Layout Example



## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Implications of Slow or Floating CMOS Inputs application report](#)
- Texas Instruments, [Power Sequencing for AXC Family of Devices application report](#)

#### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 12.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

#### 12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

#### 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 12.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AXC2T45QDCURQ1	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2FZT	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

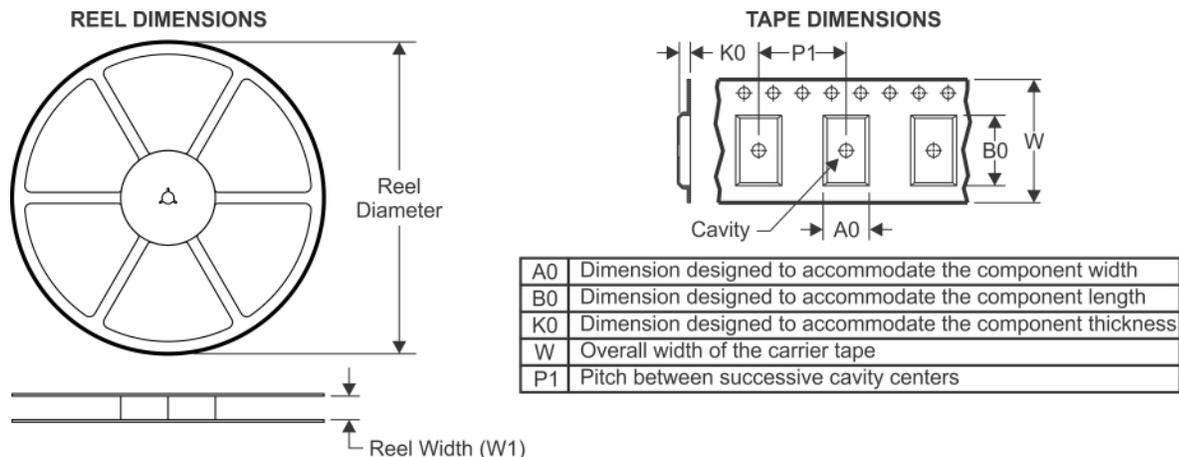
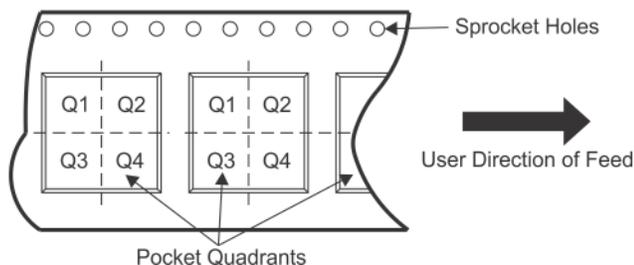
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74AXC2T45-Q1 :**

- Catalog : [SN74AXC2T45](#)

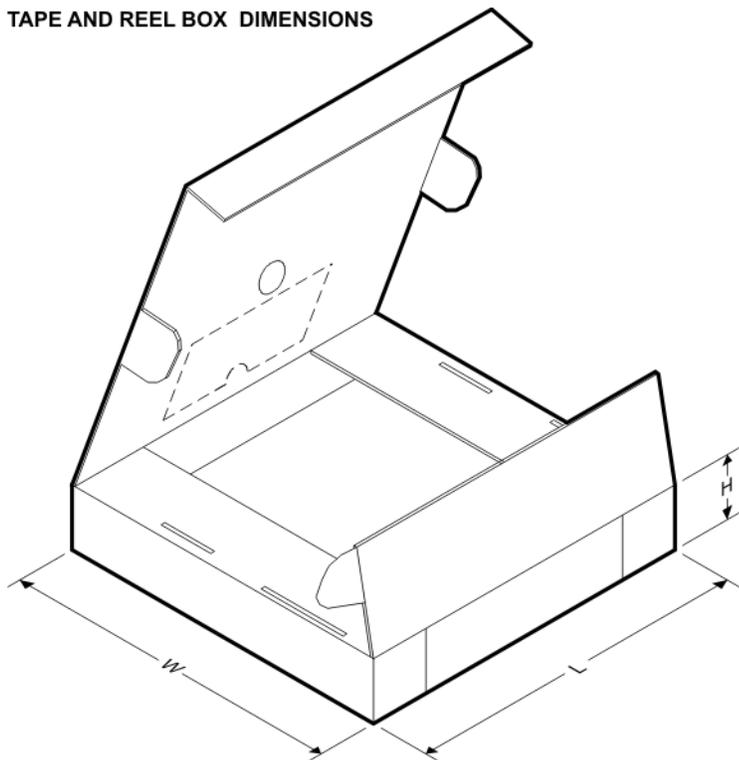
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AXC2T45QDCURQ1	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AXC2T45QDCURQ1	VSSOP	DCU	8	3000	180.0	180.0	18.0

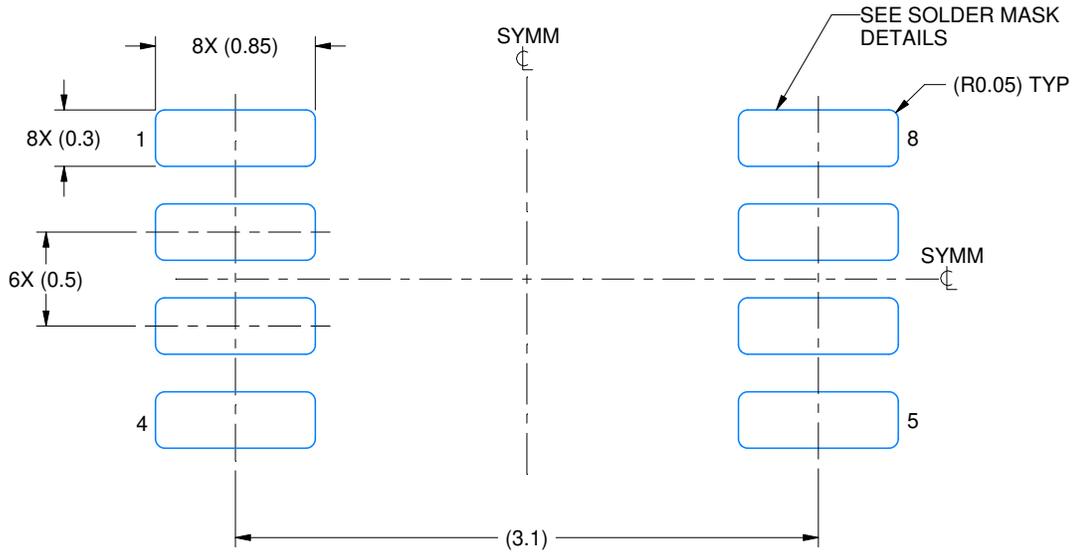


# EXAMPLE BOARD LAYOUT

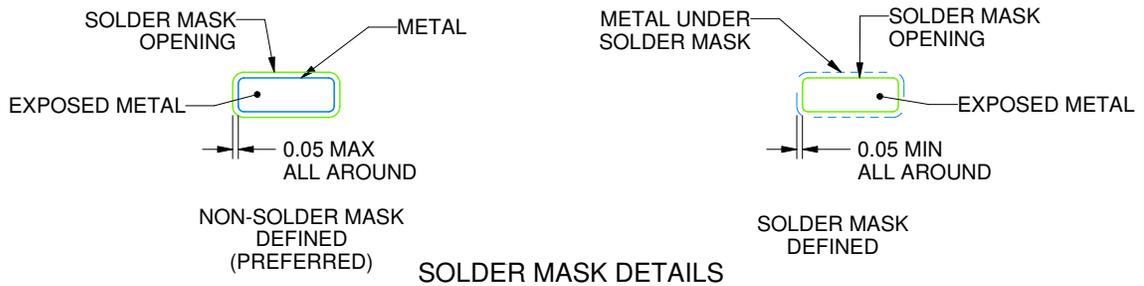
DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 25X



4225266/A 09/2014

NOTES: (continued)

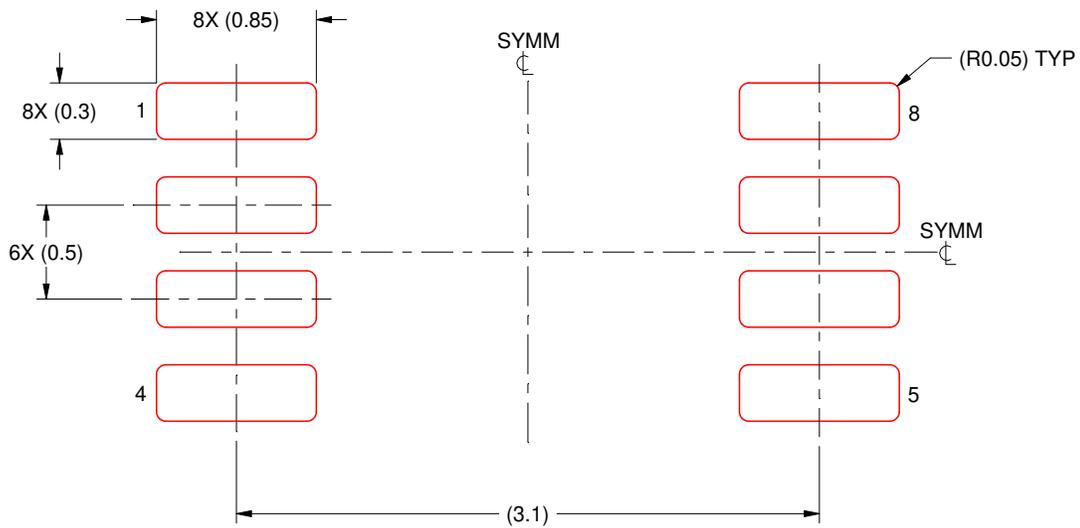
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2023, Texas Instruments Incorporated