RELIABILITY REPORT

FOR

MAX8796GTJ+

PLASTIC ENCAPSULATED DEVICES

November 30, 2010

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Conclusion

The MAX8796GTJ+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim''s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim''s quality and reliability standards.

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I. Device Description

A. General

The MAX8796/MAX8797/MAX17401 are 1-phase Quick-PWM(tm) step-down VID power-supply controllers for Intel notebook CPUs and graphics. The Quick-PWM control provides instantaneous response to fast load current steps. Active voltage positioning reduces power dissipation and bulk output capacitance requirements and allows ideal positioning compensation for tantalum, polymer, or ceramic bulk output capacitors. The MAX8796/MAX8797/MAX17401 are intended for two different notebook CPU/GPU core applications: either bucking down the battery directly to create the core voltage, or else bucking down the +5V system supply. The single-stage conversion method allows this device to directly step down high-voltage batteries for the highest possible efficiency. Alternatively, 2-stage conversion (stepping down the +5V system supply instead of the battery) at higher switching frequency provides the minimum possible physical size. A slew-rate controller allows controlled transitions between VID codes. A thermistor-based temperature sensor provides programmable thermal protection. A power monitor provides an analog voltage output proportional to the power consumed by the CPU/GPU. The MAX8796/MAX17401 implement both the Intel IMVP-6 CPU core specifications, as well as the Intel GMCH graphics core specifications. The MAX8797 implements the Intel GMCH graphics core specifications. The MAX8796/MAX17401 are available in a 32-pin TQFN package. The MAX8797 is available in a 28-pin TQFN package.

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II. Manufacturing Information

A. Description/Function: 1-Phase, Quick-PWM Intel IMVP-6/GMCH Controllers
B. Process: S45
C. Number of Device Transistors: 10146
D. Fa brication Location: Texas
E. Assembly Location: Thailand
F. Date of Initial Production: January 22, 2010

III. Packaging Information

A. Package Type: 32-pin TQFN 5x5
B. Lead Frame: Copper
C. Lead Finish: 100% matte Tin
D. Die Attach: Conductive
E. Bondwire: Au (1 mil dia.)
F. Mold Material: Epoxy with silica filler
G. Assembly Diagram: #05-9000-2634
H. Flammability Rating: Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C: Level 1
J. Single Layer Theta Ja: 47°C/W
K. Single Layer Theta Jc: 1.7°C/W
L. Multi Layer Theta Ja: 29°C/W
M. Multi Layer Theta Jc: 2.7°C/W

IV. Die Information

A. Dimensions: 77 X 73 mils
B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect: Al/0.5%Cu with Ti/TiN Barrier
D. B ackside Metallization: None
E. Minimum Metal Width: Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing: Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions: 5 mil. Sq.
H. I solation Dielectric: SiO_2
I. Die Separation Method: Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. S ampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 96 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 11.4 \times 10^{-9}$

λ = 11.4 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim"s reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the S45 Process results in a FIT Rate of 0.49 @ 25C and 8.49 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (ESD lot TDCZGA027D D/C 0846, Latchup lot SDCZCA004H D/C 0802)

The PE11 die type has been found to have all pins able to withstand a HBM transient pulse of +/-300 per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA.

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Table 1
Reliability Evaluation Test Results

MAX8796GTJ+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C	DC Parameters	48	0	TDCZGQ002B, DC 0816
	Biased	& functionality	48	0	TDCZGQ002A, DC 0816
	Time = 192 hrs.				

Note 1: Life Test Data may represent plastic DIP qualification lots.

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