

CY7C1051DV33

8-Mbit (512 K × 16) Static RAM

Features

- Temperature ranges □ -40 °C to 85 °C
- High speed □ t_{AA} = 10 ns
- Low active power
 I_{CC} = 110 mA at f = 100 MHz
- Low CMOS standby power □ I_{SB2} = 20 mA
- 2.0-V data retention
- Automatic power-down when deselected
- Transistor-transistor logic (TTL)-compatible inputs and outputs
- Easy memory expansion with CE and OE features
- Available in Pb-free 48-ball fine ball grid array (FBGA) and 44-pin thin small outline package (TSOP) II packages

Functional Description

The CY7C1051DV33 is a high performance CMOS Static RAM organized as 512 K words by 16-bits.

To write to the device, take Chip Enable $\overline{(CE)}$ and Write Enable $\overline{(WE)}$ inputs LOW. If Byte LOW Enable (BLE) is LOW, then data from I/O pins (I/O₀–I/O₇), is written into the location specified on the address pins (A₀–A₁₈). If Byte HIGH Enable (BHE) is LOW, then data from I/O pins (I/O₈–I/O₁₅) is written into the location specified on the address pins (A₀–A₁₈).

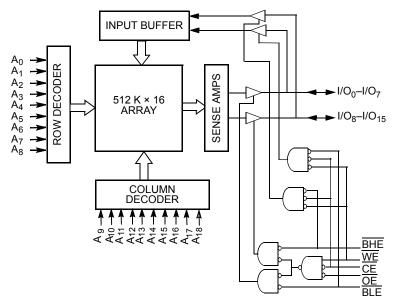
To read from the device, take Chip Enable ($\overline{\text{CE}}$) and Output Enable ($\overline{\text{OE}}$) LOW while forcing the Write Enable (WE) HIGH. If Byte LOW Enable (BLE) is LOW, then data from the memory location specified by the address pins appears on I/O₀–I/O₇. If Byte HIGH Enable (BHE) is LOW, then data from memory appears on I/O₈ to I/O₁₅. See the Truth Table on page 10 for a complete description of read and write modes.

The input/output pins $(I/O_0-I/O_{15})$ are placed in a high-impedance state when the device is deselected (CE HIGH), the outputs are disabled (OE HIGH), the BHE and BLE are disabled (BHE, BLE HIGH), or a write operation (CE LOW, and WE LOW) is in progress.

The CY7C1051DV33 is available in a 44-pin TSOP II package with center power and ground (revolutionary) pinout and a 48-ball FBGA package.

For a complete list of related documentation, click here.

Logic Block Diagram



Cypress Semiconductor Corporation Document Number: 001-00063 Rev. *J



CY7C1051DV33

Contents

Pin Configurations	3
Selection Guide	
Maximum Ratings	4
Operating Range	
DC Electrical Characteristics	
Capacitance	4
Thermal Resistance	
AC Test Loads and Waveforms	
Data Retention Characteristics	5
Data Retention Waveform	
AC Switching Characteristics	
Switching Waveforms	
Truth Table	

Ordering Information	11
Ordering Code Definitions	11
Package Diagrams	12
Acronyms	13
Document Conventions	13
Units of Measure	13
Document History Page	14
Sales, Solutions, and Legal Information	15
Worldwide Sales and Design Support	15
Products	15
PSoC® Solutions	15
Cypress Developer Community	15
Technical Support	15





Pin Configurations

Figure 1. Pin Diagram - 48-ball FBGA (Top View)^[1]

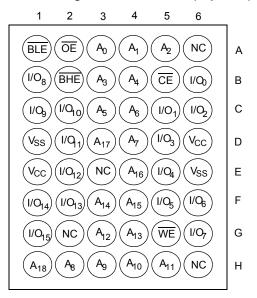


Figure 2. Pin Diagram - 44-Pin TSOP II (Top View)^[1]

	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21	 33 32 31 30 29 28 27 26 25 	מתתתתתתתתתתתתתתתתת.	A17 A16 <u>OBHE</u> J/O154 J/O13 J/O12 VSS VCC11 J/O10 J/O8 A14 A13 A14
A7 A8 A9 D				A ₁₂ A ₁₁ A ₁₀

Selection Guide

Description	-10	-12	Unit
Maximum access time	10	12	ns
Maximum operating current	110	100	mA
Maximum CMOS standby current	20	20	mA



Maximum Ratings

Exceeding the maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature65 °C to +150 °C
Ambient temperature with power applied55 °C to +125 °C
Supply voltage on V_{CC} to relative $GND^{[2]}$ –0.5 V to +4.6 V
DC voltage applied to outputs in high-Z state $^{[2]}$ 0.3 V to V_{CC} + 0.3 V
DC input voltage $^{[2]}$ 0.3 V to V_{CC} + 0.3 V
Current into outputs (LOW)

DC Electrical Characteristics

Over the Operating Range

Static discharge voltage.....>2001 V

(per MIL-STD-883, Method 3015)

Latch-up current>200 mA

Operating Range

Range	Ambient Temperature	V _{cc}	Speed
Industrial	–40 °C to +85 °C	$3.3~V\pm0.3~V$	10 ns
Industrial	–40 °C to +85 °C	$3.3~V\pm0.3~V$	12 ns

Deremeter	Description	Test Conditions		-10	-12		Unit
Parameter	Description	Test Conditions	Min	Max	Min	Max	Unit
V _{OH}	Output HIGH voltage	Min V _{CC} , I _{OH} = –4.0 mA	2.4	-	2.4	-	V
V _{OL}	Output LOW voltage	Min V _{CC} , I _{OL} = 8.0 mA	-	0.4	-	0.4	V
V _{IH} ^[2]	Input HIGH voltage		2.0	V _{CC} + 0.3	2.0	V _{CC} + 0.3	V
V _{IL} [2]	Input LOW voltage		-0.3	0.8	-0.3	0.8	V
I _{IX}	Input leakage current	$GND \leq V_{IN} \leq V_{CC}$	-1	+1	-1	+1	μA
I _{OZ}	Output leakage current	$GND \leq V_{OUT} \leq V_{CC}$, Output Disabled	–1	+1	–1	+1	μΑ
I _{CC}	V _{CC} operating supply current	$f = f_{MAX} = 1/t_{RC}$	-	110	-	100	mA
I _{SB1}	Automatic CE power down current —TTL inputs	$ \begin{array}{l} \text{Max } V_{CC}, \ \overline{CE} \geq V_{IH} \\ V_{IN} \geq V_{IH} \ \text{or} \ V_{IN} \leq V_{IL}, \ f = f_{MAX} \end{array} $	-	40	-	35	mA
I _{SB2}	Automatic CE Power Down Current —CMOS Inputs	$\begin{array}{l} \mbox{Max V}_{CC}, \ \overline{CE} \geq V_{CC} - 0.3 \ \mbox{V}, \\ \mbox{V}_{IN} \geq V_{CC} - 0.3 \ \mbox{V or } V_{IN} \leq 0.3 \ \mbox{V}, f \\ \mbox{=} 0 \end{array}$	-	20	-	20	mA

Capacitance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description Test Conditions		Max	Unit
C _{IN}	Input capacitance	$T_A = 25 ^{\circ}C, f = 1 \text{MHz}, V_{CC} = 3.3 \text{V}$	12	pF
C _{OUT}	I/O capacitance		12	pF

Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	FBGA Package	TSOP II Package	Unit
Θ _{JA}	Thermal resistance (Junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	28.31	51.43	°C/W
Θ _{JC}	Thermal resistance (Junction to case)		11.4	15.8	°C/W

Note 2. $V_{IL(min)}$ = -2.0 V and $V_{IH(max)}$ = V_{CC} + 2.0 V for pulse durations of less than 20 ns.



AC Test Loads and Waveforms

AC characteristics (except High-Z) are tested using the load conditions shown in Figure 3 (a). High-Z characteristics are tested for all speeds using the test load shown in Figure 3 (c).

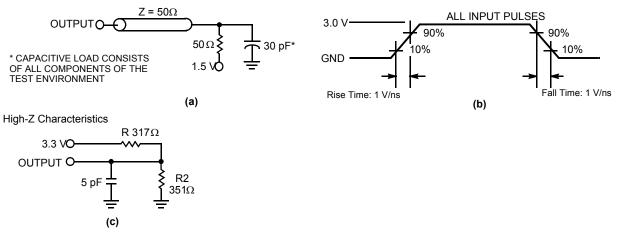


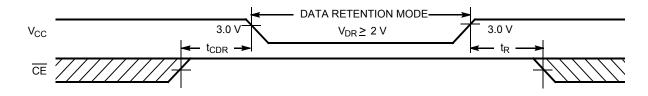
Figure 3. AC Test Loads and Waveforms

Data Retention Characteristics

Over the Operating Range

Parameter	Description	Min	Max	Unit	
V _{DR}	V _{CC} for Data Retention		2.0	-	V
I _{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0 \text{ V}, \overline{CE} \ge V_{CC} - 0.3 \text{ V},$ $V_{IN} \ge V_{CC} - 0.3 \text{ V} \text{ or } V_{IN} \le 0.3 \text{ V}$	-	20	mA
Topp!'	Chip Deselect to Data Retention Time	$V_{IN} \ge V_{CC} - 0.3 \text{ V or } V_{IN} \le 0.3 \text{ V}$	0	-	ns
t _R [4]	Operation Recovery Time		t _{RC}	_	ns

Data Retention Waveform



Notes

^{3.} No inputs may exceed V_{CC} + 0.3 V 4. Full device operation requires linear V_{CC} ramp from V_{DR} to V_{CC}(min) \geq 50 µs or stable at V_{CC}(min) \geq 50 µs.



AC Switching Characteristics

Over the Operating Range^[5]

Demonstern	Description	-	-10	-12		11
Parameter	Description	Min	Max	Min	Мах	Unit
Read Cycle	•				•	-
t _{power} ^[6]	V _{CC} (typical) to the First Access	100	-	100	-	μS
t _{RC}	Read Cycle Time	10	-	12	_	ns
t _{AA}	Address to Data Valid	-	10	-	12	ns
t _{OHA}	Data Hold from Address Change	2.5	-	2.5	_	ns
t _{ACE}	CE LOW to Data Valid	-	10	-	12	ns
t _{DOE}	OE LOW to Data Valid	_	5	_	6	ns
t _{LZOE}	OE LOW to Low-Z	0	_	0	_	ns
t _{HZOE}	OE HIGH to High-Z ^[7, 8]	_	5	_	6	ns
t _{LZCE}	CE LOW to Low-Z ^[8]	3	_	3	_	ns
t _{HZCE}	CE HIGH to High-Z ^[7, 8]	_	5	_	6	ns
t _{PU}	CE LOW to Power Up	0	_	0	_	ns
t _{PD}	CE HIGH to Power Down	_	10	_	12	ns
t _{DBE}	Byte Enable to Data Valid	_	5	_	6	ns
t _{LZBE}	Byte Enable to Low-Z	0	_	0	_	ns
t _{HZBE}	Byte Disable to High-Z	_	5	_	6	ns
Write Cycle ^{[9, 1}	10]				•	-
t _{WC}	Write Cycle Time	10	_	12	_	ns
t _{SCE}	CE LOW to Write End	7	_	8	_	ns
t _{AW}	Address Setup to Write End	7	_	8	_	ns
t _{HA}	Address Hold from Write End	0	-	0	_	ns
t _{SA}	Address Setup to Write Start	0	-	0	_	ns
t _{PWE}	WE Pulse Width	7	-	8	-	ns
t _{SD}	Data Setup to Write End	5	-	6	-	ns
t _{HD}	Data Hold from Write End	0	-	0	-	ns
t _{LZWE}	WE HIGH to Low-Z ^[8]	3	3 –		-	ns
t _{HZWE}	WE LOW to High-Z ^[7, 8]	_	5		6	ns
t _{BW}	Byte Enable to End of Write	7	-	8	-	ns
			1		1	

Notes

- Notes
 5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.
 6. t_{POWER} gives the minimum amount of time that the power supply must be at typical V_{CC} values until the first memory access can be performed.
 7. t_{HZOE}, t_{HZEE} and t_{HZWE} are specified with a load capacitance of 5 pF as in part (d) of "AC Test Loads and Waveforms" on page 5. Transition is measured when the outputs enter a high impedance state.
 8. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZDE} is less than t_{LZDE}, t_{HZBE} and t_{HZWE} is less than t_{LZWE} for any device.
 9. The internal write time of the memory is defined by the overlap of CE LOW, and WE LOW. CE and WE must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data setup and hold timing must refer to the leading edge of the signal that terminates the write.
 10. The minimum write cycle time for Write Cycle No. 3 (WE controlled, OE LOW) is the sum of t_{HZWE} and t_{SD}.



Switching Waveforms

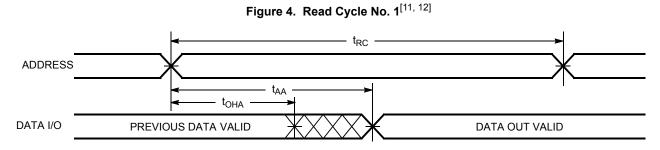
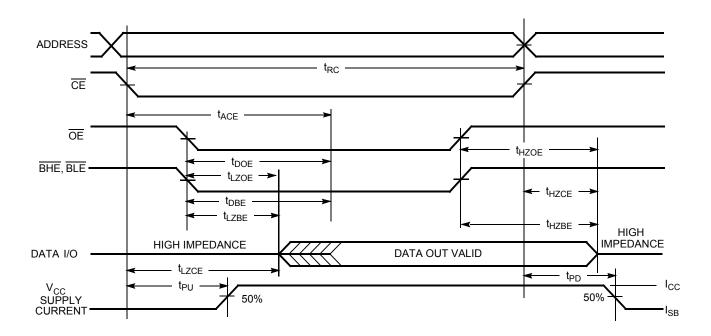


Figure 5. Read Cycle No. 2 (OE Controlled) ^[12, 13]



Notes

- 11. <u>Dev</u>ice is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$, \overline{BHE} , \overline{BLE} , or both = V_{IL} . 12. WE is HIGH for Read cycle. 13. Address valid before or coincident with \overline{CE} transition LOW.



Switching Waveforms (continued)

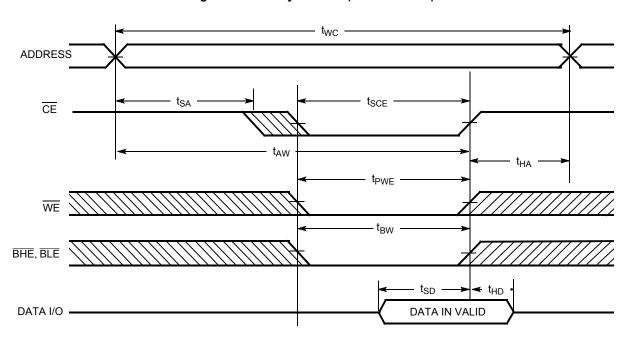
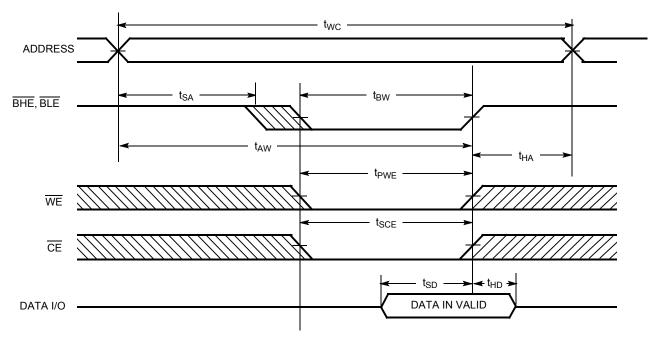


Figure 6. Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled) [14, 15]

Figure 7. Write Cycle No. 2 (BLE or BHE Controlled)



Notes

14. Data I/O is high-impedance if OE, or BHE, BLE, or both = V_{IH}.
 15. If CE goes HIGH simultaneously with WE going HIGH, the output remains in a high-impedance state.



Switching Waveforms (continued)

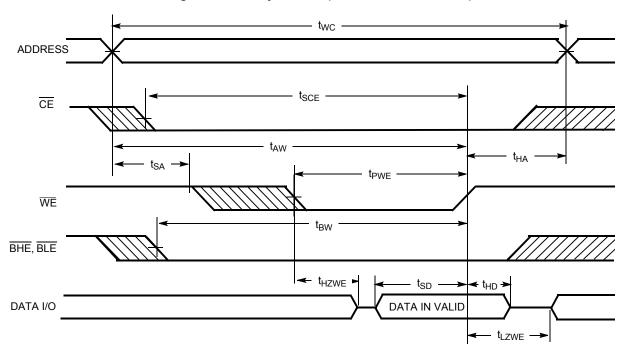


Figure 8. Write Cycle No. 3 (WE Controlled, OE LOW) ^[16]



Truth Table

CE	OE	WE	BLE	BHE	I/O ₀ –I/O ₇	I/O ₈ –I/O ₁₅	Mode	Power
Н	Х	Х	Х	Х	High-Z	High-Z	Power Down	Standby (I _{SB})
L	L	Н	L	L	Data Out	Data Out	Read All Bits	Active (I _{CC})
L	L	Н	L	Н	Data Out	High-Z	Read Lower Bits Only	Active (I _{CC})
L	L	Н	Н	L	High-Z	Data Out	Read Upper Bits Only	Active (I _{CC})
L	Х	L	L	L	Data In	Data In	Write All Bits	Active (I _{CC})
L	Х	L	L	Н	Data In	High-Z	Write Lower Bits Only	Active (I _{CC})
L	Х	L	Н	L	High-Z	Data In	Write Upper Bits Only	Active (I _{CC})
L	Н	Н	Х	Х	High-Z	High-Z	Selected, Outputs Disabled	Active (I _{CC})



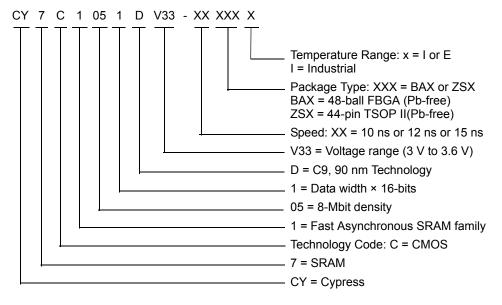
Ordering Information

Cypress offers other versions of this type of product in many different configurations and features. The following table contains only the list of parts that are currently available. For a complete listing of all options, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products or contact your local sales representative. Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives and distributors. To find the office closest to you, visit us at http://www.cypress.com/go/datasheet/offices.

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1051DV33-10BAXI	51-85193	48-ball FBGA (Pb-free)	Industrial
	CY7C1051DV33-10ZSXI	51-85087	44-pin TSOP II (Pb-free)	
12	CY7C1051DV33-12ZSXI	51-85087	44-pin TSOP II (Pb-free)	Industrial

Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions

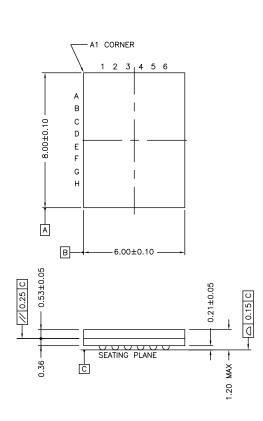


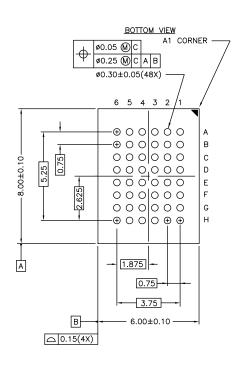


Package Diagrams

Figure 9. 48-Ball FBGA (6 x 8 x 1.2 mm), 51-85193

TOP VIEW



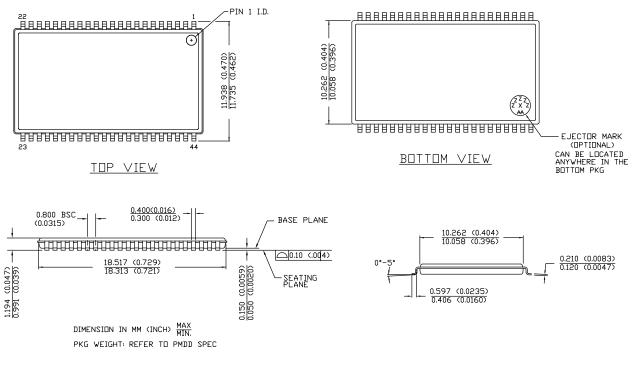


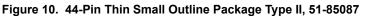
REFERENCE JEDEC MO-207

51-85193 *C



Package Diagrams (continued)





51-85087 *E

Acronyms

Acronym	Description	
CE	chip enable	
CMOS	complementary metal oxide semiconductor	
I/O	input/output	
OE	output enable	
SRAM	static random access memory	
SOJ	small outline J-lead	
TSOP	thin small outline package	
VFBGA	very fine-pitch ball grid array	

Document Conventions

Units of Measure

Symbol	Unit of Measure	
ns	nanosecond	
V	volt	
μA	microampere	
mA	milliampere	
mV	millivolt	
mW	milliwatt	
MHz	megahertz	
pF	picofarad	
°C	degree Celsius	
W	watt	



Document History Page

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	342195	PCI	See ECN	New Datasheet
*A	380574	SYT	See ECN	Redefined I _{CC} values for Com'l and Ind'l temperature ranges I_{CC} (Com'l): Changed from 110, 90 and 80 mA to 110, 100 and 95 mA for 8, 10 and 12 ns speed bins respectively I_{CC} (Ind'l): Changed from 110, 90 and 80 mA to 120, 110 and 105 mA for 8, 10 and 12 ns speed bins respectively Changed the Capacitance values from 8 pF to 10 pF on Page # 3
*B	485796	NXR	See ECN	Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court" Removed -8 and -12 Speed bins from product offering, Removed Commercial Operating Range option, Modified Maximum Ratings for DC input voltage from -0.5 V to -0.3 V and V_{CC} + 0.5 V to V_{CC} + 0.3 V Changed the Description of I _{IX} from Input Load Current to Input Leakage Current. Changed t _{HZBE} from 5 ns to 6 ns Updated footnote #7 on High-Z parameter measurement Added footnote #11 Updated the Ordering Information table and Replaced Package Name column with Package Diagram.
*C	866000	NXR	See ECN	Changed ball E3 from V _{SS} to NC in FBGA pin configuration
*D	1513285	VKN/AESA	See ECN	Converted from preliminary to final Changed t _{HZBE} from 6 ns to 5 ns for 10 ns speed bin Added 12 ns speed bin Changed t _{OHA} spec from 3 ns to 2.5 ns Updated Ordering information table
*E	2911009	VKN	04/12/10	Replaced 48-Ball (7 x 8.5 x 1.2 mm) FBGA with 48-Ball (6 x 8 x 1.2mm) FBGA Updated Package diagrams, Updated ordering information.
*F	3086522	PRAS	11/15/2010	Included Auto-E information (preliminary) in Ordering Information.
*G	3112625	AJU	12/16/2010	Added Ordering Code Definitions.
*H	3369149	TAVA	09/12/2011	Removed all references to Automotive information.
*	4530449	MEMJ	10/10/2014	Updated Switching Waveforms: Added Note 16 and referred the same note in Figure 8. Updated Package Diagrams: spec 51-85087 – Changed revision from *D to *E. Updated in new template. Completing Sunset Review.
*J	4578447	MEMJ	01/16/2015	Added related documentation hyperlink in page 1. Removed the prune part number CY7C1051DV33-12BAXI in Ordering Information.



Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc
Memory	cypress.com/go/memory
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC[®] Solutions

psoc.cypress.com/solutions PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community Community | Forums | Blogs | Video | Training

Technical Support cypress.com/go/support

© Cypress Semiconductor Corporation, 2005-2015. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.

Document Number: 001-00063 Rev. *J

Revised January 16, 2015

All products and company names mentioned in this document may be the trademarks of their respective holders.