

MOSFET - Power, Single N-Channel

80 V, 6.7 mΩ, 80 A

NVMFS6H836N

Features

- Small Footprint (5x6 mm) for Compact Design
- Low R_{DS(on)} to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- NVMFS6H836NWF – Wettable Flank Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halide Free, and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		V _{DSS}	80	V	
Gate-to-Source Voltage		V _{GS}	±20	V	
Continuous Drain Current R _{θJC} (Notes 1, 3)	Steady State	T _C = 25°C	I _D	74	A
		T _C = 100°C		53	
Power Dissipation R _{θJC} (Note 1)		T _C = 25°C	P _D	89	W
		T _C = 100°C		44	
Continuous Drain Current R _{θJA} (Notes 1, 2, 3)	Steady State	T _A = 25°C	I _D	15	A
		T _A = 100°C		11	
Power Dissipation R _{θJA} (Notes 1, 2)		T _A = 25°C	P _D	3.7	W
		T _A = 100°C		1.8	
Pulsed Drain Current	T _A = 25°C, t _p = 10 μs	I _{DM}	432	A	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to +175	°C	
Source Current (Body Diode)		I _S	74	A	
Single Pulse Drain-to-Source Avalanche Energy (I _{L(pk)} = 4.6 A)		E _{AS}	521	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T _L	260	°C	

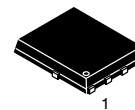
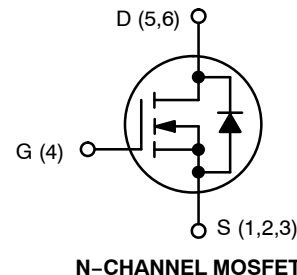
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

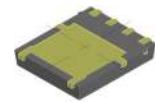
Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State	R _{θJC}	1.7	°C/W
Junction-to-Ambient – Steady State (Note 2)	R _{θJA}	40.6	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

V _{(BR)DSS}	R _{DS(ON) MAX}	I _{D MAX}
80 V	6.7 mΩ @ 10 V	80 A

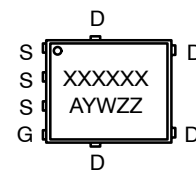


DFN5 (SO-8FL) CASE 488AA STYLE 1



DFNW5 5x6 (FULL-CUT SO8FL WF) CASE 507BA

MARKING DIAGRAM



XXXXXX = 6H836N (NVMFS6H836N) or 836NWF (NVMFS6H836NWF)
 A = Assembly Location
 Y = Year
 W = Work Week
 ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NVMFS6H836N

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			39		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 80\text{ V}$	$T_J = 25^\circ\text{C}$		10	μA
			$T_J = 125^\circ\text{C}$		100	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 95\ \mu\text{A}$	2.0		4.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			-7.3		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 15\text{ A}$		5.6	6.7	m Ω
Forward Transconductance	g_{FS}	$V_{DS} = 15\text{ V}, I_D = 25\text{ A}$		97		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 40\text{ V}$		1640		μF
Output Capacitance	C_{OSS}			230		
Reverse Transfer Capacitance	C_{RSS}			8.0		
Total Gate Charge	$Q_G(TOT)$	$V_{GS} = 10\text{ V}, V_{DS} = 40\text{ V}; I_D = 25\text{ A}$		25		nC
Threshold Gate Charge	$Q_G(TH)$			5.2		
Gate-to-Source Charge	Q_{GS}			8.5		
Gate-to-Drain Charge	Q_{GD}			4.3		
Plateau Voltage	V_{GP}			4.9		

SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 64\text{ V}, I_D = 25\text{ A}, R_G = 2.5\ \Omega$		16		ns
Rise Time	t_r			45		
Turn-Off Delay Time	$t_{d(OFF)}$			41		
Fall Time	t_f			34		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 15\text{ A}$	$T_J = 25^\circ\text{C}$		0.8	1.2	V
			$T_J = 125^\circ\text{C}$		0.7		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 25\text{ A}$		43		ns	
Charge Time	t_a			29			
Discharge Time	t_b			15			
Reverse Recovery Charge	Q_{RR}			54		nC	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

5. Switching characteristics are independent of operating junction temperatures.

NVMFS6H836N

TYPICAL CHARACTERISTICS

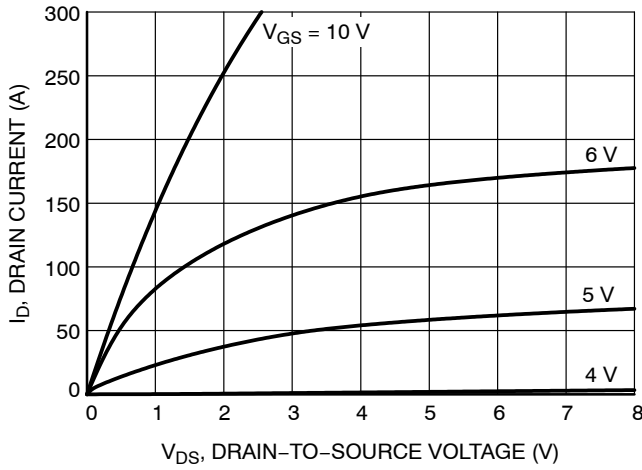


Figure 1. On-Region Characteristics

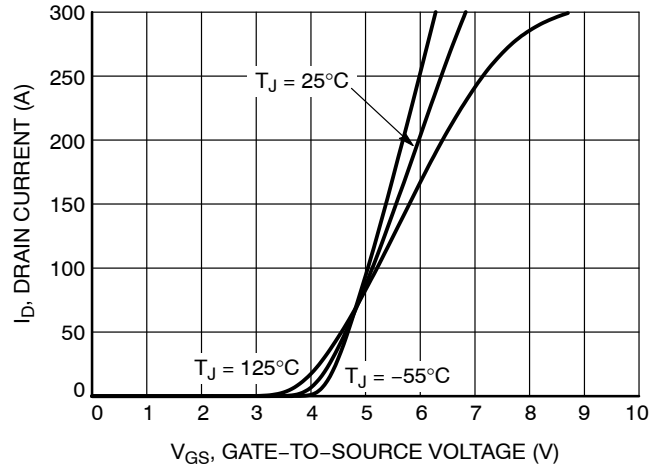


Figure 2. Transfer Characteristics

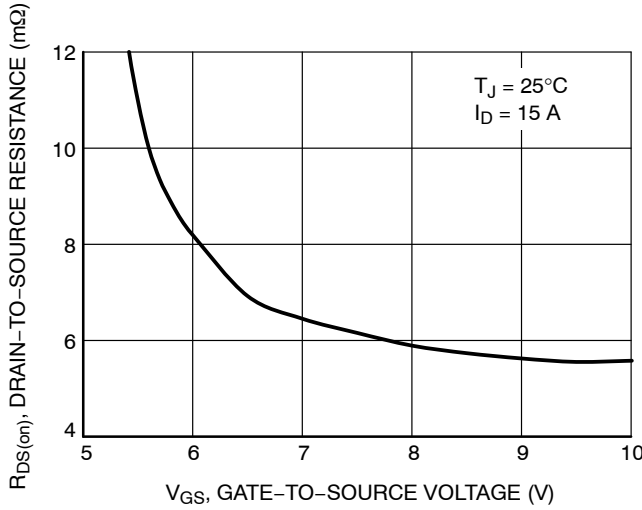


Figure 3. On-Resistance vs. Gate-to-Source Voltage

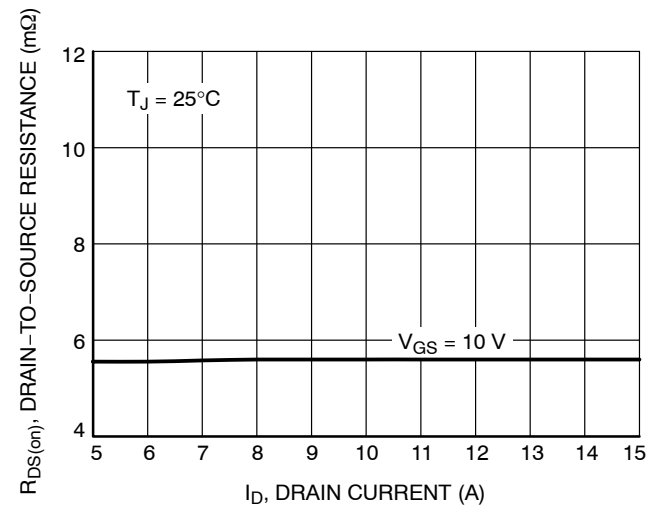


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

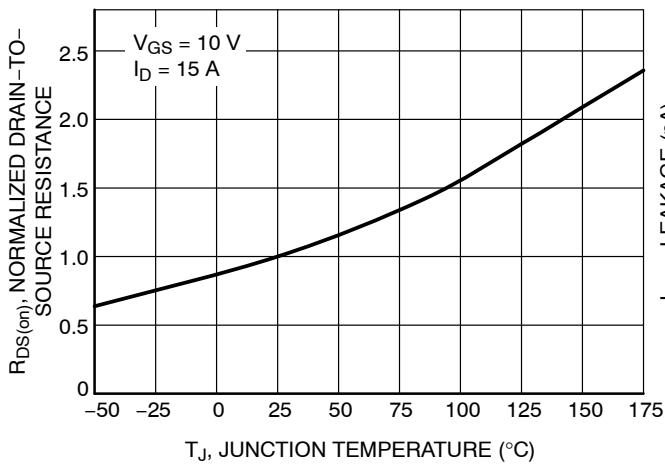


Figure 5. On-Resistance Variation with Temperature

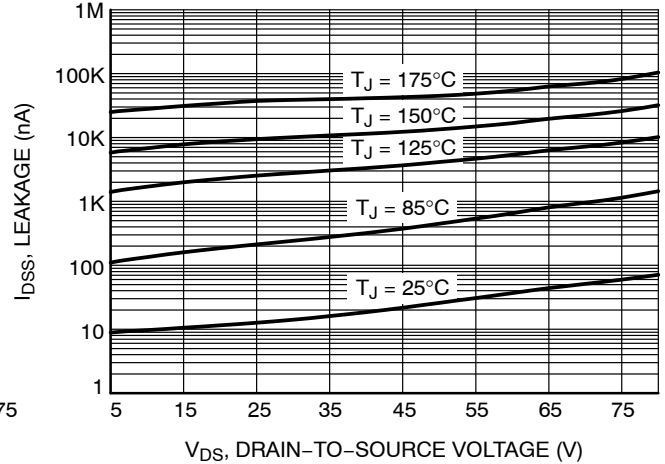


Figure 6. Drain-to-Source Leakage Current vs. Voltage

NVMFS6H836N

TYPICAL CHARACTERISTICS (continued)

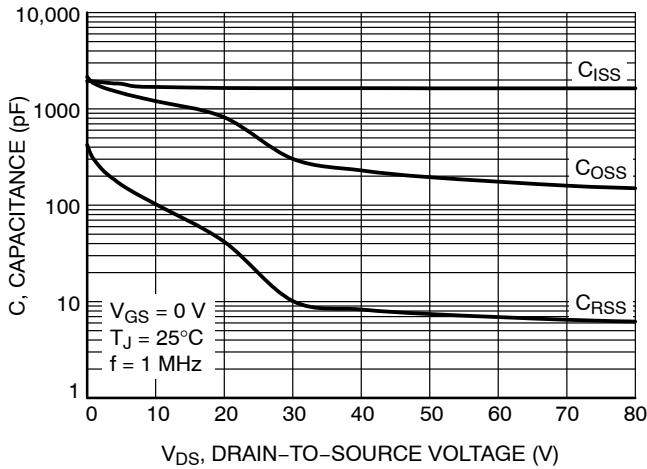


Figure 7. Capacitance Variation

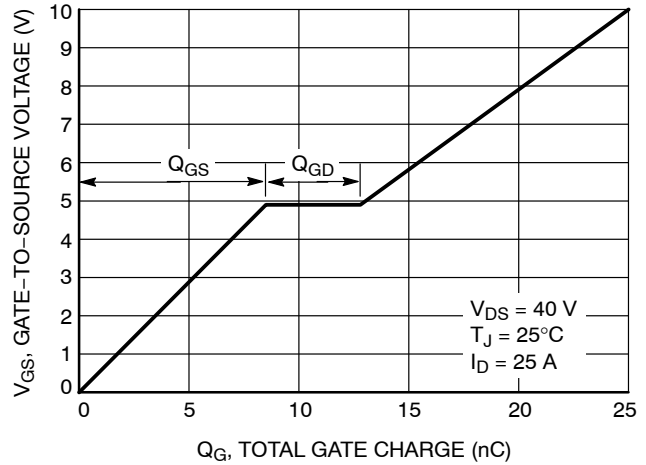


Figure 8. Gate-to-Source Voltage vs. Total Charge

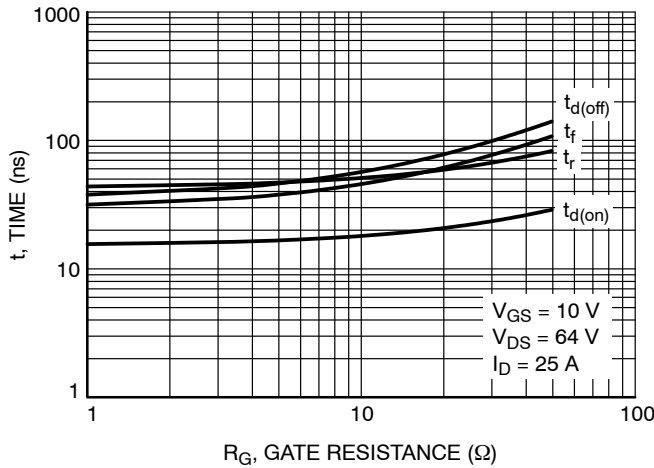


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

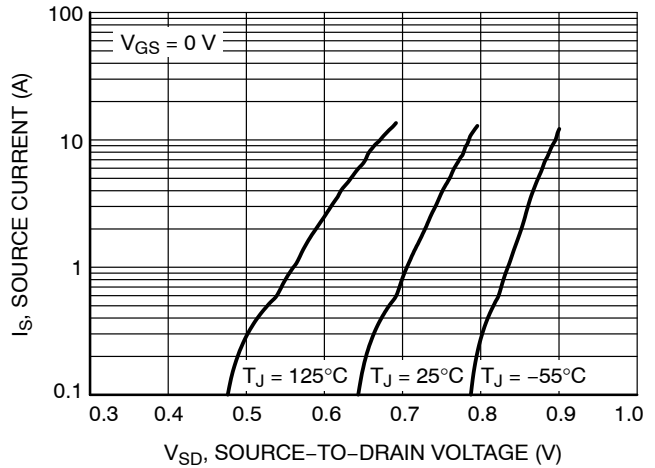


Figure 10. Diode Forward Voltage vs. Current

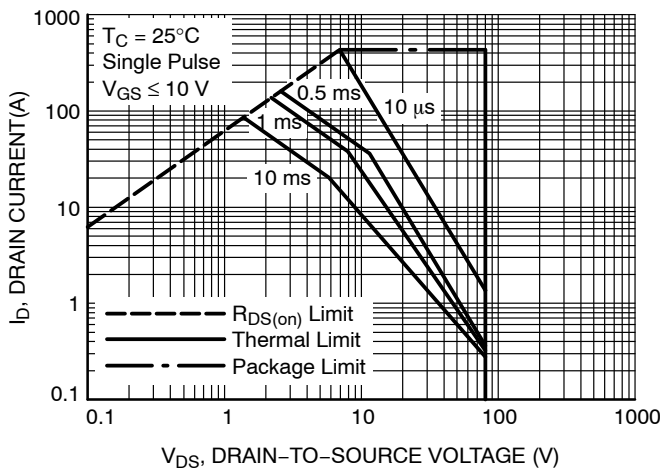


Figure 11. Maximum Rated Forward Biased Safe Operating Area

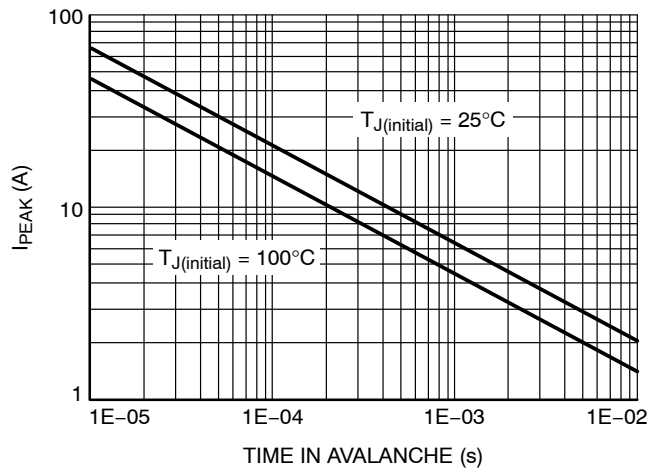


Figure 12. IPEAK vs. Time in Avalanche

NVMFS6H836N

TYPICAL CHARACTERISTICS (continued)

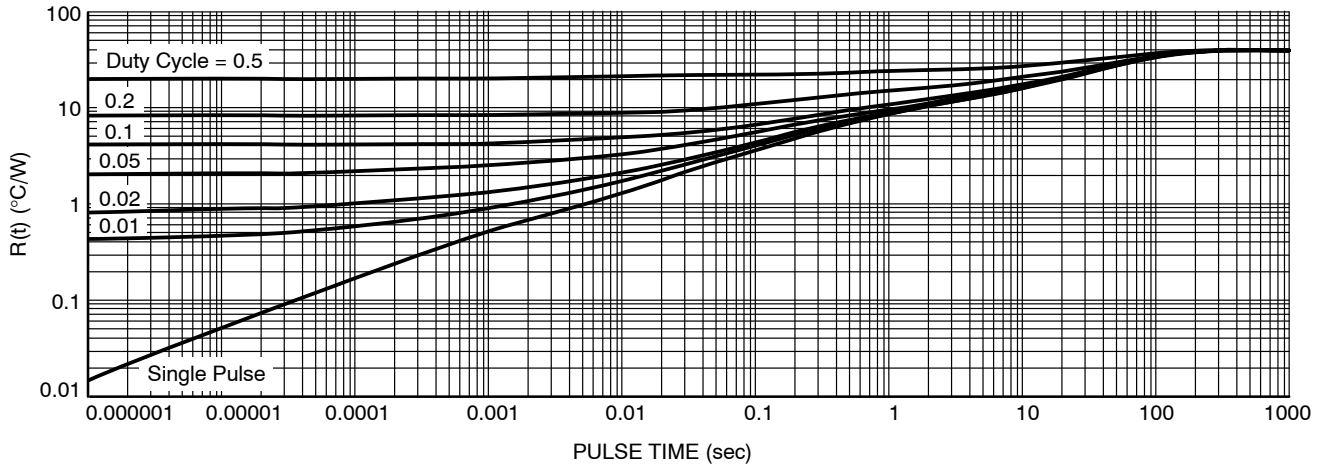


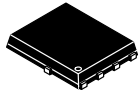
Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NVMFS6H836NT1G	6H836N	DFN5 (Pb-Free, Halide Free)	1500 / Tape & Reel
NVMFS6H836NT3G	6H836N	DFN5 (Pb-Free, Halide Free)	5000 / Tape & Reel
NVMFS6H836NWFT1G	836NWF	DFNW5 (Pb-Free, Halide Free, Wettable Flanks)	1500 / Tape & Reel
NVMFS6H836NWFT3G	836NWF	DFNW5 (Pb-Free, Halide Free, Wettable Flanks)	5000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

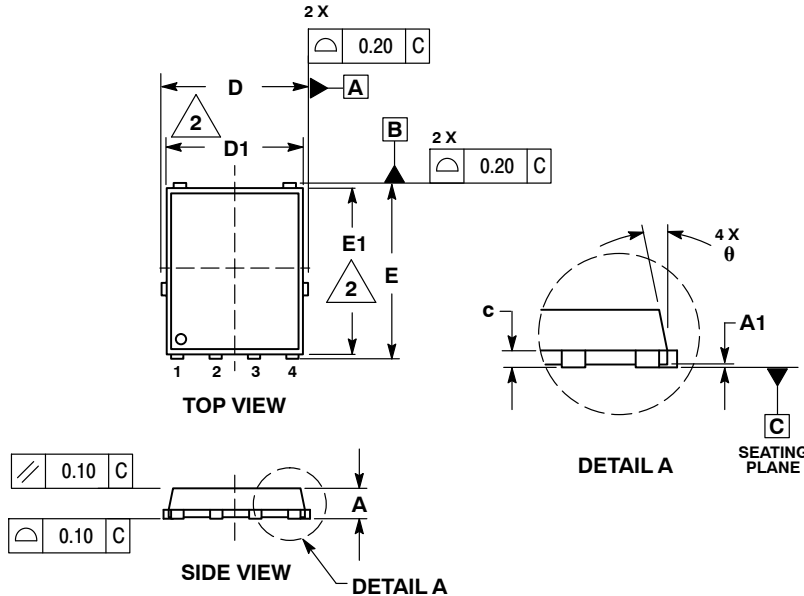
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



1
SCALE 2:1

DFN5 5x6, 1.27P
(SO-8FL)
CASE 488AA
ISSUE N

DATE 25 JUN 2018

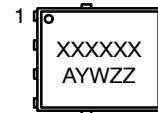


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

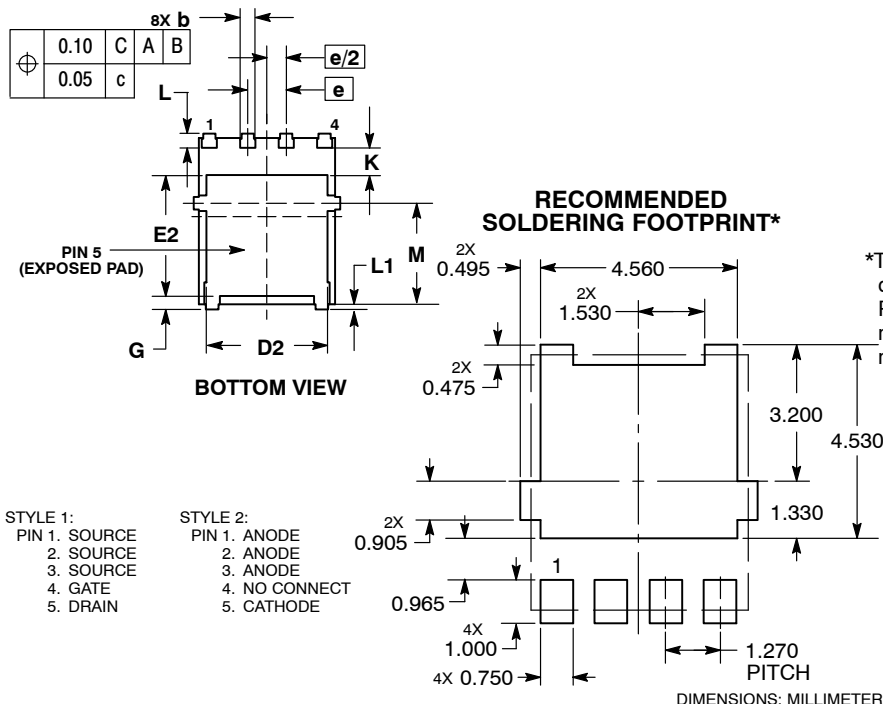
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0°	---	12°

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



- STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
- STYLE 2:
PIN 1. ANODE
2. ANODE
3. ANODE
4. NO CONNECT
5. CATHODE

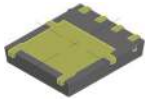
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	DFN5 5x6, 1.27P (SO-8FL)	PAGE 1 OF 1

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

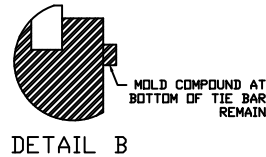
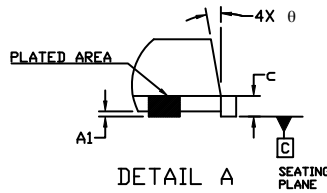
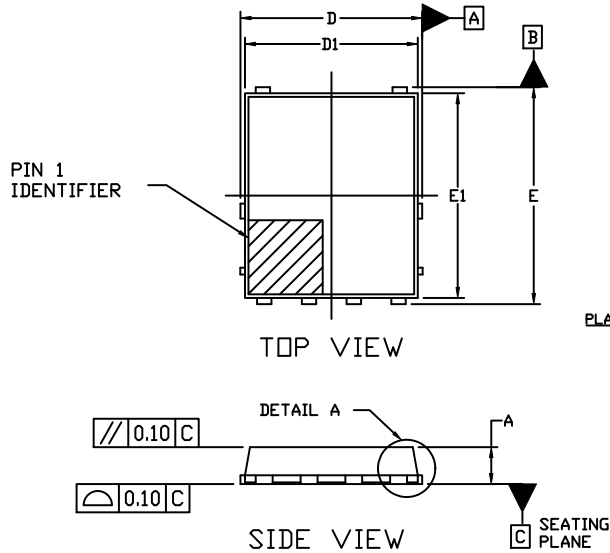


DFNW5 5x6 (FULL-CUT SO8FL WF)

CASE 507BA

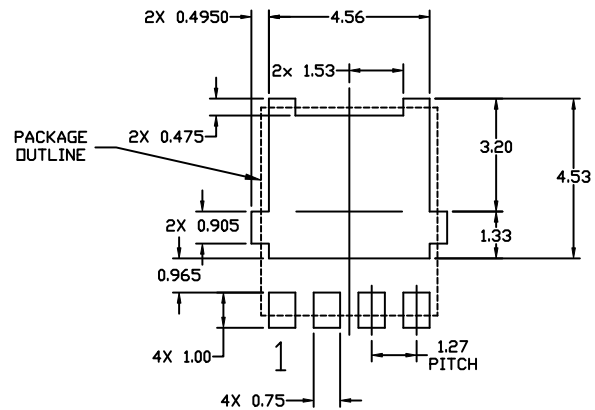
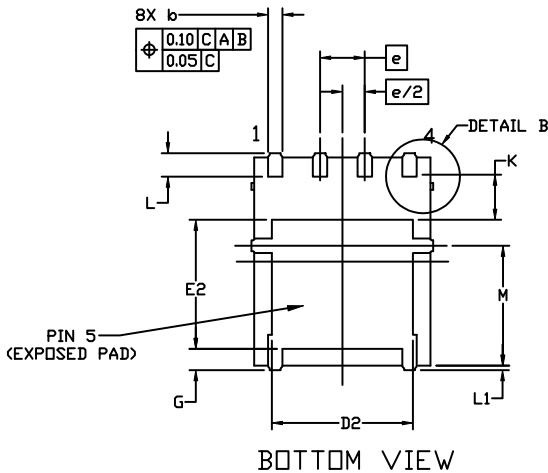
ISSUE A

DATE 03 FEB 2021

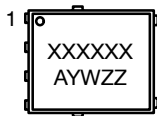


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
 2. CONTROLLING DIMENSION: MILLIMETERS
 3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
 4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
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E	6.00	6.15	6.30
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E2	3.45	3.65	3.85
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G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.150 REF		
M	3.00	3.40	3.80
θ	0°	---	12°



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- *This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

- ### RECOMMENDED MOUNTING FOOTPRINT
- * For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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