LOW EMI CLOCK GENERATOR

MK5811A

Description

The MK5811A device generates a low EMI output clock from a clock or crystal input. The device is designed to dither a high emissions clock to lower EMI in consumer applications. Using IDT's proprietary mix of analog and digital Phase Locked Loop (PLL) technology, the device spreads the frequency spectrum of the output and reduces the frequency amplitude peaks by several dB. The MK5811A offers both centered and down spread from a high-speed clock input.

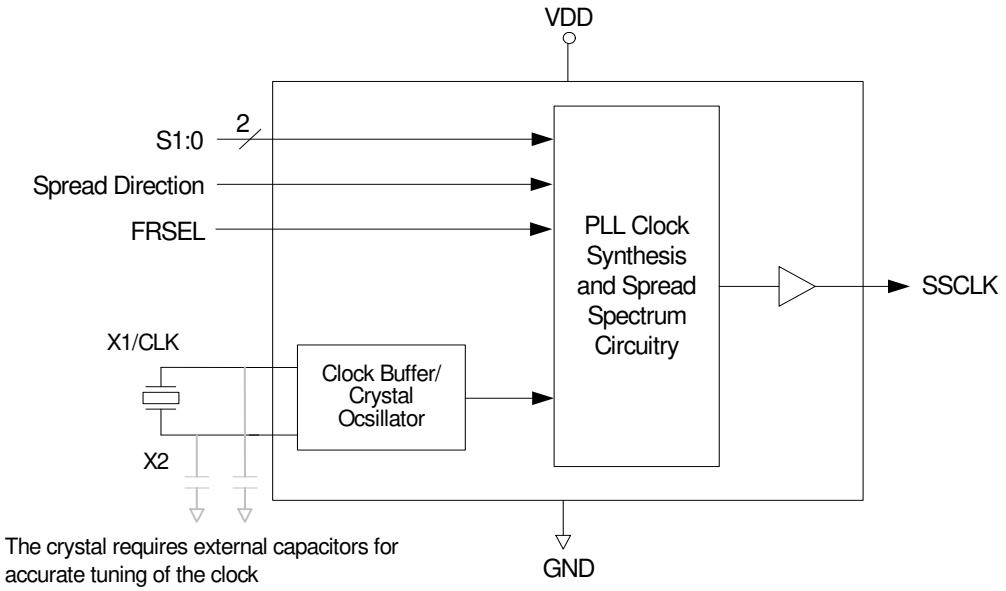
For different multiplier configurations, use the MK5812 (2x) or MK5814 (4x).

IDT offers many other clocks for computers and computer peripherals. Consult IDT when you need to remove crystals and oscillators from your board.

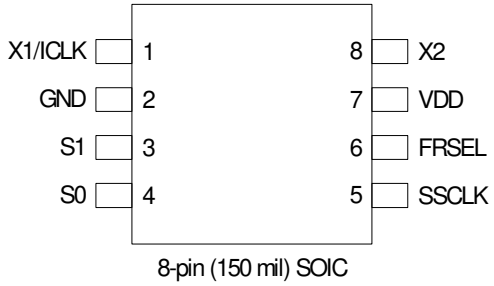
Features

- Packaged in 8-pin SOIC
- Pb (lead) free package
- Provides a spread spectrum output clock
- Supports flat panel controllers
- Accepts a clock or crystal input (provides same frequency dithered output)
- Input frequency range of 4 to 32 MHz
- Output frequency range of 4 to 32 MHz
- 1X frequency multiplication
- Center and down spread
- Peak reduction by 8 dB to 16 dB typical on 3rd through 19th odd harmonics
- Low EMI feature can be disabled
- Operating voltage of 3.3 V
- Advanced, low-power CMOS process

Block Diagram



Pin Assignment



8-pin (150 mil) SOIC

Spread Direction and Spread Percentage

S1 Pin 3	S0 Pin 4	Spread Direction	Spread Percentage
0	0	Center	±1.4
0	M	Center	±1.1
0	1	Center	±0.6
M	0	Center	±0.5
M	M	No Spread	-
M	1	Down	-1.6
1	0	Down	-2.0
1	M	Down	-0.7
1	1	Down	-3.0

0 = connect to GND
M = unconnected (floating)
1 = connect directly to VDD

Frequency Selection

Product	FRSEL (pin 6)	Input Freq. Range	Multiplier	Output Freq. Range
MK5811	0	4.0 to 8.0 MHz	X1	4.0 to 8.0 MHz
	1	8.0 to 16.0MHz	X1	8.0 to 16.0MHz
	M	16.0 to 32.0MHz	X1	16.0 to 32.0MHz
MK5812[1]	0	4.0 to 8.0 MHz	X2	8.0 to 16.0MHz
	1	8.0 to 16.0MHz	X2	16.0 to 32.0MHz
	M	16.0 to 32.0MHz	X2	32.0 to 64.0MHz
MK5814[1]	0	4.0 to 8.0 MHz	X4	16.0 to 32.0MHz
	1	8.0 to 16.0MHz	X4	32.0 to 64.0MHz
	M	16.0 to 32.0MHz	X4	64.0 to 128MHz

0 = connect to GND
M = unconnected (floating)
1 = connect directly to VDD

Note 1: The information in this datasheet does not apply to the MK5812 and MK5814 as each have independent datasheets available at www.idt.com.

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X1/ICLK	Input	Connect to 4-32 MHz crystal or clock.
2	GND	Power	Connect to ground.
3	S1	Input	Function select 1 input. Selects spread amount and direction per table above. (default-internal mid-level).
4	S0	Input	Function select 0 input. Selects spread amount and direction per table above. (default-internal mid-level).
5	SSCLK	Output	Clock output with Spread spectrum
6	FRSEL	Input	Function select for input frequency range. Default to mid level “M”.
7	VDD	Power	Connect to +3.3 V.
8	X2	XO	Crystal connection to 4-32 MHz crystal. Leave unconnected for clock

External Components

The MK5811A requires a minimum number of external components for proper operation.

Decoupling Capacitor

A decoupling capacitor of 0.01µF must be connected between VDD and GND on pins 7 and 2. Connect the capacitor as close to these pins as possible. For optimum device performance, mount the decoupling capacitor on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

Series Termination Resistor

Use series termination when the PCB trace between the clock output and the load is over 1 inch. To series terminate a 50Ω trace (a commonly used trace impedance), place a 20Ω resistor in series with the clock line. Place the resistor as close to the clock output pin as possible. The nominal impedance of the clock output is 30Ω.

Tri-level Select Pin Operation

The S1 and S0 select pins are tri-level, meaning that they have three separate states to make the selections shown in the table on page 2. To select the M (mid) level, the connection to these pins must be eliminated by either floating them originally, or tri-stating the GPIO pins which drive the select pins.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, observe the following guidelines:

1) Mount the 0.01µF decoupling capacitor on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitor and VDD pin. The PCB trace to the VDD pin and the PCB trace to the ground via should be kept as short as possible.

2) To minimize EMI, place the 20Ω series-termination resistor (if needed) close to the clock output.

3) An optimum layout is one with all components on the same side of the board, thus minimizing vias through other signal layers. Other signal traces should be routed away from the MK5811A device. This includes signal traces located underneath the device, or on layers adjacent to the ground plane layer used by the device.

Crystal Information

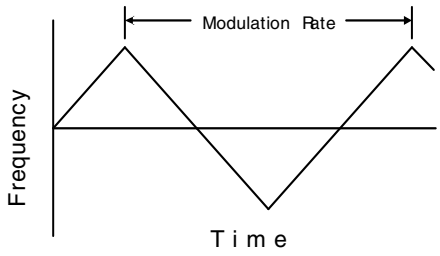
The crystal used should be a fundamental mode (do not use third overtone), parallel resonant crystal. To optimize the initial accuracy, connect crystal capacitors from pins X1 to ground and X2 to ground. The value of these capacitors is given by the following equation:

$$\text{Crystal caps (pF)} = (C_L - 6) \times 2$$

In the equation, C_L is the crystal load capacitance. For example, a crystal with a 16 pF load capacitance uses two 20 pF [(16-6) x 2] capacitors.

Spread Spectrum Profile

The MK5811A is a low EMI clock generator using a optimized frequency slew rate algorithm to facilitate down stream tracking of zero delay buffers and other PLL devices.



Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK5811A. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device, at these or any other conditions, above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +85°C
Storage Temperature	-65 to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+85	°C
Power Supply Voltage (measured in respect to GND)	+3.0		3.63	V

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±10%**, Ambient Temperature 0 to +85°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0	3.3	3.63	V
Supply Current	IDD	No load, at 3.3 V, Fin=12 MHz		23	25	mA
		No load, at 3.3 V, Fin=24 MHz			30	mA
		No load, at 3.3 V, Fin=32 MHz			35	mA
Input High Voltage	V_{IH}		0.85VDD	VDD	VDD	V
Input middle Voltage	V_{IHM}		0.4VDD	0.5VDD	0.6VDD	V
Input Low Voltage	V_{IL}		0.0	0.0	0.15VDD	V

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output High Voltage	V_{OH}	CMOS, I_{OH} = 12 mA	2.4			V
Output High Voltage	V_{OH}	I_{OH} = 24 mA	2.0			V
Output Low Voltage	V_{OL}	I_{OL} = -12 mA			0.4	V
		I_{OL} = -24 mA			1.2	V
Input Capacitance	C_{IN1}	S0, S1, FRSEL pins		4	6	pF
	C_{IN2}	X1, X2 pins		6	9	pF
Nominal Output Impedance	Z_O			30		Ω

AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±10%**, Ambient Temperature 0 to +85° C, C_L = 15 pF

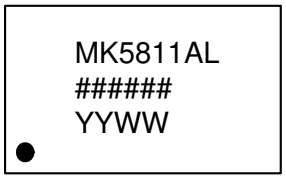
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Clock Frequency			4		32	MHz
Output Clock Frequency			4		32	MHz
Input Clock Duty Cycle		Time above VDD/2	40		60	%
Output Clock Duty Cycle		Time above 1.5 V	45	50	55	%
Cycle-to-cycle Jitter[1]		Fin=4MHz, Fout=4 MHz		350	800	ps
Cycle-to-cycle Jitter[1]		Fin=8MHz, Fout=8 MHz		250	450	ps
Output Rise Time	t_R	0.4 to 2.4 V		1.2		ns
Output Fall Time	t_F	2.4 to 0.4 V		1.2		ns
EMI Peak Frequency Reduction				8 to 16		dB

Note 1: Spread is enabled.

Thermal Characteristics for 8-pin SOIC

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		150		°C/W
	θ_{JA}	1 m/s air flow		140		°C/W
	θ_{JA}	3 m/s air flow		120		°C/W
Thermal Resistance Junction to Case	θ_{JC}			40		°C/W

Marking Diagram

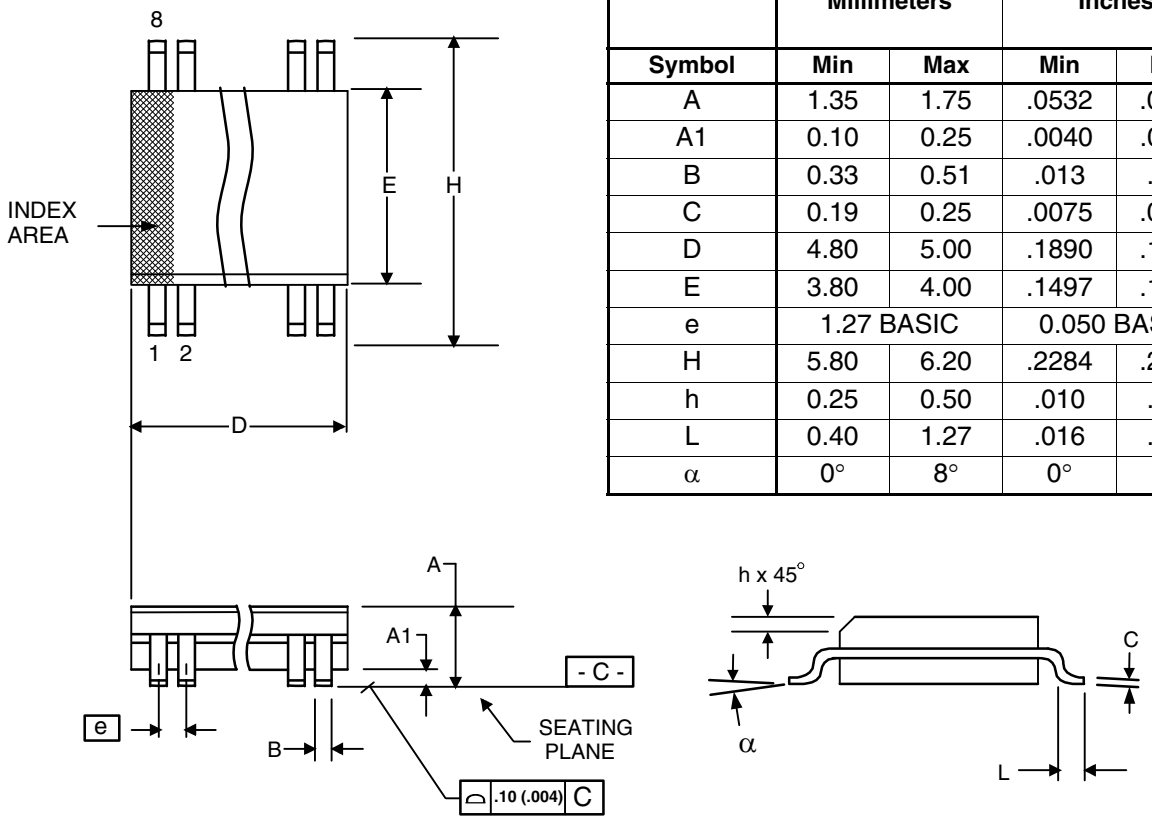


Notes:

1. “######” denotes lot number.
2. “YYWW” is the last two digits of the year and week the part was assembled.
3. “L” denotes Pb free.
4. Bottom marking: country of origin.

Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
MK5811ASLF	see page 5	Tubes	8-pin SOIC	0 to +85° C
MK5811ASLFTR		Tape and Reel	8-pin SOIC	0 to +85° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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