KAE-02152

1920 (H) x 1080 (V) Interline CCD Image Sensor

ON Semiconductor®

www.onsemi.com

The KAE−02152 image sensor is a 1080p, 2/3” format Interline Transfer EMCCD that provides increased Quantum Efficiency (particularly for NIR wavelengths) without a decrease in Modulation Transfer Function (MTF) when compared to the KAE−02150.

Each of the sensor’s four outputs includes both a conventional horizontal CCD register and a high gain EMCCD register. An intra−scene switchable gain feature samples each charge packet on a pixel−by−pixel basis, enabling the camera system to determine whether the charge will be routed through the normal gain output or the EMCCD output based on a user selectable threshold. This feature enables imaging in extreme low light even when bright objects are within a dark scene, allowing a single camera to capture quality images from sunlight to starlight. The device is available in two package configurations: PGA, and PGA with integrated thermoelectric cooler (TEC).

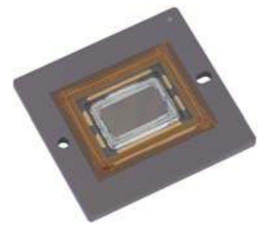


Figure 1. KAE−02152 Interline CCD Image Sensor

Table 1. GENERAL SPECIFICATIONS

Parameter	Typical Value
Architecture	Interline CCD; with EMCCD
Total Number of Pixels	1984 (H) × 1124 (V)
Number of Effective Pixels	1936 (H) × 1096 (V)
Number of Active Pixels	1920 (H) × 1080 (V)
Pixel Size	5.5 μm (H) × 5.5 μm (V)
Active Image Size	10.56 mm (H) × 5.94 mm (V) 12.1 mm (Diag.), 2/3″ Optical Format
Aspect Ratio	16:9
Number of Outputs	1, 2, or 4
Charge Capacity	20,000 e^-
Output Sensitivity	44 μV/e^-
Quantum Efficiency Peak Mono/Color (RGB) 850 nm 920 nm	 51% / 44% / 45% / 41% 16% 8%
Read Noise (20 MHz) Normal Mode (1× Gain) Intra-Scene Mode (20× Gain)	 9 e^- rms < 1 e^- rms
Dark Current (0°C) Photodiode, VCCD	 < 0.1 e^-/s, 6 e^-/s
Dynamic Range Normal Mode (1× Gain) Intra-Scene Mode (20× Gain)	 68 dB 86 dB
Charge Transfer Efficiency	0.999999
Blooming Suppression	> 1000 X
Smear	−100 dB
Image Lag	< 1 e^-
Maximum Pixel Clock Speed	40 MHz
Maximum Frame Rate Normal Mode, Intra-Scene Mode	 60 fps (40 MHz), 30 fps (20 MHz)
Package	135 pin PGA 143 pin PGA with TEC
Cover Glass	Clear Glass, Taped MAR Glass, Sealed (with TEC only)

NOTE: All Parameters are specified at T = 0°C unless otherwise noted.

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Features

- Increased QE, with 2x Improvement at 820 nm
- Intra-Scene Switchable Gain
- Wide Dynamic Range
- Low Noise Architecture
- Exceptional Low Light Imaging
- Global Shutter
- Excellent Image Uniformity and MTF
- Bayer Color Pattern and Monochrome
- PGA, or PGA with integrated TEC

Applications

- Surveillance
- Scientific Imaging
- Medical Imaging
- Intelligent Transportation

January, 2018 − Rev. 1

Publication Order Number:
KAE−02152/D

ORDERING INFORMATION

US export controls apply to all shipments of this product designated for destinations outside of the US and Canada, requiring ON Semiconductor to obtain an export license from the US Department of Commerce before image sensors or evaluation kits can be exported.

Table 2. ORDERING INFORMATION

Part Number	Description	Marking Code
KAE−02152−ABB−JP−FA	Monochrome, Microlens, PGA Package, Taped Clear Cover Glass (No Coatings), Standard Grade	KAE−02152−ABB Serial Number
KAE−02152−ABB−JP−EE	Monochrome, Microlens, PGA Package, Taped Clear Cover Glass (No Coatings), Engineering Grade	
KAE−02152−FBB−JP−FA	Gen2 Color (Bayer RGB), Microlens, PGA Package, Taped Clear Cover Glass (No Coatings), Standard Grade	KAE−02152−FBB Serial Number
KAE−02152−FBB−JP−EE	Gen2 Color (Bayer RGB), Microlens, PGA Package, Taped Clear Cover Glass (No Coatings), Engineering Grade	
KAE−02152−ABB−SD−FA	Monochrome, Microlens, PGA Package with Integrated TEC, Sealed Clear Cover Glass with AR Coating (both sides), Standard Grade	KAE−02152−ABB Serial Number
KAE−02152−ABB−SD−EE	Monochrome, Microlens, PGA Package with Integrated TEC, Sealed Clear Cover Glass with AR Coating (both sides), Engineering Grade	
KAE−02152−FBB−SD−FA	Gen2 Color (Bayer RGB), Microlens, PGA Package with Integrated TEC, Sealed Clear Cover Glass with AR Coating (both sides), Standard Grade	KAE−02152−FBB Serial Number
KAE−02152−FBB−SD−EE	Gen2 Color (Bayer RGB), Microlens, PGA Package with Integrated TEC, Sealed Clear Cover Glass with AR Coating (both sides), Engineering Grade	
KAE−02152−ABB−SP−FA	Monochrome, Microlens, PGA Package with integrated TEC, Taped Clear Cover Glass (No Coatings), Standard Grade	KAE−02152−ABB Serial Number
KAE−02152−ABB−SP−EE	Monochrome, Microlens, PGA Package with integrated TEC, Taped Clear Cover Glass (No Coatings), Engineering Grade	
KAE−02152−FBB−SP−FA	Gen2 Color (Bayer RGB), Microlens, PGA Package with integrated TEC, Taped Clear Cover Glass (No Coatings), Standard Grade	KAE−02152−FBB Serial Number
KAE−02152−FBB−SP−EE	Gen2 Color (Bayer RGB), Microlens, PGA Package with integrated TEC, Taped Clear Cover Glass (No Coatings), Engineering Grade	
KAE−02152−QBB−SD−FA	Gen2 Color (Sparse CFA), Microlens, PGA Package with integrated TEC, Sealed Clear Cover Glass with AR Coating (both sides), Standard Grade	KAE−02152−QBB Serial Number
KAE−02152−QBB−SD−EE	Gen2 Color (Sparse CFA), Microlens, PGA Package with integrated TEC, Sealed Clear Cover Glass with AR Coating (both sides), Engineering Grade	

Table 3. EVALUATION SUPPORT

Part Number	Description
G3−FPGA−BD−A−GEVK	Evaluation Board
KAE−S1−J−HEAD−BD−A−GEVK	PGA Package Head Board
KAE−S1−S−HEAD−BD−A−GEVK	PGA Package with Integrated TEC Head Board
LENS−MOUNT−KIT−D−GEVK	Lens Mount Kit for IT−CCD Evaluation Hardware
KAE−02152−AB−SD−A−GEVK	Full Evaluation Kit. Includes Image Sensor KAE−02152−ABB−SD−FA
KAE−02152−FB−SD−A−GEVK	Full Evaluation Kit. Includes Image Sensor KAE−02152−FBB−SD−FA
KAE−02152−QB−SD−A−GEVK	Full Evaluation Kit. Includes Image Sensor KAE−02152−QBB−SD−FA

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

Warning

The KAE−02152−ABB−SD, KAE−02152−FBB−SD and KAE−02152−QBB−SD packages have an integrated thermoelectric cooler (TEC) and have epoxy sealed cover glass. The seal formed is non−hermetic, and may allow moisture ingress over time, depending on the storage environment.

As a result, care must be taken to avoid cooling the device below the dew point inside the package cavity, since this may result in condensation on the sensor.

For all KAE−02152 configurations, no warranty, expressed or implied, covers condensation.

DEVICE DESCRIPTION

Architecture

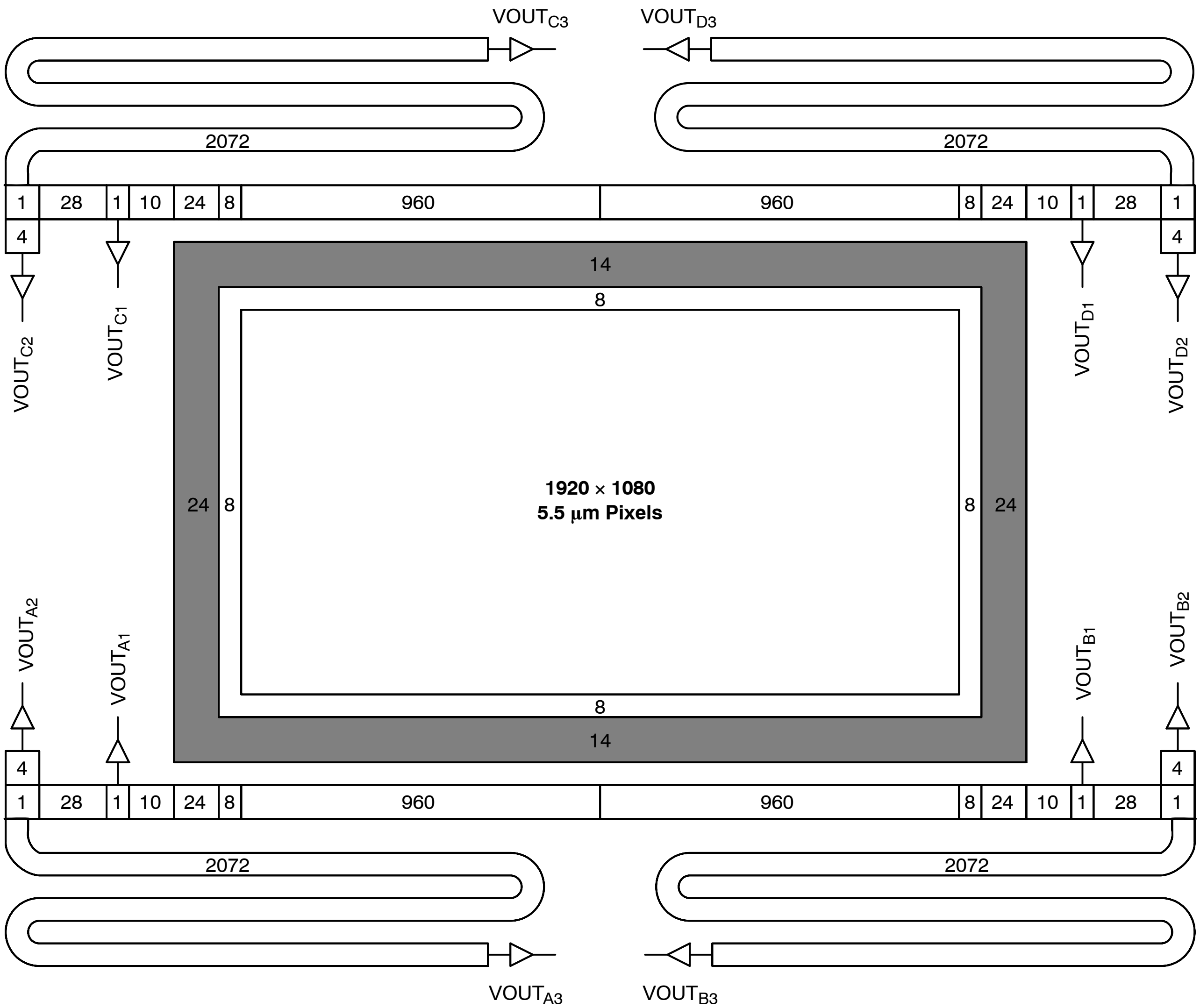


Figure 2. Block Diagram

Dark Reference Pixels

There are 14 dark reference rows at the top and bottom of the image sensor, as well as 24 dark reference columns on the left and right sides. However, the rows and columns at the very edges should not be included in acquiring a dark reference signal, since they may be subject to some light leakage.

Active Buffer Pixels

8 unshielded pixels adjacent to any leading or trailing dark reference regions are classified as active buffer pixels. These pixels are light sensitive but are not tested for defects and non-uniformities.

Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the individual silicon photodiodes. These photoelectrons are collected locally by the formation of potential wells at each photo-site. Below photodiode saturation, the number of photoelectrons collected at each pixel is linearly dependent upon light level and exposure time and non-linearly dependent on wavelength. When the photodiodes charge capacity is reached, excess electrons are discharged into the substrate to prevent blooming

ESD Protection

Adherence to the power-up and power-down sequence is critical. Failure to follow the proper power-up and power-down sequences may cause damage to the sensor. See Power-Up and Power-Down Sequence section.

Bayer Color Filter Pattern

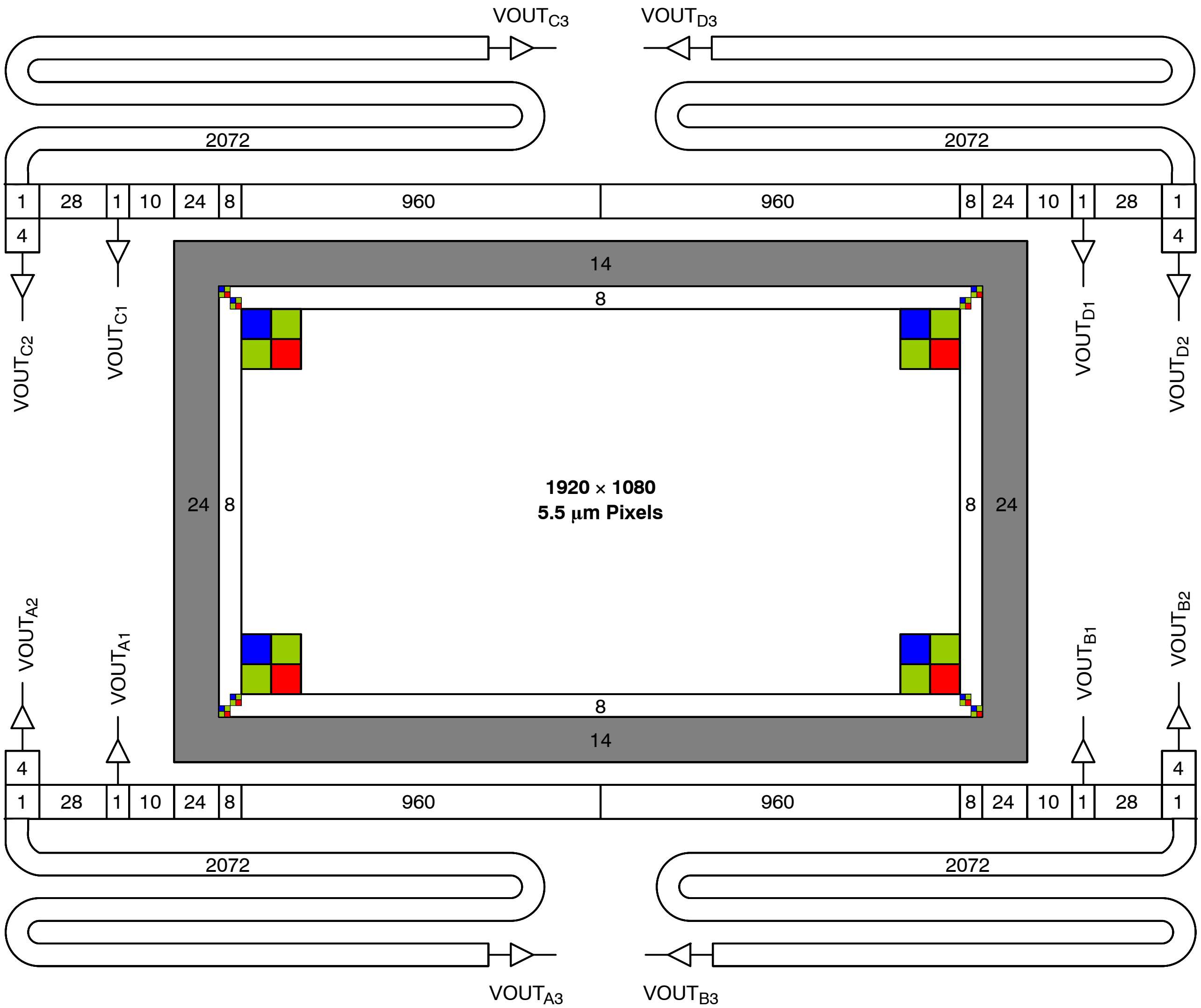


Figure 3. Bayer Color Filter Pattern

Sparse Color Filter Pattern

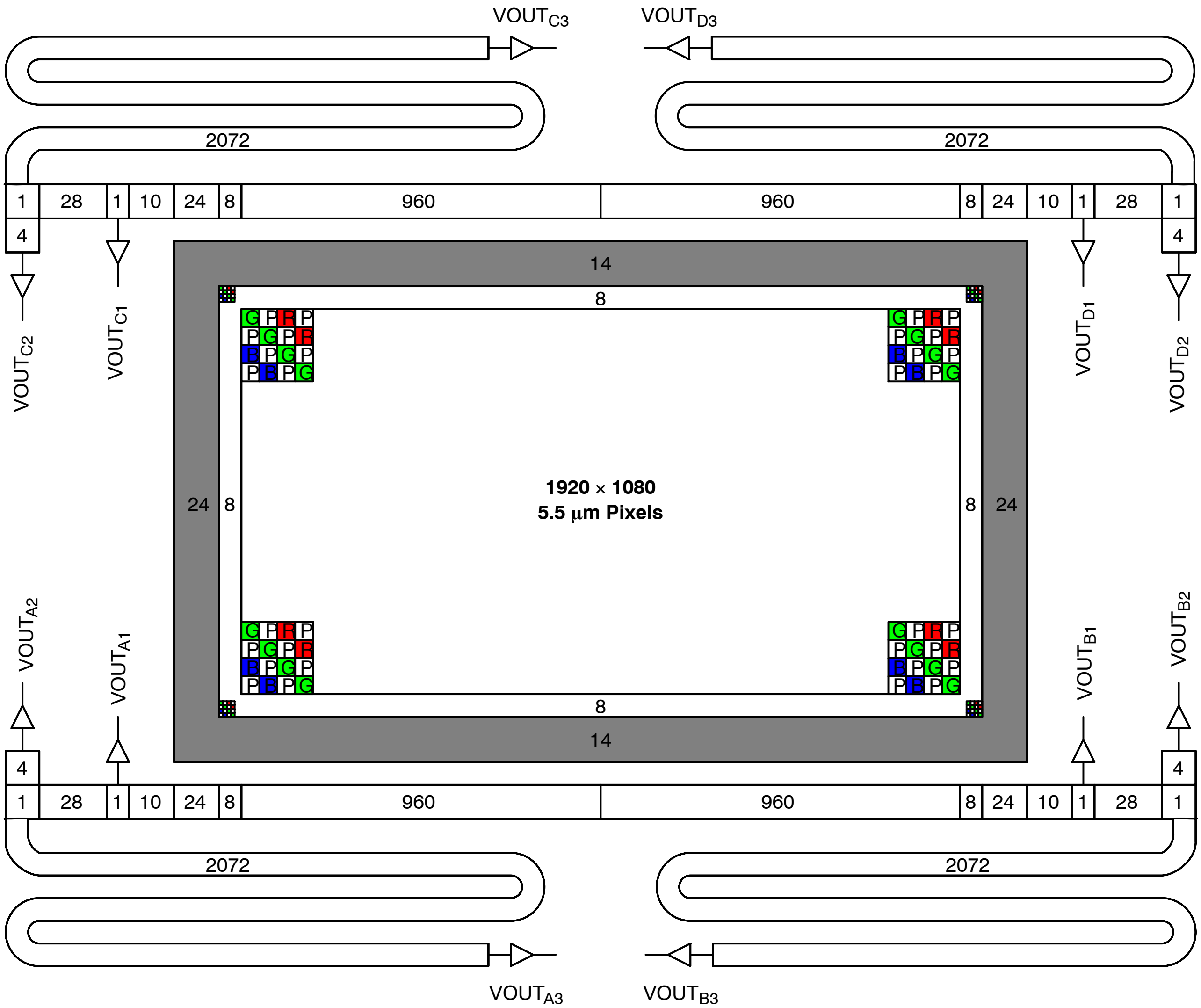


Figure 4. Sparse Color Filter Pattern

Physical Description

Pin Grid Array and Pin Description

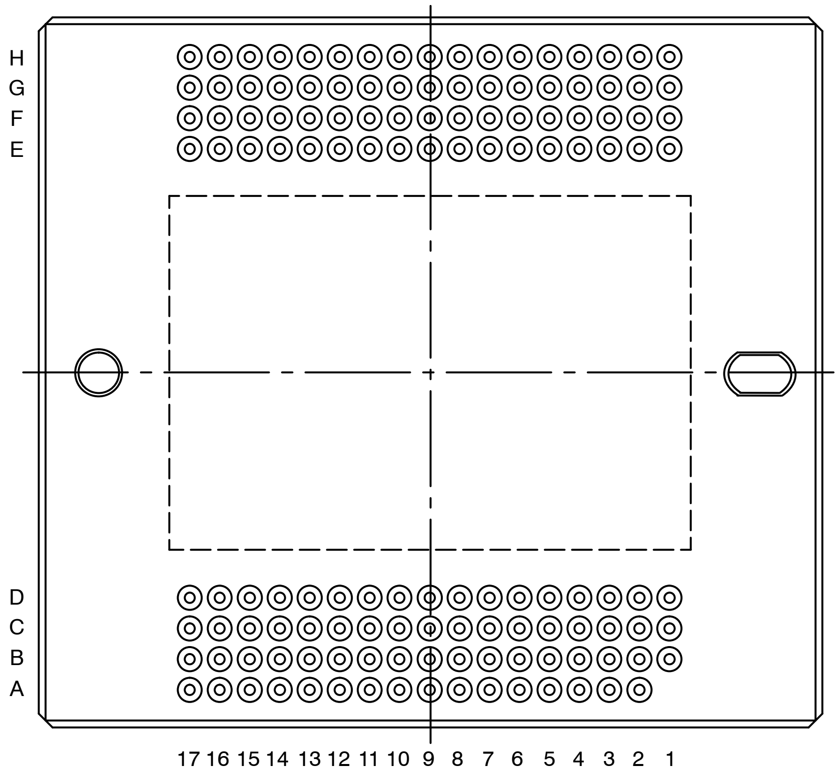


Figure 5. PGA Package Designations (Bottom View)

Table 4. PIN DESCRIPTION

Pin	Label	Description
A02	V3B	VCCD Bottom Phase 3
A03	N/C	No Connection
A04	RG2a	Amplifier 2 Reset, Quadrant A
A05	N/C	No Connection
A06	VDD23ab	Amplifier 2 and 3 Supply, Quadrants A, B
A07	H1BEMa	EMCCD Barrier Phase 1, Quadrant A
A08	H2Ba	HCCD Barrier Phase 2, Quadrant A
A09	GND	Ground
A10	H2Bb	HCCD Barrier Phase 2, Quadrant B
A11	H1BEMb	EMCCD barrier phase 1, Quadrant B
A12	VDD23ab	Amplifier 2 and 3 Supply, Quadrants A, B
A13	N/C	No Connection
A14	RG2a	Amplifier 2 Reset, Quadrant B
A15	N/C	No Connection
A16	V3B	VCCD Bottom Phase 3
A17	ESD	ESD Protection Disable
B01	DEVID	Device ID Resistor
B02	V4B	VCCD Bottom Phase 4
B03	VOUT1a	Amplifier 1 Output, Quadrant A

Table 4. PIN DESCRIPTION (continued)

Pin	Label	Description
B04	VOUT2a	Video Output 2, Quadrant A
B05	H2SW3a	HCCD Output 3 Selector, Quadrant A
B06	VOUT3a	Video Output 3, Quadrant A
B07	H2BEMa	EMCCD Barrier Phase 2, Quadrant A
B08	H1Ba	HCCD Barrier Phase 1, Quadrant A
B09	GND	Ground
B10	H1Bb	HCCD Barrier Phase 1, Quadrant B
B11	H2BEMb	EMCCD Barrier Phase 2, Quadrant B
B12	VOUT3b	Video Output 3, Quadrant B
B13	H2SW3b	HCCD Output 3 Selector, Quadrant B
B14	VOUT2b	Video Output 2, Quadrant B
B15	VOUT1b	Amplifier 1 Output, Quadrant B
B16	V4B	VCCD Bottom Phase 4
B17	SUB	Substrate
C01	V1B	VCCD Bottom Phase 1
C02	N/C	No Connection
C03	VSS1a	Amplifier 1 Return, Quadrant A
C04	VDD23ab	Amplifier 2 and 3 Supply, Quadrants A, B
C05	H2SW2a	HCCD Output 2 Selector, Quadrant A
C06	N/C	No Connection
C07	H1SEMa	EMCCD Storage Multiplier Phase 1, Quadrant A
C08	H2Sa	HCCD Storage Phase 2, Quadrant A
C09	GND	Ground
C10	H2Sb	HCCD Storage Phase 2, Quadrant B
C11	H1SEMb	EMCCD Storage Multiplier Phase 1, Quadrant B
C12	N/C	No Connection
C13	H2SW2b	HCCD Output 2 Selector, Quadrant B
C14	VDD23ab	Amplifier 2 and 3 Supply, Quadrants A, B
C15	VSS1b	Amplifier 1 Return, Quadrant B
C16	N/C	No Connection
C17	V1B	VCCD Bottom Phase 1
D01	V2B	VCCD Bottom Phase 2
D02	VDD1a	Amplifier 1 Supply, Quadrant A
D03	RG1a	Amplifier 1 Reset, Quadrant A
D04	H2Xa	Floating Gate Exit HCCD Gate, Quadrant A
D05	H2La	HCCD Last Gate, Outputs 1, 2 and 3, Quadrant A
D06	RG3a	Amplifier 3 Reset, Quadrant A
D07	H2SEMa	EMCCD Storage Multiplier Phase 2, Quadrant A
D08	H1Sa	HCCD Storage Phase 1, Quadrant A
D09	GND	Ground
D10	H1Sb	HCCD Storage Phase 1, Quadrant B
D11	H2SEMb	EMCCD Storage Multiplier Phase 2, Quadrant B
D12	RG3b	Amplifier 3 Reset, Quadrant B
D13	H2Lb	HCCD Last Gate, Outputs 1, 2 and 3, Quadrant B
D14	H2Xb	Floating Gate Exit HCCD Gate, Quadrant B

Table 4. PIN DESCRIPTION (continued)

Pin	Label	Description
D15	RG1b	Amplifier 1 Reset, Quadrant B
D16	VDD1b	Amplifier 1 Supply, Quadrant B
D17	V2B	VCCD Bottom Phase 2
E01	V2T	VCCD Top Phase 2
E02	VDD1c	Amplifier 1 Supply, Quadrant C
E03	RG1c	Amplifier 1 Reset, Quadrant C
E04	H2Xc	Floating Gate Exit HCCD Gate, Quadrant C
E05	H2Lc	HCCD Last Gate, Outputs 1, 2 and 3, Quadrant C
E06	RG3c	Amplifier 3 Reset, Quadrant C
E07	H2SEMc	EMCCD Storage Multiplier Phase 2, Quadrant C
E08	H1Sc	HCCD Storage Phase 1, Quadrant C
E09	GND	Ground
E10	H1Sd	HCCD Storage Phase 1, Quadrant D
E11	H2SEMd	EMCCD Storage Multiplier Phase 2, Quadrant D
E12	RG3d	Amplifier 3 Reset, Quadrant D
E13	H2Ld	HCCD Last Gate, Outputs 1, 2 and 3, Quadrant D
E14	H2Xd	Floating Gate Exit HCCD Gate, Quadrant D
E15	RG1d	Amplifier 1 Reset, Quadrant D
E16	VDD1d	Amplifier 1 Supply, Quadrant D
E17	V2T	VCCD Top Phase 2
F01	V1T	VCCD Top Phase 1
F02	N/C	No Connection
F03	VSS1c	Amplifier 1 Return, Quadrant C
F04	VDD23cd	Amplifier 2 and 3 Supply, Quadrants C, D
F05	H2SW2c	HCCD Output 2 Selector, Quadrant C
F06	N/C	No Connection
F07	H1SEMc	EMCCD Storage Multiplier Phase 1, Quadrant C
F08	H2Sc	HCCD Storage Phase 2, Quadrant C
F09	GND	Ground
F10	H2Sd	HCCD Storage Phase 2, Quadrant D
F11	H1SEMd	EMCCD Storage Multiplier Phase 1, Quadrant D
F12	N/C	No Connection
F13	H2SW2d	HCCD Output 2 Selector, Quadrant D
F14	VDD23cd	Amplifier 2 and 3 Supply, Quadrants C, D
F15	VSS1d	Amplifier 1 Return, Quadrant D
F16	N/C	No Connection
F17	V1T	VCCD Top Phase 1
G01	ESD	ESD Protection Disable
G02	V4T	VCCD Top Phase 4
G03	VOUT1c	Amplifier 1 Output, Quadrant C
G04	VOUT2c	Video Output 2, Quadrant C
G05	H2SW3c	HCCD Output 3 Selector, Quadrant C
G06	VOUT3c	Video Output 3, Quadrant C
G07	H2BEMc	EMCCD Barrier Phase 2, Quadrant C
G08	H1Bc	HCCD Barrier Phase 1, Quadrant C

Table 4. PIN DESCRIPTION (continued)

Pin	Label	Description
G09	GND	Ground
G10	H1Bd	HCCD Barrier Phase 1, Quadrant D
G11	H2BEMd	EMCCD Barrier Phase 2, Quadrant D
G12	VOUT3d	Video Output 3, Quadrant D
G13	H2SW3d	HCCD Output 3 Selector, Quadrant D
G14	VOUT2d	Video Output 2, Quadrant D
G15	VOUT1d	Amplifier 1 Output, Quadrant D
G16	V4T	VCCD Top Phase 4
G17	SUB	Substrate
H01	GND	Ground
H02	V3T	VCCD Top Phase 3
H03	N/C	No Connection
H04	RG2c	Amplifier 2 Reset, Quadrant C
H05	N/C	No Connection
H06	VDD23cd	Amplifier 2 and 3 Supply, Quadrants C, D
H07	H1BEMc	EMCCD Barrier Phase 1, Quadrant C
H08	H2Bc	HCCD Barrier Phase 2, Quadrant C
H09	GND	Ground
H10	H2Bd	HCCD Barrier Phase 2, Quadrant D
H11	H1BEMd	EMCCD Barrier Phase 1, Quadrant D
H12	VDD23cd	Amplifier 2 and 3 Supply, Quadrants C, D
H13	N/C	No Connection
H14	RG2d	Amplifier 2 Reset, Quadrant D
H15	N/C	No Connection
H16	V3T	VCCD Top Phase 3
H17	SUBREF	Substrate Voltage Reference

PGA with Integrated TEC Pin Description and Device Orientation

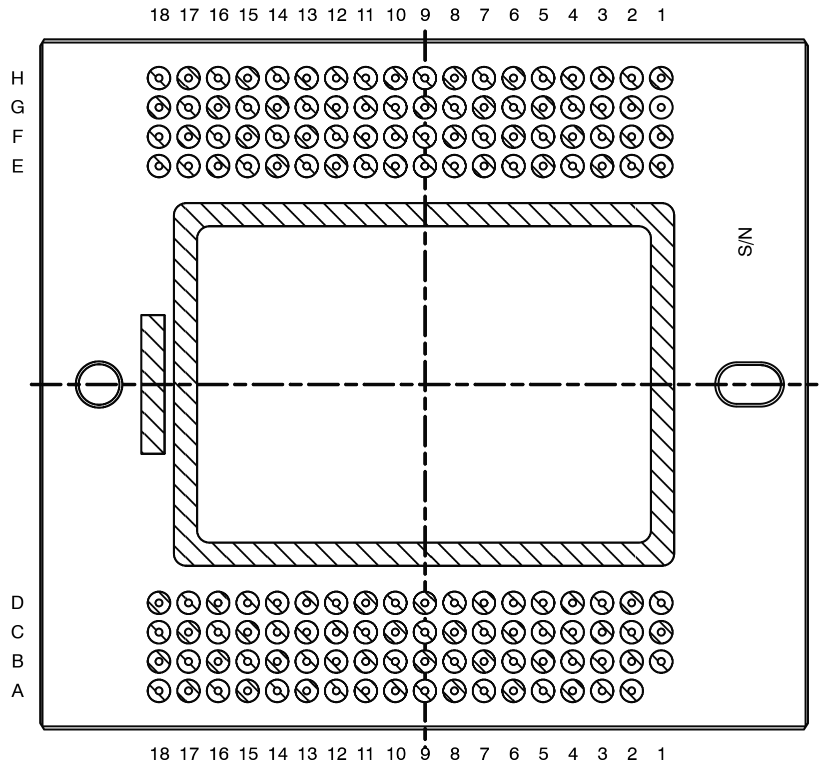


Figure 6. PGA with TEC Pin Descriptions − Bottom View

Table 5. PGA WITH INTEGRATED TEC PIN DESCRIPTION

Pin	Label	Description
A02	V3B	VCCD Bottom Phase 3
A03	NTC1	Negative Temperature Coefficient Thermistor Terminal 1
A04	RG2a	Amplifier 2 Reset, Quadrant A
A05	NTC2	Negative Temperature Coefficient Thermistor Terminal 2
A06	VDD23ab	Amplifier 2 And 3 Supply, Quadrants A, B
A07	H1BEMa	EMCCD Barrier Phase 1, Quadrant A
A08	H2Ba	HCCD Barrier Phase 2, Quadrant A
A09	GND	Ground
A10	H2Bb	HCCD Barrier Phase 2, Quadrant B
A11	H1BEMb	EMCCD Barrier Phase 1, Quadrant B
A12	VDD23ab	Amplifier 2 And 3 Supply, Quadrants A, B
A13	N/C	No Connect
A14	RG2b	Amplifier 2 Reset, Quadrant B
A15	N/C	No Connection
A16	V3B	VCCD Bottom Phase 3
A17	ESD	ESD Protection Disable
A18	TEC−	Thermal Electric Cooler Negative Terminal
B01	DEVID	Device ID Resistor
B02	V4B	VCCD Bottom Phase 4

Table 5. PGA WITH INTEGRATED TEC PIN DESCRIPTION (continued)

Pin	Label	Description
B03	VOUT1a	Amplifier 1 Output, Quadrant A
B04	VOUT2a	Video Output 2, Quadrant A
B05	H2SW3a	HCCD Output 3 Selector, Quadrant A
B06	VOUT3a	Video Output 3, Quadrant A
B07	H2BEMa	EMCCD Barrier Phase 2, Quadrant A
B08	H1Ba	HCCD Barrier Phase 1, Quadrant A
B09	GND	Ground
B10	H1Bb	HCCD Barrier Phase 1, Quadrant B
B11	H2BEMb	EMCCD Barrier Phase 2, Quadrant B
B12	VOUT3b	Video Output 3, Quadrant B
B13	H2SW3b	HCCD Output 3 Selector, Quadrant B
B14	VOUT2b	Video Output 2, Quadrant B
B15	VOUT1b	Amplifier 1 Output, Quadrant B
B16	V4B	VCCD Bottom Phase 4
B17	SUB	Substrate
B18	TEC−	Thermal Electric Cooler Negative Terminal
C01	V1B	VCCD Bottom Phase 1
C02	N/C	No Connection
C03	VSS1a	Amplifier 1 Return, Quadrant A
C04	VDD23ab	Amplifier 2 And 3 Supply, Quadrants A, B
C05	H2SW2a	HCCD Output 2 Selector, Quadrant A
C06	N/C	No Connection
C07	H1SEMa	EMCCD Storage Multiplier Phase 1, Quadrant A
C08	H2Sa	HCCD Storage Phase 2, Quadrant A
C09	GND	Ground
C10	H2Sb	HCCD Storage Phase 2, Quadrant B
C11	H1SEMb	EMCCD Storage Multiplier Phase 1, Quadrant B
C12	N/C	No Connection
C13	H2SW2b	HCCD Output 2 Selector, Quadrant B
C14	VDD23ab	Amplifier 2 And 3 Supply, Quadrants A, B
C15	VSS1b	Amplifier 1 Return, Quadrant B
C16	N/C	No Connection
C17	V1B	VCCD Bottom Phase 1
C18	TEC−	Thermal Electric Cooler Negative Terminal
D01	V2B	VCCD Bottom Phase 2
D02	VDD1a	Amplifier 1 Supply, Quadrant A
D03	RG1a	Amplifier 1 Reset, Quadrant A
D04	H2Xa	Floating Gate Exit HCCD Gate, Quadrant A
D05	H2La	HCCD Last Gate, Outputs 1,2 And 3, Quadrant A
D06	RG3a	Amplifier 3 Reset, Quadrant A
D07	H2SEMa	EMCCD Storage Multiplier Phase 2, Quadrant A
D08	H1Sa	HCCD Storage Phase 1, Quadrant A

Table 5. PGA WITH INTEGRATED TEC PIN DESCRIPTION (continued)

Pin	Label	Description
D09	GND	Ground
D10	H1Sb	HCCD Storage Phase 1, Quadrant B
D11	H2SEMb	EMCCD Storage Multiplier Phase 2, Quadrant B
D12	RG3b	Amplifier 3 Reset, Quadrant B
D13	H2Lb	HCCD Last Gate, Outputs 1,2 And 3, Quadrant B
D14	H2Xb	Floating Gate Exit HCCD Gate, Quadrant B
D15	RG1b	Amplifier 1 Reset, Quadrant B
D16	VDD1b	Amplifier 1 Supply, Quadrant B
D17	V2B	VCCD Bottom Phase 2
D18	TEC−	Thermal Electric Cooler Negative Terminal
E01	V2T	VCCD Top Phase 2
E02	VDD1c	Amplifier 1 Supply, Quadrant C
E03	RG1c	Amplifier 1 Reset, Quadrant C
E04	H2Xc	Floating Gate Exit HCCD Gate, Quadrant C
E05	H2Lc	HCCD Last Gate, Outputs 1,2 And 3, Quadrant C
E06	RG3c	Amplifier 3 Reset, Quadrant C
E07	H2SEMc	EMCCD Storage Multiplier Phase 2, Quadrant C
E08	H1Sc	HCCD Storage Phase 1, Quadrant C
E09	GND	Ground
E10	H1Sd	HCCD Storage Phase 1, Quadrant D
E11	H2SEMd	EMCCD Storage Multiplier Phase 2, Quadrant D
E12	RG3d	Amplifier 3 Reset, Quadrant B
E13	H2Ld	HCCD Last Gate, Outputs 1,2 And 3, Quadrant D
E14	H2Xd	Floating Gate Exit HCCD Gate, Quadrant D
E15	RG1d	Amplifier 1 Reset, Quadrant D
E16	VDD1d	Amplifier 1 Supply, Quadrant D
E17	V2T	VCCD Top Phase 2
E18	TEC+	Thermal Electric Cooler Positive Terminal
F01	V1T	VCCD Top Phase 1
F02	N/C	No Connection
F03	VSS1c	Amplifier 1 Return, Quadrant C
F04	VDD23cd	Amplifier 2 And 3 Supply, Quadrants C, D
F05	H2SW2c	HCCD Output 2 Selector, Quadrant C
F06	N/C	No Connection
F07	H1SEMc	EMCCD Storage Multiplier Phase 1, Quadrant C
F08	H2Sc	HCCD Storage Phase 2, Quadrant C
F09	GND	Ground
F10	H2Sd	HCCD Storage Phase 2, Quadrant D
F11	H1SEMd	EMCCD Storage Multiplier Phase 1, Quadrant D
F12	N/C	No Connection
F13	H2SW2d	HCCD Output 2 Selector, Quadrant D
F14	VDD23cd	Amplifier 2 And 3 Supply, Quadrants C, D

Table 5. PGA WITH INTEGRATED TEC PIN DESCRIPTION (continued)

Pin	Label	Description
F15	VSS1d	Amplifier 1 Return, Quadrant D
F16	N/C	No Connection
F17	V1T	VCCD Top Phase 1
F18	TEC+	Thermal Electric Cooler Positive Terminal
G01	ESD	ESD Protection Disable
G02	V4T	VCCD Top Phase 4
G03	VOUT1c	Amplifier 1 Output, Quadrant C
G04	VOUT2c	Video Output 2, Quadrant C
G05	H2SW3c	HCCD Output 3 Selector, Quadrant C
G06	VOUT3c	Video Output 3, Quadrant C
G07	H2BEMc	EMCCD Barrier Phase 2, Quadrant C
G08	H1Bc	HCCD Barrier Phase 1, Quadrant C
G09	GND	Ground
G10	H1Bd	HCCD Barrier Phase 1, Quadrant D
G11	H2BEMd	EMCCD Barrier Phase 2, Quadrant D
G12	VOUT3d	Video Output 3, Quadrant B
G13	H2SW3d	HCCD Output 3 Selector, Quadrant D
G14	VOUT2d	Video Output 2, Quadrant D
G15	VOUT1d	Amplifier 1 Output, Quadrant D
G16	V4T	VCCD Top Phase 4
G17	SUB	Substrate
G18	TEC+	Thermal Electric Cooler Positive Terminal
H01	GND	Ground
H02	V3T	VCCD Top Phase 3
H03	N/C	No Connection
H04	RG2c	Amplifier 2 Reset, Quadrant C
H05	N/C	No Connection
H06	VDD23cd	Amplifier 2 And 3 Supply, Quadrants C, D
H07	H1BEMc	EMCCD Barrier Phase 1, Quadrant C
H08	H2Bc	HCCD Barrier Phase 2, Quadrant C
H09	GND	Ground
H10	H2Bd	HCCD Barrier Phase 2, Quadrant D
H11	H1BEMd	EMCCD Barrier Phase 1, Quadrant D
H12	VDD23cd	Amplifier 2 And 3 Supply, Quadrants C, D
H13	N/C	No Connection
H14	RG2d	Amplifier 2 Reset, Quadrant D
H15	N/C	No Connection
H16	V3T	VCCD Top Phase 3
H17	SUBREF	Substrate Voltage Reference
H18	TEC+	Thermal Electric Cooler Positive Terminal

1. Pins A03 and A05 are connected to a negative temperature coefficient thermistor
2. All TEC pins (A18, B18, C18, D18, E18, F18, G18, and H18) must be driven.

IMAGING PERFORMANCE

Table 6. TYPICAL OPERATIONAL CONDITIONS

(Unless otherwise noted, the Imaging Performance Specifications are measured using the following conditions.)

Description	Condition	Notes
Light Source	Continuous Red, Green and Blue LED Illumination	1
Operation	Nominal Operating Voltages and Timing	
Temperature	0°C	

1. For monochrome sensor, only green LED used.

Table 7. SPECIFICATIONS

Description	Symbol	Min.	Nom.	Max.	Units	Sampling Plan	Temperature Tested at (°C)	Notes
Dark Field Global Non-Uniformity	DSNU	–	–	2.0	mV pp	Die	0	
Bright Field Global Non-Uniformity		–	2.0	5.0	% rms	Die	0	1
Bright Field Global Peak to Peak Non-Uniformity	PRNU	–	5.0	15.0	% pp	Die	0	1
Bright Field Center Non-Uniformity		–	1.0	2.0	% rms	Die	0	1
Maximum Photoresponse Nonlinearity (EMCCD Gain = 1)	NL	–	2	–	%	Design		2
Maximum Gain Difference Between Outputs (EMCCD Gain = 1)	ΔG	–	10	–	%	Design		2
Maximum Signal Error due to Nonlinearity Differences (EMCCD Gain = 1)	ΔNL	–	1	–	%	Design		2
Horizontal CCD Charge Capacity	H_{Ne}	–	30	–	ke^-	Design		
Vertical CCD Charge Capacity	V_{Ne}	–	30	–	ke^-	Design		
Photodiode Charge Capacity	P_{Ne}	–	20	–	ke^-	Die	0	3
Horizontal CCD Charge Transfer Efficiency	HCTE	0.999995	0.999999	–		Die	0	
Vertical CCD Charge Transfer Efficiency	VCTE	0.999995	0.999999	–		Die	0	
Photodiode Dark Current (Average)	I_{PD}	–	0.1	3	e^-/p/s	Design	0	
Vertical CCD Dark Current	I_{VD}	–	6	–	e^-/p/s	Design	0	
Image Lag	Lag	–	–	< 1	e^-	Design		
Antiblooming Factor	X_{AB}	1,000	–	–		Design		
Vertical Smear (blue light)	Smr	–	−100	–	dB	Design		
Read Noise (EMCCD Gain = 1)	n_{e^-T}	–	9	–	e^- rms	Design		4
Read Noise (EMCCD Gain = 20)		–	< 1	–	e^- rms	Die	0	
EMCCD Excess Noise Factor (Gain = 20x)		–	1.4	–		Design	0	

Table 7. SPECIFICATIONS (continued)

Description	Symbol	Min.	Nom.	Max.	Units	Sampling Plan	Temperature Tested at (°C)	Notes
Dynamic Range (ECCD Gain = 1)	DR	–	68	–	dB	Design		4, 5
Dynamic Range (High Gain)		–	60	–	dB	Design		
Dynamic Range (Intra-Scene)		–	86	–	dB	Design		
Output Amplifier DC Offset (VOUT2, VOUT3)	V_{ODC}	8.0	10	12.0	V	Die	0	
Output Amplifier DC Offset (VOUT1)	V_{ODC}	−0.5	1	2.5	V	Die	0	
Output Amplifier Bandwidth	f_{-3dB}	–	250	–	MHz	Die	0	6
Output Amplifier Impedance	R_{OUT}	–	140	–	Ω	Die	0	
Output Amplifier Sensitivity (Normal output)	ΔV/ΔN	–	44	–	μV/e⁻	Design		
Output Amplifier Sensitivity (Floating Gate Amplifier)	ΔV/ΔN (FG)	–	6.2	–	μV/e⁻	Design		
Quantum Efficiency (Peak) Monochrome Red Green Blue 850 nm 920 nm	QE_{MAX}	 – – – –	 51 44 45 41 16 8	 – – – – –	%	Design		
Power 4-Output Mode (20MHz) (40MHz) 2-Output Mode (20MHz) (40MHz) 1-Output Mode (20MHz) (40MHz)		 – – – – – –	 0.7 0.8 0.5 0.5 0.4 0.4	 – – – – – –	W	Design		

1. Per color
2. Value is over the range of 10% to 90% of photodiode saturation.
3. The operating value of the substrate reference voltage, V_{AB}, can be read from pin 60.
4. At 40 MHz.
5. Uses 20LOG (P_{Ne} / n_{e-T}).
6. Calculated from $f_{-3dB} = 1 / 2\pi \cdot R_{OUT} \cdot C_{LOAD}$ where C_{LOAD} = 5 pF.

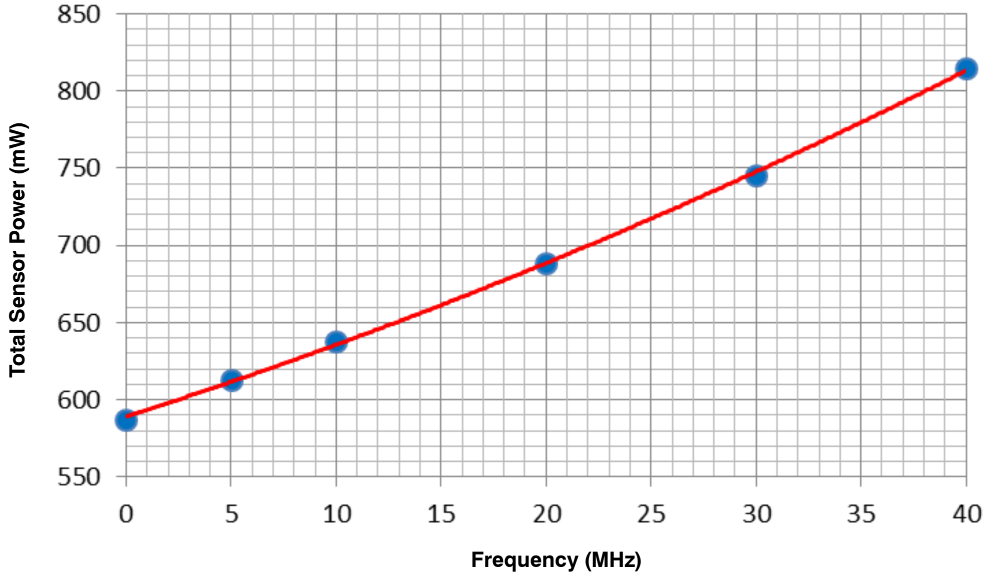


Figure 7. Total Power Dissipated on the Sensor vs. Frequency

TYPICAL PERFORMANCE CURVES

Quantum Efficiency

Monochrome with Microlens

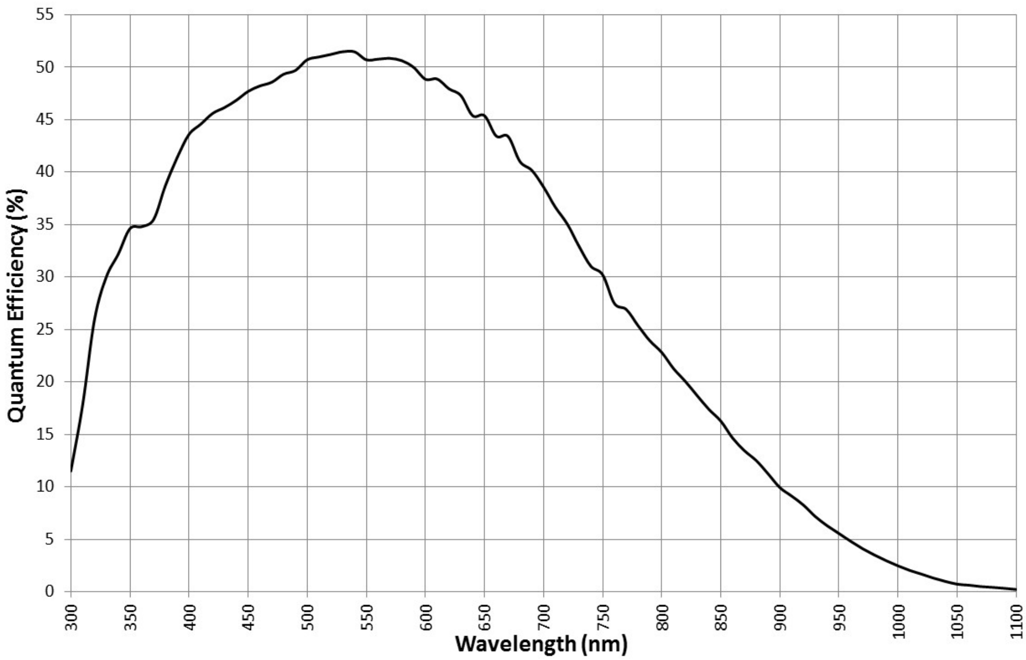


Figure 8. Monochrome QE with Microlens and No Glass

Figure 9. Monochrome QE with Microlens and MAR Glass

Color (Bayer RGB) with Microlens

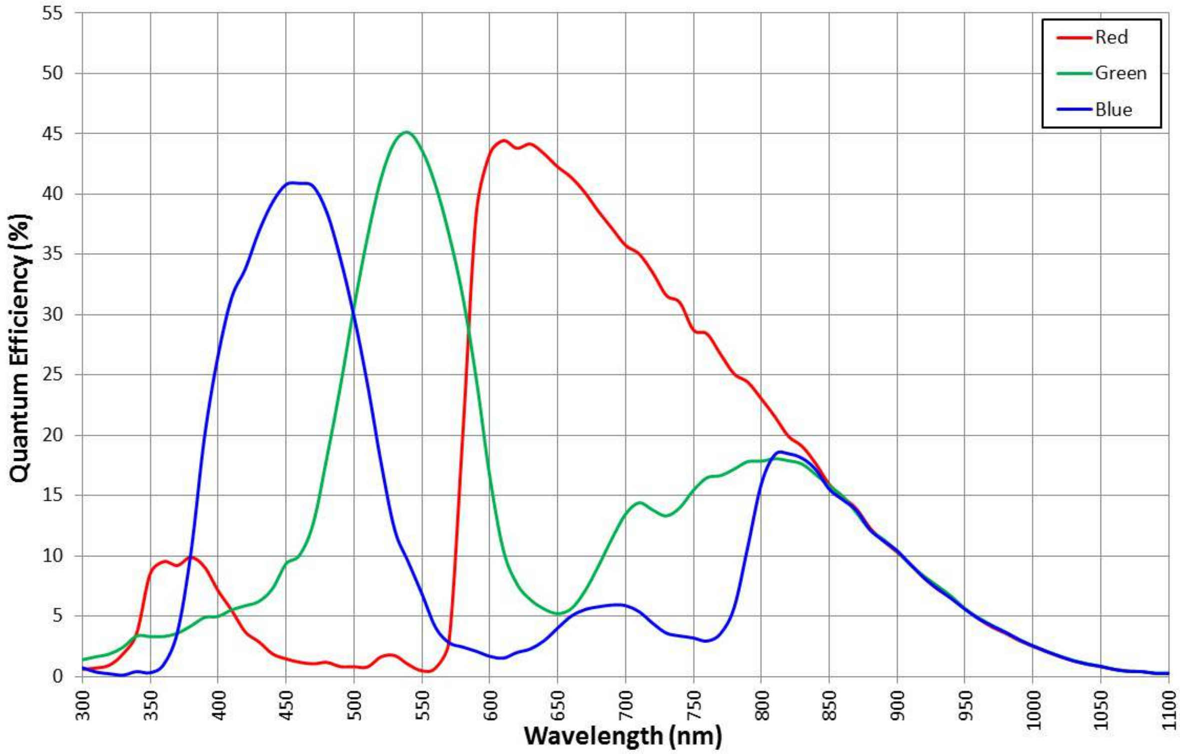


Figure 10. Color (Bayer RGB) QE with Microlens and No Glass

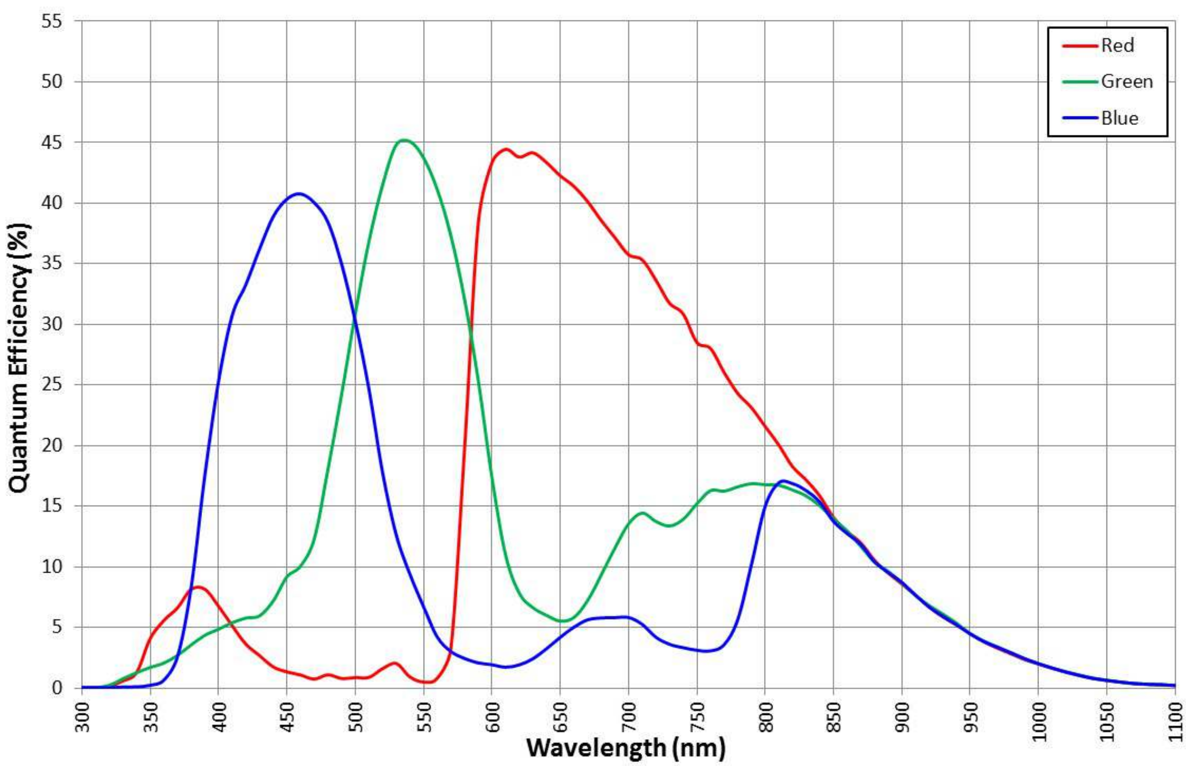


Figure 11. Color (Bayer RGB) QE with Microlens and MAR Glass

Color (Sparse CFA) with Microlens

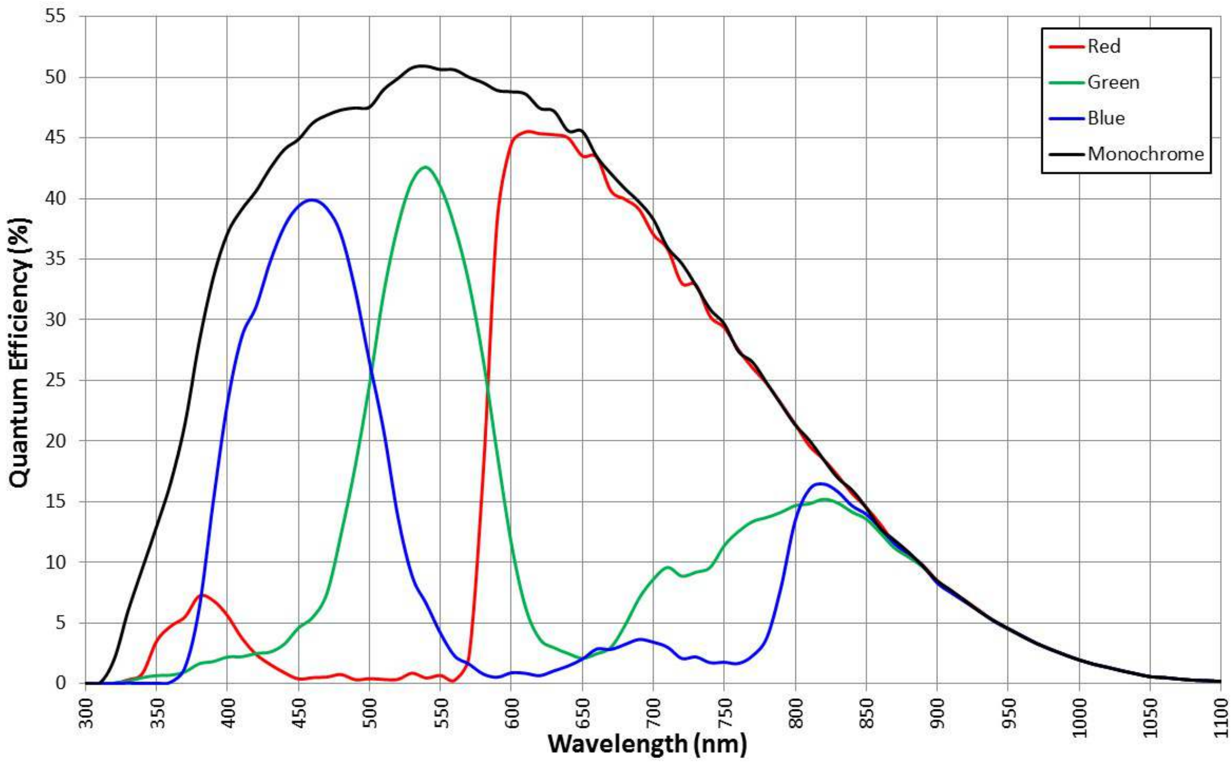


Figure 12. Color (Sparse CFA) QE with Microlens and MAR Glass

Angular Response

Horizontal − the incident light angle is varied in a plane parallel to the HCCD.
Vertical − the incident light angle is varied in a plane perpendicular to the HCCD.

Monochrome with Microlens

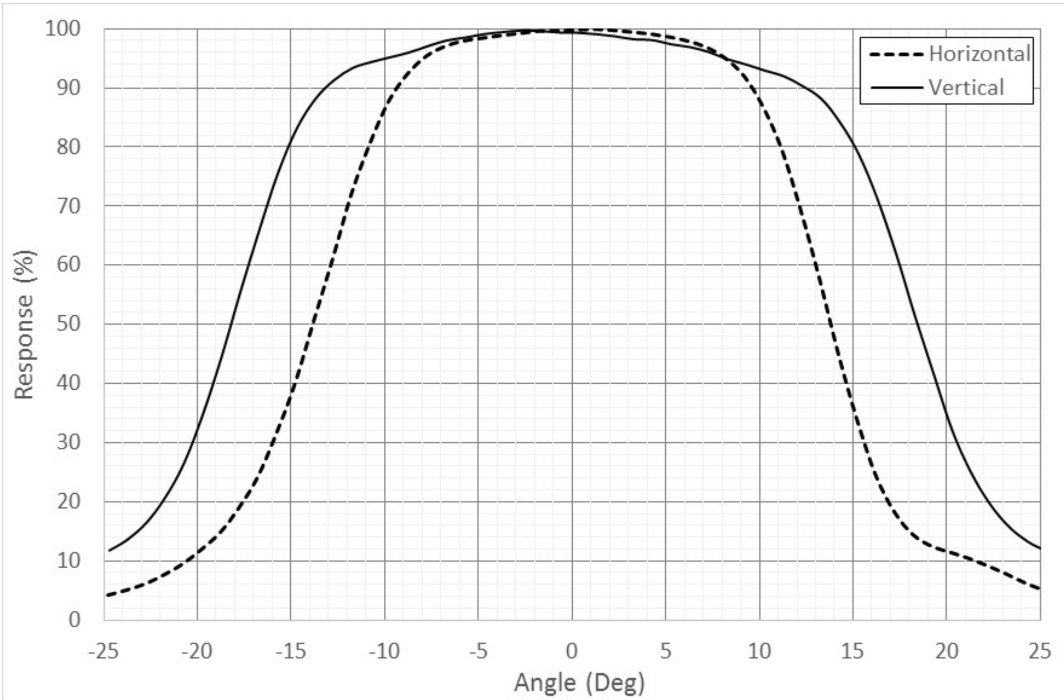


Figure 13. Monochrome with Microlens Angle Response

Color (Bayer RGB) with Microlens

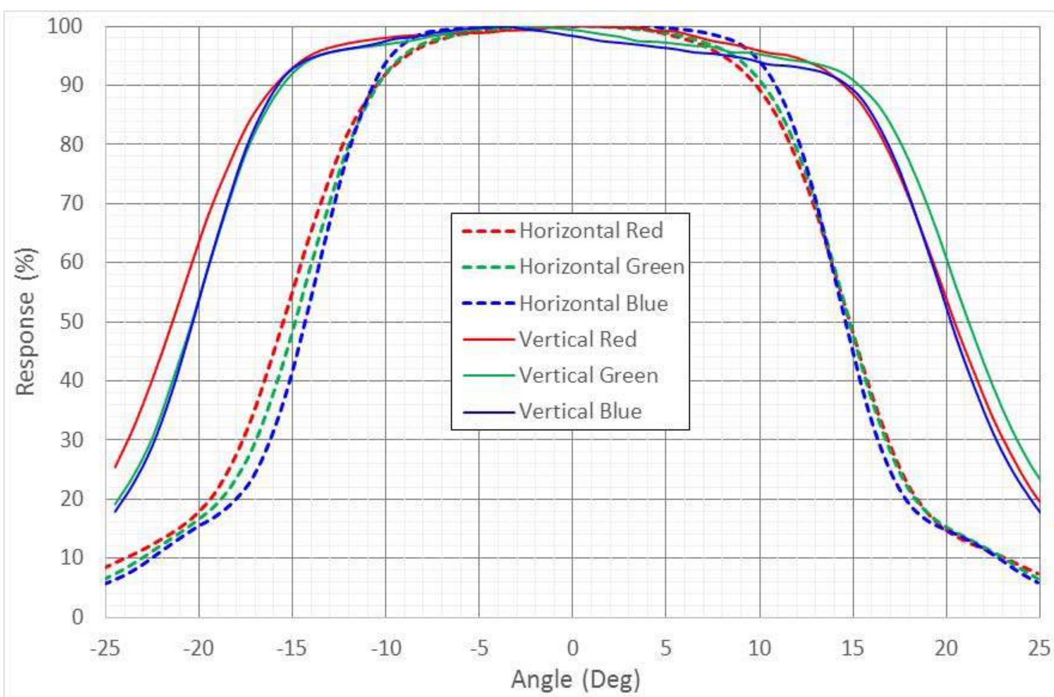


Figure 14. Color with Microlens Angle Response

Sparse Color with Microlens

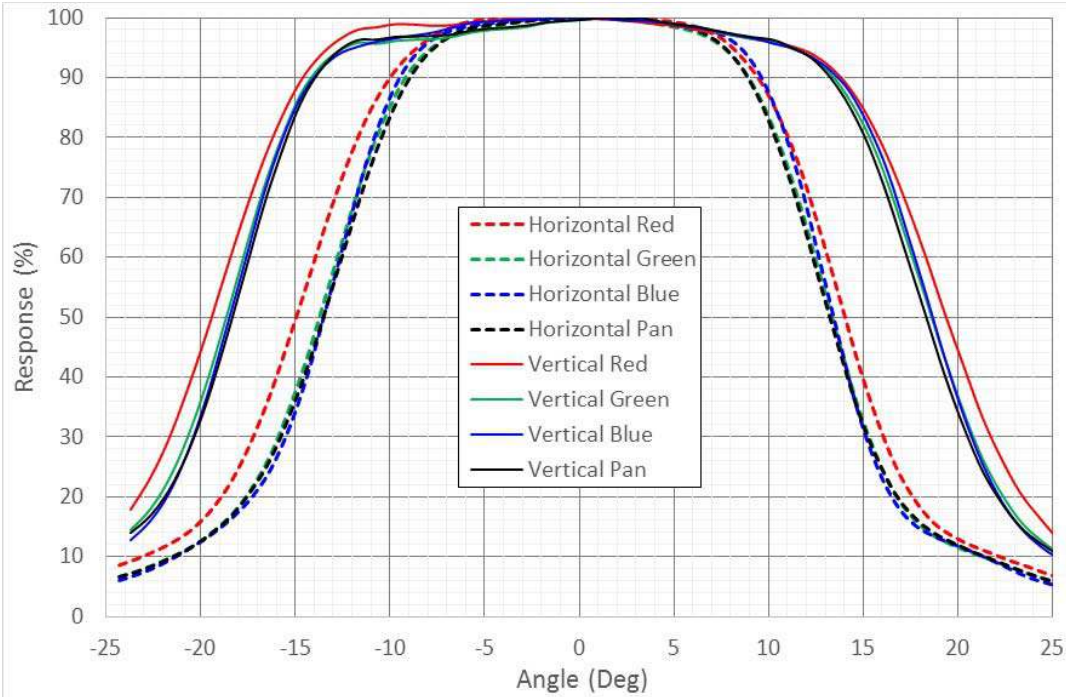


Figure 15. Sparse Color with Microlens Angle Response

Frame Rates

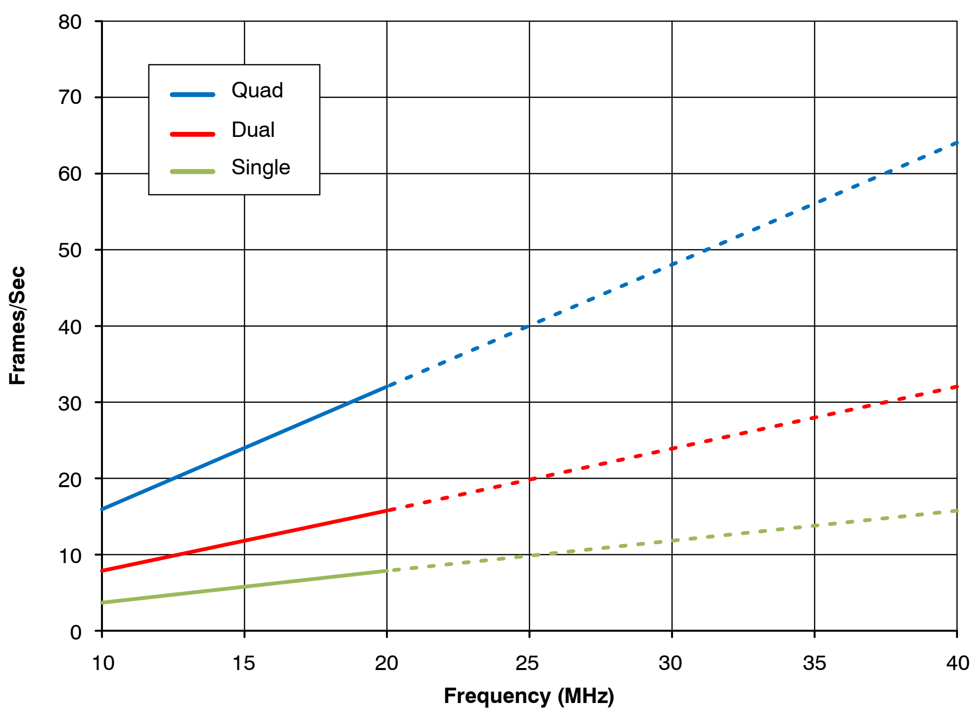


Figure 16. Frame Rates vs. Frequency

DEFECT DEFINITIONS

Table 8. DEFECT DEFINITIONS

Description	Threshold/Definition	Maximum Number Allowed	Notes
Major Dark Field Defective Bright Pixel	≥ 10 mV	20	1, 2
Major Bright Field Defective Dark Pixel	≥ 12%		
Minor Dark Field Defective Bright Pixel	≥ 5 mV	200	
Cluster Defect	A Group of 2 to 10 Contiguous Major Defective Pixels No Greater than 2 Pixels in Width	8	3
Column Defect	A Group of More than 10 Contiguous Major Dark Defective Pixels along a Single Column or 10 Contiguous Bright Defective Pixels along a Single Column	0	3, 4

1. The thresholds are defined for an operating temperature of 0°C, quad output mode, gain of 20X and a readout rate of 20 MHz. For operation at 22°C, thresholds of 30 mV for major bright pixels and 10 mV for minor bright pixels would give approximately the same numbers of defects.
2. For the color device, a bright field defective pixel deviates by 12% with respect to pixels of the same color.
3. Column and cluster defects are separated by no less than 2 good pixels in any direction (excluding single pixel defects).
4. Low exposure dark column defects are not counted at temperatures above 0°C.

OPERATION

Table 9. ABSOLUTE MAXIMUM RATINGS

(Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the description. If the level or the condition is exceeded, the device will be degraded and may be damaged. Operation at these values will reduce MTTF.)

Description	Symbol	Minimum	Maximum	Units	Notes
Operating Temperature	T_{OP}	−40	40	°C	1
Humidity	RH	5	90	%	2
Output Bias Current	I_{OUT}	–	60	mA	3
Off-Chip Load	CL	–	10	pF	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Noise performance will degrade at higher temperatures.
2. T = 25°C. Excessive humidity will degrade MTF. The maximum humidity for operation is 50% for OPNs beginning with KAE−02152−ABB−SD, KAE−02152−FBB−SD, and KAE−02152−QBB−SD.
3. Total for all outputs. Maximum current is −15 mA for each output. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher current and lower load capacitance at the expense of reduced gain (sensitivity).

Table 10. ABSOLUTE MAXIMUM VOLTAGE RATINGS BETWEEN PINS AND GROUND

Description	Minimum	Maximum	Units	Notes
VDD23ab, VDD23cd	−0.4	17.5	V	1
VOUT2, VOUT3	−0.4	15	V	
VDD1, VOUT1	−0.4	7.0	V	
V1B, V1T	ESD – 0.4	ESD + 22.0	V	
V2B, V2T, V3B, V3T, V4B, V4T	ESD – 0.4	ESD + 14.0	V	
H1S, H1B, H2S, H2B, H1BEM, H2BEM, H2SL, H2X, H2SW2, H2SW3, RG1, RG2, RG3	– 0.4	10	V	1
H1SEM, H2SEM	−0.4	20	V	
ESD	−9.0	0.0	V	
SUB	6.5	40	V	2, 3

1. “α” denotes a, b, c or d.
2. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions.*
3. The measured value for $VSUB_{REF}$ is a diode drop higher than the recommended minimum VSUB bias.

Power-Up and Power-Down Sequence

SUB and ESD power up first, then power up all other biases in any order. No pin may have a voltage less than ESD at any time. All HCCD pins must be greater than or equal to GND at all times. The SUB_{REF} pin will not become valid until VDD23ab has been powered, therefore the SUB voltage cannot be directly derived from the SUB_{REF} pin. The SUB pin should be at least 4 V before powering up VDD23ab or VDD23cd.

Table 11. DC BIAS OPERATING CONDITIONS

Description	Pins	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current	Notes
Output Amplifier Return	VSS1	V_{SS1}	−8.3	−8.0	−7.7	V	4 mA	
Output Amplifier Supply	VDD1	V_{DD1}	4.5	5.0	6.0	V	15 mA	
Output Amplifier Supply	VDD23	V_{DD23}	+14.7	+15.0	+15.3	V	37.0 mA	1
Ground	GND	GND	0.0	0.0	0.0	V	17.0 mA	
Substrate	SUB	V_{SUB}	5.0	$VSUB_{REF}$ – 0.5	$VSUB_{REF}$ + 28	V	Up to 1 mA (Determined by Photocurrent)	2
ESD Protection Disable	ESD	ESD	−8.3	−8.0	−7.7	V	0.25 mA	
Output Bias Current	VOUT	I_{OUT}	2.0	2.5	5.0	mA		

1. VDD bias pins for all four quadrants must be maintained at 15 V during operation.
2. For each image sensor the voltage output on the VSUBREF pin is programmed to be one diode drop, 0.5 V, above the nominal SUB voltage. The voltage output on VSUBREF is unique to each image sensor and may vary from 5.0 to 8.5 V. The output impedance of VSUBREF is approximately 100 k. The applied VSUB should be one diode drop lower than the VSUBREF value measured on the device, when VDD23 is at the specified voltage.

AC Operating Conditions

Table 12. CLOCK LEVELS

Pin	Function	HCCD and RG					
		Low Level			Amplitude		
		Low	Nominal	High	Low	Nominal	High
H2B(a,b,c,d)	Reversible HCCD Barrier 2	−0.2	0.0	0.2	3.1	3.3	3.6
H1B(a,b,c,d)	Reversible HCCD Barrier 1	−0.2	0.0	0.2	3.1	3.3	3.6
H2S(a,b,c,d)	Reversible HCCD Storage 2	−0.2	0.0	0.2	3.1	3.3	3.6
H2B(a,b,c,d)	Reversible HCCD Storage 1	−0.2	0.0	0.2	3.1	3.3	3.6
H2SW(2,3)(a,b,c,d)	HCCD Switch 2 and 3	−0.2	0.0	0.2	3.1	3.3	3.6
H2L(a,b,c,d)	HCCD Last Gate	−0.2	0.0	0.2	3.1	3.3	3.6
H2X(a,b,c,d)	Floating Gate Exit	−0.2	0.0	0.2	6.0	6.4	6.8
RG1(a,b,c,d)	Floating Gate Reset	Cap			3.1	3.3	3.6
RG(2,3)(a,b,c,d)	Floating Diffusion Reset	Cap			3.1	3.3	3.6
H1BEM(a,b,c,d)	Multiplier Barrier 1	−0.2	0.0	0.2	4.6	5.0	5.4
H2BEM(a,b,c,d)	Multiplier Barrier 2	−0.2	0.0	0.2	4.6	5.0	5.4
H1SEM(a,b,c,d)	Multiplier Storage 1	−0.3	0.0	0.3	7.0	–	18.0
H2SEM(a,b,c,d)	Multiplier Storage 2	−0.3	0.0	0.3	7.0	–	18.0

1. HCCD Operating Voltages. There can be no overshoot on any horizontal clock below −0.4 V: the specified absolute minimum. The H1SEM and H2SEM clock amplitudes need to be software programmable to adjust the charge multiplier gain.
2. Reset Clock Operation: The RG1, RG2, and RG3 signals must be capacitive coupled into the image sensor with a 0.01 μF to 0.1 μF capacitor. The reset clock overshoot can be no greater than 0.3 V, as shown in Figure 17, below:

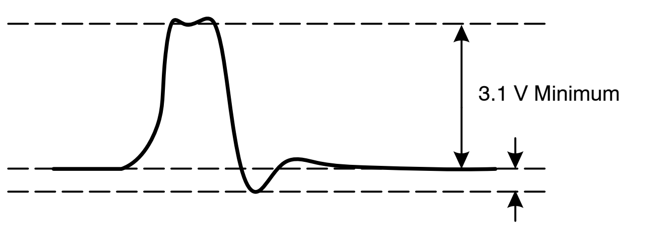


Figure 17. RG Clock Overshoot

Clock Capacitances

Pin	Capacitance (pF)	Pin	Capacitance (pF)	Pin	Capacitance (pF)	Pin	Capacitance (pF)
H1Sa	76	H1Ba	39	H1BEMa	56	H1SEMa	66
H1Sb	76	H1Bb	39	H1BEMb	56	H1SEMb	66
H1Sc	76	H1Bc	39	H1BEMc	56	H1SEMc	66
H1Sd	76	H1Bd	39	H1BEMd	56	H1SEMd	66
H2Sa	76	H2Ba	39	H2BEMa	56	H2SEMa	66
H2Sb	76	H2Bb	39	H2BEMb	56	H2SEMb	66
H2Sc	76	H2Bc	39	H2BEMc	56	H2SEMc	66
H2Sd	76	H2Bd	39	H2BEMd	56	H2SEMd	66

Note: The capacitance of all other HCCD pins 15 pF or less.

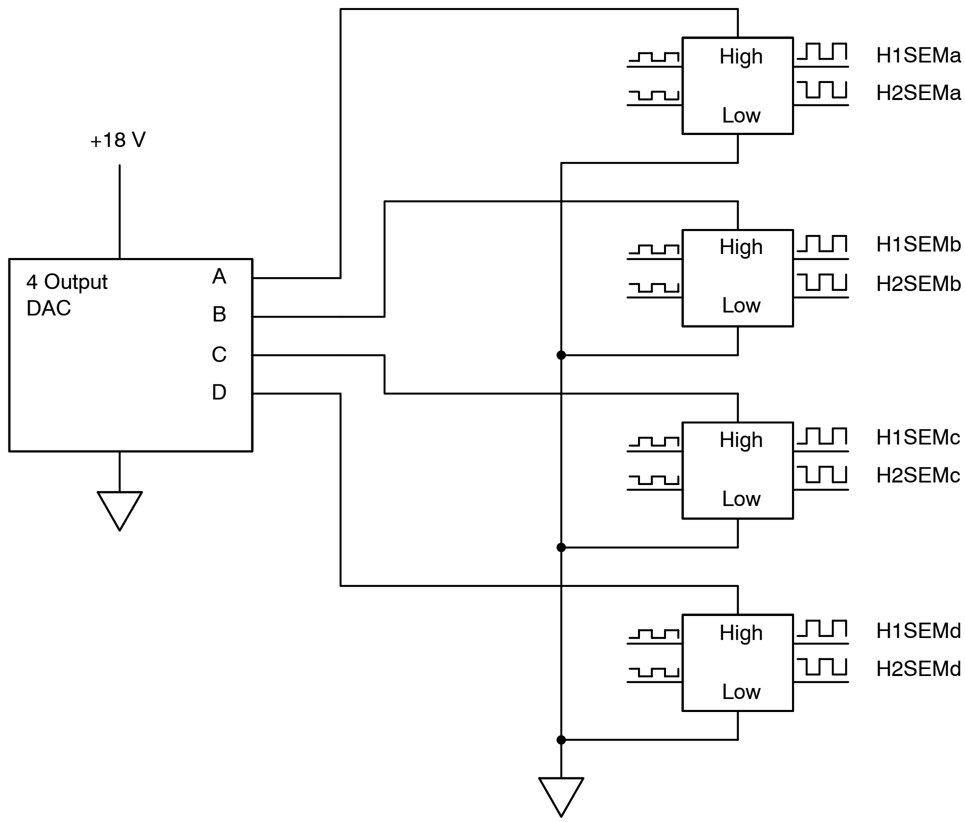


Figure 18. EMCCD Clock Adjustable Levels

For the EMCCD clocks, each quadrant must have independently adjustable high levels. All quadrants have a common low level of GND. The high level adjustments must be software controlled to balance the gain of the four outputs.

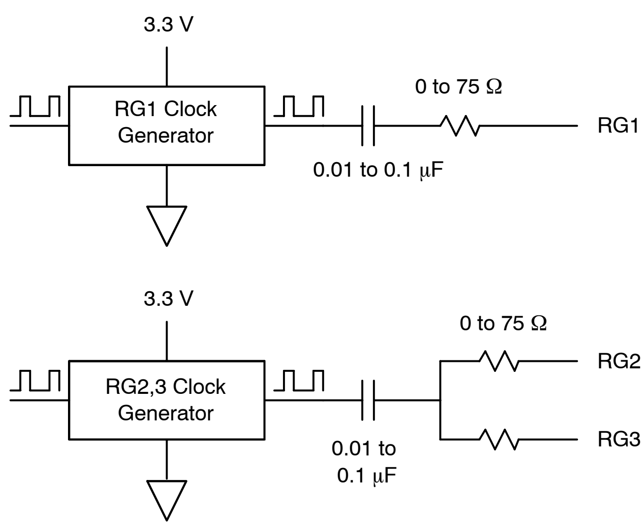


Figure 19. Reset Clock Drivers

The reset clock drivers must be coupled by capacitors to the image sensor. The capacitors can be anywhere in the range 0.01 to 0.1 μF. The damping resistor values would vary between 0 and 75 Ω depending on the layout of the circuit board.

Table 13. VCCD

Pin	Function	Low	Nominal	High
V(1,2,3,4)(T,B)	Vertical CCD Clock, Low Level	−8.0	−8.0	−6
V(1,2,3,4)(T,B)	Vertical CCD Clock, Mid Level	−0.2	0	0.2
V(1)(T,B)	Vertical CCD Clock, High (3rd) Level	8.5	9.0	12.5

1. The Vertical CCD operating voltages. The VCCD low level will be −8.0 V for operating temperatures of 0°C and above. Below 0°C the VCCD low level should be increased for optimum noise performance.

Table 14. BIAS VOLTAGES

Pin	Function	Low	Nominal	High
ESD	ESD	−8.3	−8.0	−7.7
SUB (Notes 1, 2)	Electronic Shutter	$VSUB_{REF}$ + 22	–	$VSUB_{REF}$ + 28
VDD1(a,b,c,d)	Floating Gate Power	4.5	5.0	6.0
VSS1(a,b,c,d)	Floating Gate Return	−8.3	−8.0	−7.7
VDD(2,3)(a,b,c,d)	Floating Diffusion Power	14.7	15.0	15.3
VOUT1(a,b,c,d)	Floating Gate Output Range	−0.5	1.0	2.5
VOUT(2,3)(a,b,c,d)	Floating Diffusion Output Range	8.0	10.0	12.0

1. Caution: Do not clock the EMCCD register while the electronic shutter pulse is high.
2. The substrate bias (SUB) should normally be kept at V_{AB}, which can be read from Pin 60. However, this value was determined from operation at 0°C, and has an approximate temperature dependence of 0.01 V/degree.

Device Identification

The device identification pin (DevID) may be used to determine which ON Semiconductor 5.5 micron pixel interline CCD sensor is being used.

Table 15. DEVICE IDENTIFICATION

Description	Pins	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current	Notes
Device Identification	DevID	DevID	44,000	50,000	56,000	Ω	0.3 mA	1, 2, 3

1. Nominal value subject to verification and/or change during release of preliminary specifications.
2. If the Device Identification is not used, it may be left disconnected.
3. After Device Identification resistance has been read during camera initialization, it is recommended that the circuit be disabled to prevent localized heating of the sensor due to current flow through the R_DeviceID resistor.

Recommended Circuit

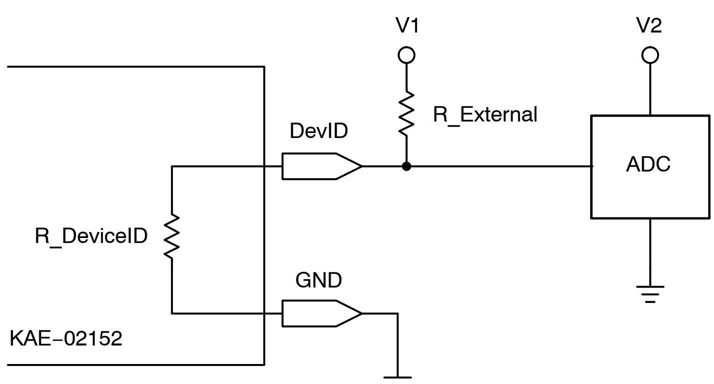


Figure 20. Device Identification Recommended Circuit

THEORY OF OPERATION

Image Acquisition

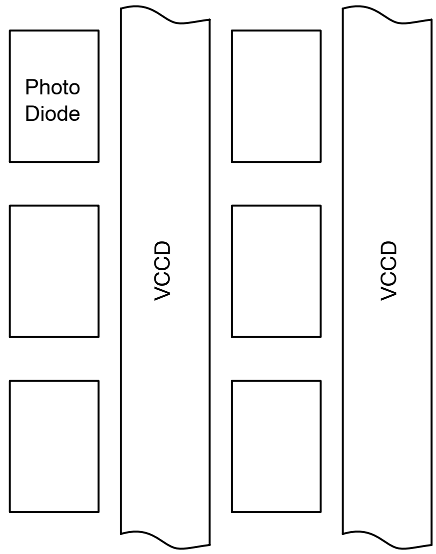


Figure 21. Illustration of 2 Columns and 3 Rows of Pixels

This image sensor is capable of detecting up to 20,000 electrons with a small signal noise floor of 1 electron all within one image. Each 5.5 μm square pixel, as shown in Figure 21 above, consists of a light sensitive photodiode and a portion of the vertical CCD (VCCD). Not shown is a microlens positioned above each photodiode to focus light away from the VCCD and into the photodiode. Each photon incident upon a pixel will generate an electron in the photodiode with a probability equal to the quantum efficiency.

The photodiode may be cleared of electrons (electronic shutter) by pulsing the SUB pin of the image sensor up to a voltage of 30 V to 40 V ($VSUB_{REF}$ + 22 V to $VSUB_{REF}$ + 28 V) for a time of at least 1 μs. When the SUB pin is above 30 V, the photodiode can hold no electrons, and the electrons flow downward into the substrate. When the voltage on SUB drops below 30 V, the integration of electrons in the photodiode begins. The HCCD clocks should be stopped when the electronic shutter is pulsed, to avoid having the large voltage pulse on SUB coupling into the video outputs and altering the EMCCD gain.

It should be noted that there are certain conditions under which the device will have no anti-blooming protection: when the V1T and V1B pins are high, very intense illumination generating electrons in the photodiode will flood directly into the VCCD. When the electronic shutter pulse overlaps the V1T and V1B high-level pulse that transfers electrons from the photodiode to the VCCD, then photo-electrons will flow to the substrate and not the VCCD. This condition may be desirable as a means to obtain very short integration times.

The VCCD is shielded from light by metal to prevent detection of more photons. For very bright spots of light, some photons may leak through or around the metal light shield and result in electrons being transferred into the VCCD. This is called image smear.

Image Readout

At the start of image readout, the voltage on the V1T and V1B pins is pulsed from 0 V up to the high level for at least 1 μs and back to 0 V, which transfers the electrons from the photodiodes into the VCCD. If the VCCD is not empty, then the electrons will be added to what is already in the VCCD. The VCCD is read out one row at a time. During a VCCD row transfer, the HCCD clocks are stopped. All gates of type H1 stop at the high level and all gates of type H2 stop at the low level. After a VCCD row transfer, charge packets of electrons are advanced one pixel at a time towards the output amplifiers by each complimentary clock cycle of the H1 and H2 gates.

The charge multiplier has a maximum charge handling capacity (after gain) of 20,000 electrons. This is not the average signal level. It is the maximum signal level. Therefore, it is advisable to keep the average signal level at 15,000 electrons or less to accommodate a normal distribution of signal levels. For a charge multiplier gain of 20x, no more than 15,000/20 = 750 electrons should be allowed to enter the charge multiplier. Overfilling the charge multiplier beyond 20,000 electrons will shorten its useful operating lifetime. In addition, sending signals larger than 180–200 electrons into the EMCCD will produce images with lower signal-to-noise ratio than if they were read out of the normal floating diffusion output. See Application Note AND9244.

To prevent overfilling the charge multiplier, a non-destructive floating gate output amplifier (VOUT1) is provided on each quadrant of the image sensor as shown in Figure 22.

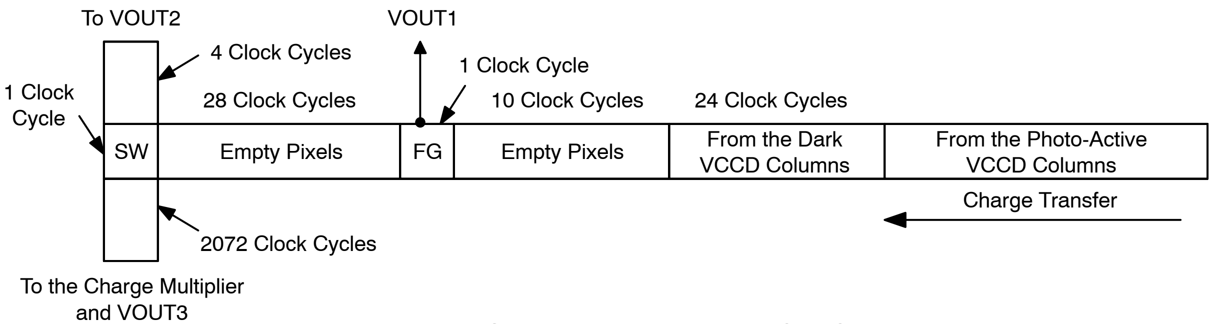
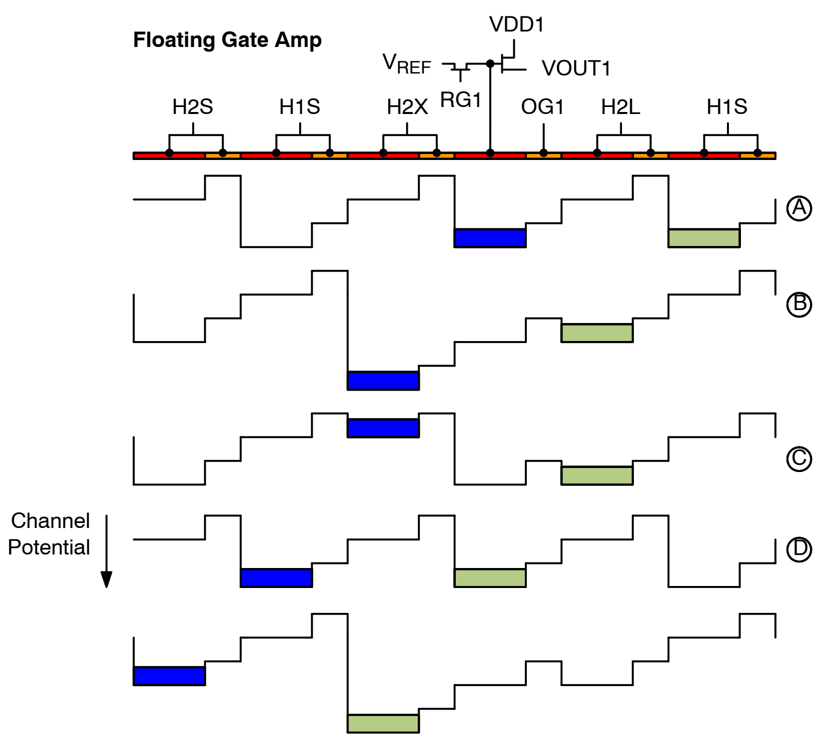


Figure 22. The Charge Transfer Patch of One Quadrant

The non-destructive floating gate output amplifier is able to sense how much charge is present in a charge packet without altering the number of electrons in that charge packet. This type of amplifier has a low charge-to-voltage conversion gain (about 6.2 $\mu V/e^-$) and high noise (about 60 electrons), but it is being used only as a threshold detector, and not an imaging detector. Even with 60 electrons of noise, it is adequate to determine whether a charge packet is greater than or less than the recommended threshold of 180 electrons.

After one row has been transferred from the VCCD into the HCCD, the HCCD clock cycles should begin. After 10 clock cycles, the first dark VCCD column pixel will arrive at VOUT1. After another 24 (34 total) clock cycles, the first photo-active charge packet will arrive at VOUT1.

The transfer sequence of a charge packet through the floating gate amplifier is shown in Figure 23 below. The time steps of this sequence are labeled A through D, and are indicated in the timing diagram shown as Figure 24. The RG1 gate is pulse high during the time that the H2X gate is pulsed high. This holds the floating gate at a constant voltage so the H2X gate can pull the charge packet out of the floating gate. The RG1 pulse should be at least as wide as the H2X pulse. The H2X pulse width should be at least 12 ns. The rising edge of H2X relative to the falling edge of H1S is critical. The H2X pulse cannot begin its rising edge transition until the H1S edge is less than 0.4 V. If the H2X rising edge comes too soon then there may be some backwards flow of charge for signals above 10,000 electrons.



Note: The blue and green rectangles represent two separate charge packets. The direction of charge transfer is from right to left.

Figure 23. Charge Packet Transfer Sequence through the Floating Gate Amplifier

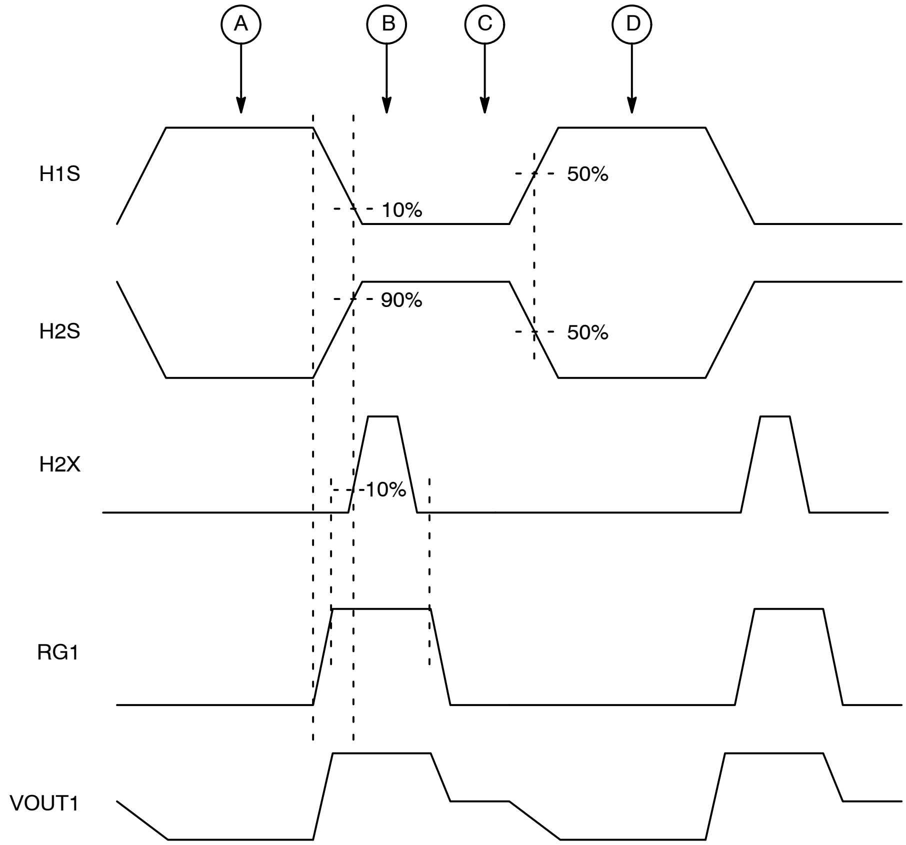


Figure 24. Timing Signals that Control the Transfer of Charge through the Floating Gate Amplifier

The charge packet is transferred under the floating gate on the falling edge of H2L. When this transfer takes place the floating gate is not connected to any voltage source. The presence of charge under the gate causes a change in voltage on the floating gate according to V = Q / C, where Q is the size of the charge packet and C is the capacitance of the floating gate. With an output sensitivity of 6.2 μV/e⁻, each electron on the floating gate would give a 6.2 μV change in VOUT1 voltage. Therefore if the decision threshold is to only allow charge packets of 180 electrons or less into the charge multiplier, this would correspond to 180 × 6.2 = 1.1 mV. If the video output is less than 1.1 mV, then the camera must set the timing of the H2SW2 and H2SW3 pins to route the charge packet to the charge multiplier. This action must take place 28 clock cycles after the charge packet was under the floating gate amplifier. The 28 clock cycle delay is to allow for pipeline delays of the A/D converter inside the analog front end. The timing generator must examine the output of the analog front end and dynamically alter the timing on H2SW2 and H2SW3. To route a charge packet to the charge multiplier (VOUT3), H2SW2 is held at GND and H2SW3 is clocked with the same timing as H2S for that one clock cycle. To route a charge packet to the low gain output amplifier (VOUT2), H2SW3 is held at GND and H2SW2 is clocked with the same timing as H2S for that one clock cycle.

When operating the device at maximum (40 MHz) data rate, all the charge must be routed through the low gain amplifier (VOUT2). This is best accomplished with the floating gate reset (RG1) held at its high level while clocking the HCCD, and the H2X gate clocked with the same timing as H2S and H2B. During the line timing patterns L1 or L2, the RG1 gate should be clocked low. There is a diode on the sensor that sets the DC offset of the RG1 gate when it is clocked low. If the RG1 is not clocked low once per line then the RG1 DC offset will drift. This timing scheme is represented in the diagram shown below:

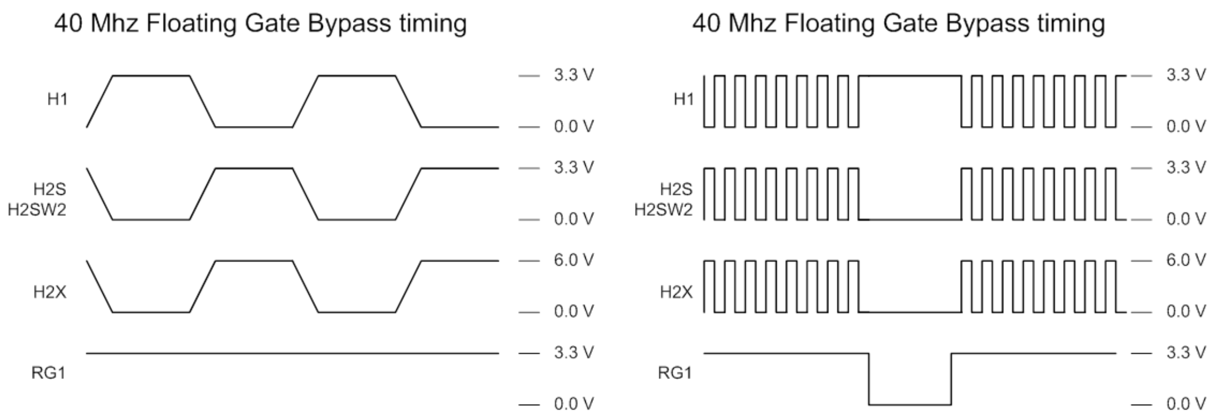


Figure 25. 40 MHz Floating Gate Bypass Timing

EMCCD OPERATION

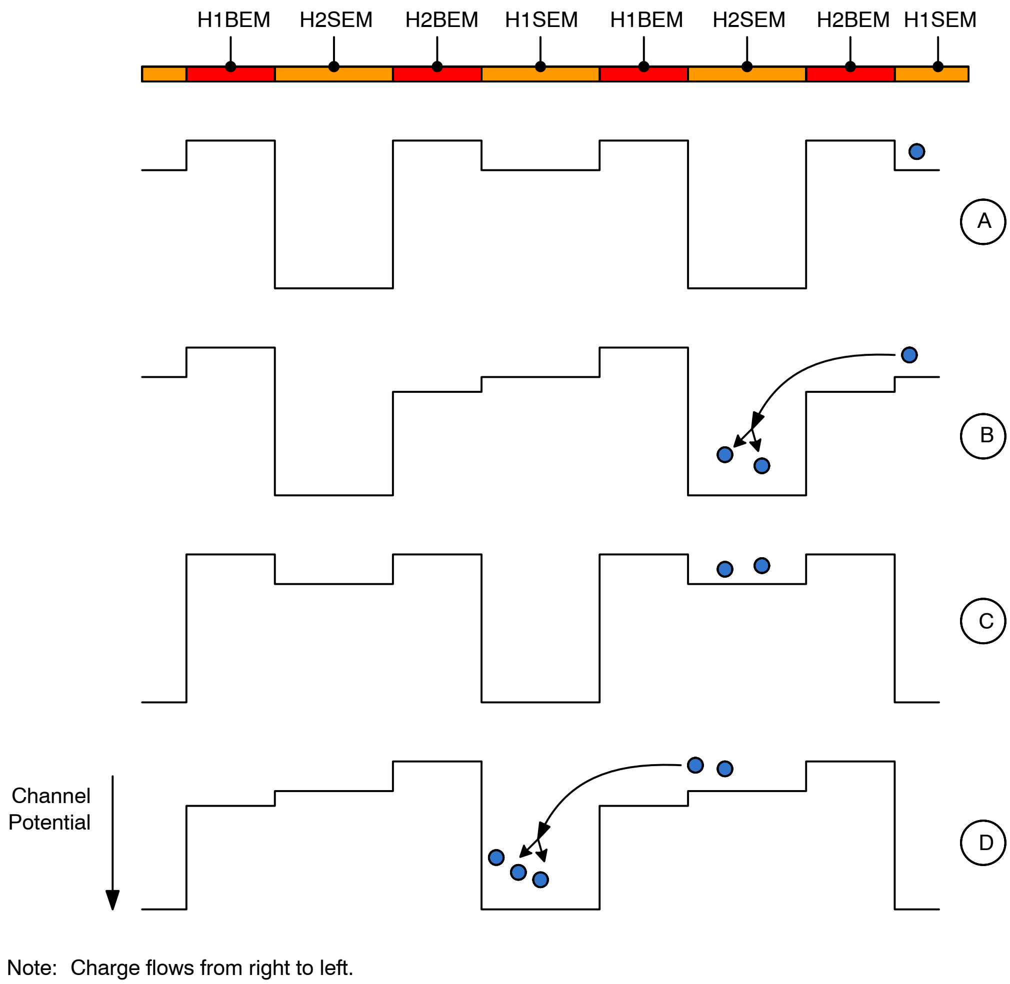


Figure 26. The Charge Multiplication Process

The charge multiplication process, shown in Figure 26 above, begins at time step A, when an electron is held under the H1SEM gate. The H2BEM and H1BEM gates block the electron from transferring to the next phase until the H2SEM has reached its maximum voltage. When the H2BEM is clocked from 0 to 5 V, the channel potential under H2BEM increases until the electron can transfer from H1SEM to H2SEM. When the H2SEM gate is above 10 V, the electric field between the H2BEM and H2SEM gates gives the electron enough energy to free a second electron which is collected under H2SEM. Then the voltages on H2BEM and H2SEM are both returned to 0 V at the same time that H1SEM is ramped up to its maximum voltage. Now the process can repeat again with charge transferring into the H1SEM gate.

The alignment of clock edges is shown in Figure 27. The rising edge of the H1BEM and H2BEM gates must be delayed until the H1SEM or H2SEM gates have reached their maximum voltage. The falling edge of H1BEM and H2BEM must reach 0 V before the H1SEM or H2SEM reach 0 V. There are a total of 1,800 charge multiplying transfers through the EMCCD on each quadrant.

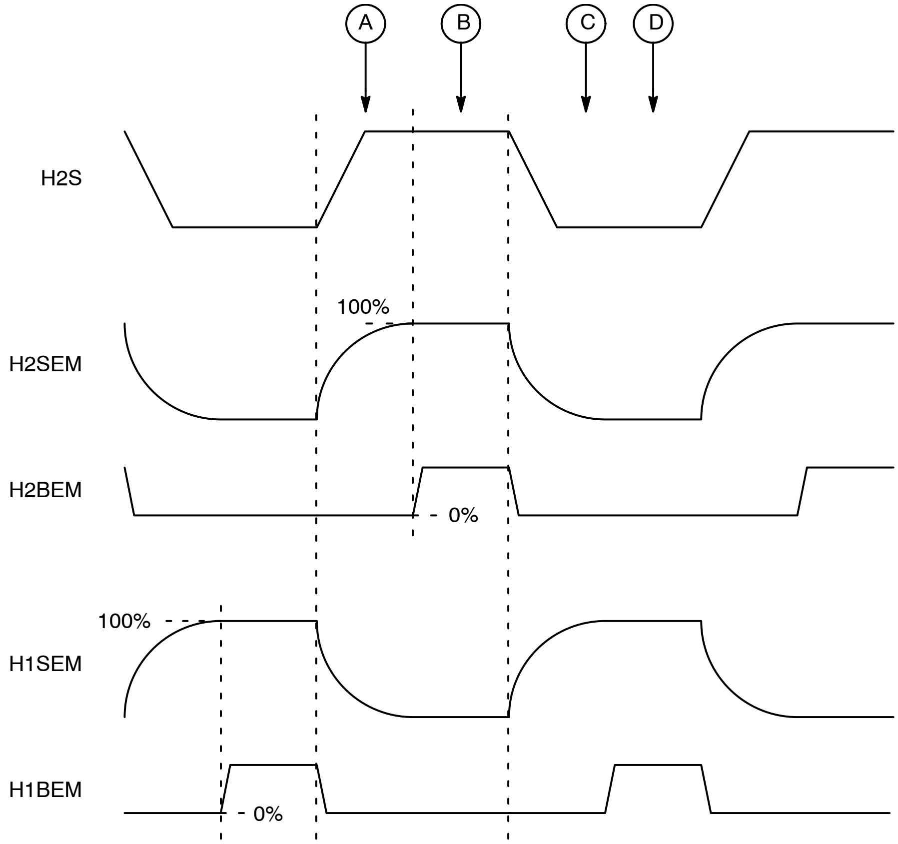
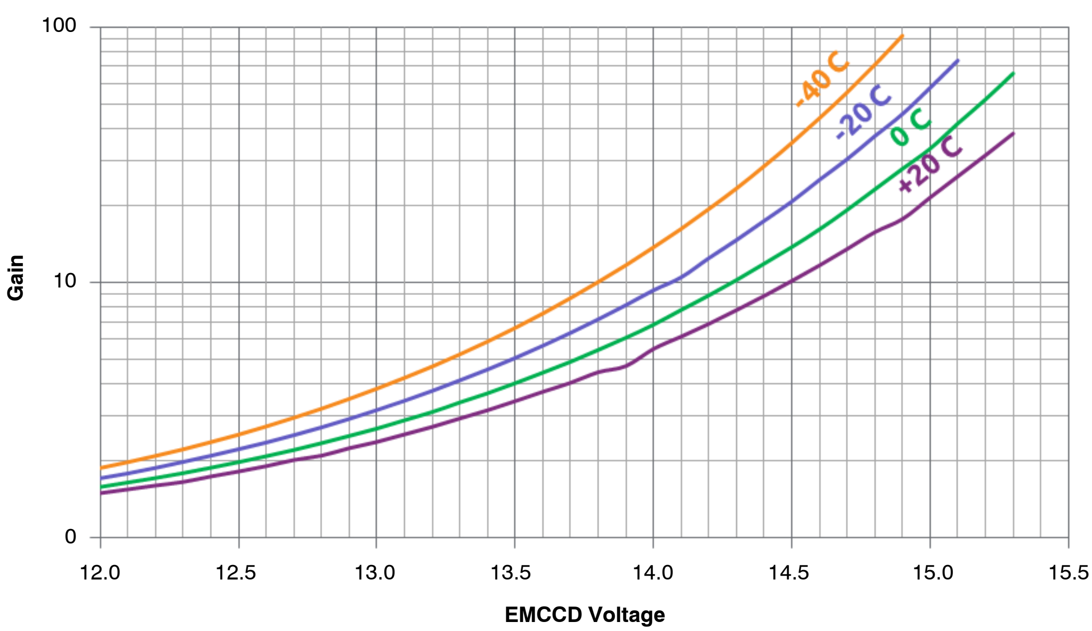


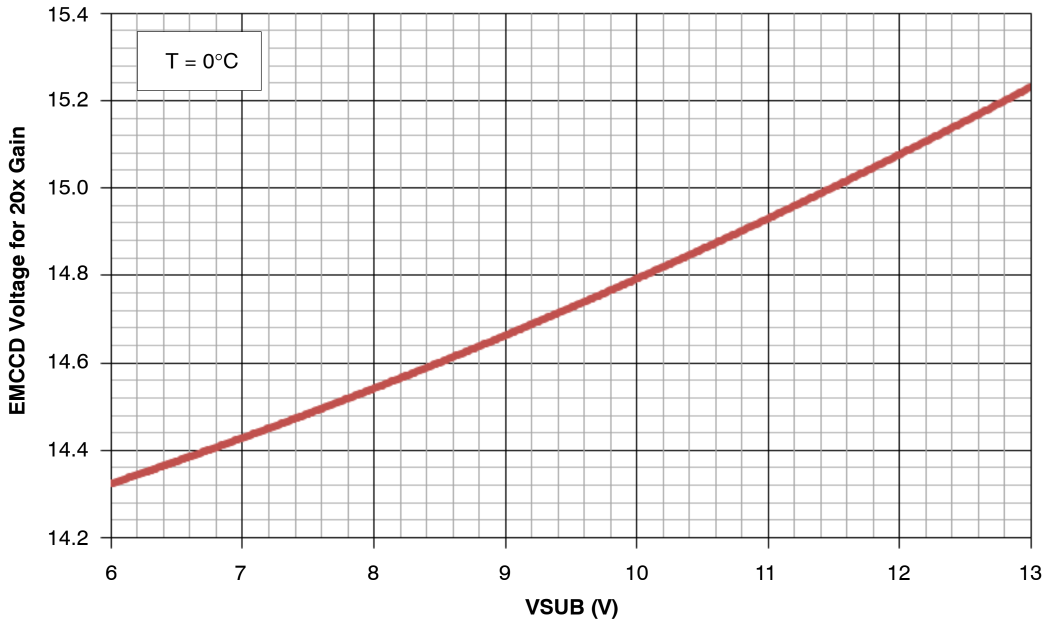
Figure 27. The Timing Diagram for Charge Multiplication

The amount of gain through the EMCCD will depend on temperature and H1SEM and H2SEM voltage as shown in Figure 28. Gain also depends on substrate voltage, as shown in Figure 29, and on the input signal, as shown in Figure 30.



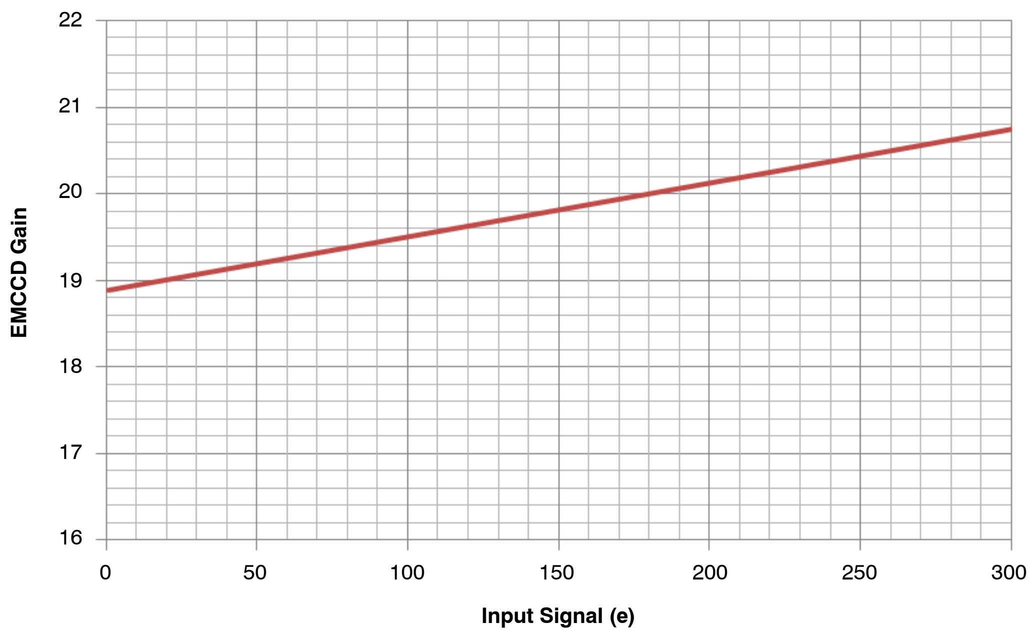
Note: This figure represents data from only one example image sensor, other image sensors will vary.

Figure 28. The Variation of Gain vs. EMCCD High Voltage and Temperature



Note: This figure represents data from only one example image sensor, other image sensors will vary.

Figure 29. The Change in the Required EMCCD Voltage for a Gain of 20x vs. the Substrate Voltage



Note: The EMCCD voltage was set to provide 20x gain with an input of 180 electrons.

Figure 30. EMCCD Gain vs. Input Signal

If more than one output is used, then the EMCCD high level voltage must be independently adjusted for each quadrant. This is because each quadrant will require a slightly different voltage to obtain the same gain. In addition, the voltage required for a given gain differs unpredictably from one image sensor to the next, as in Figure 31. Because of this, the gain vs. voltage relationship must be calibrated for each image sensor, although within each quadrant, the H1SEM and H2SEM high level voltage should be equal.

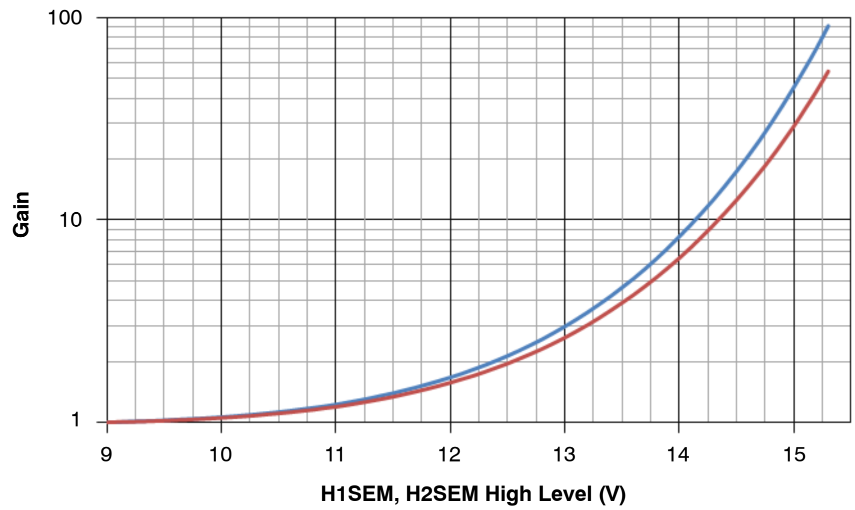
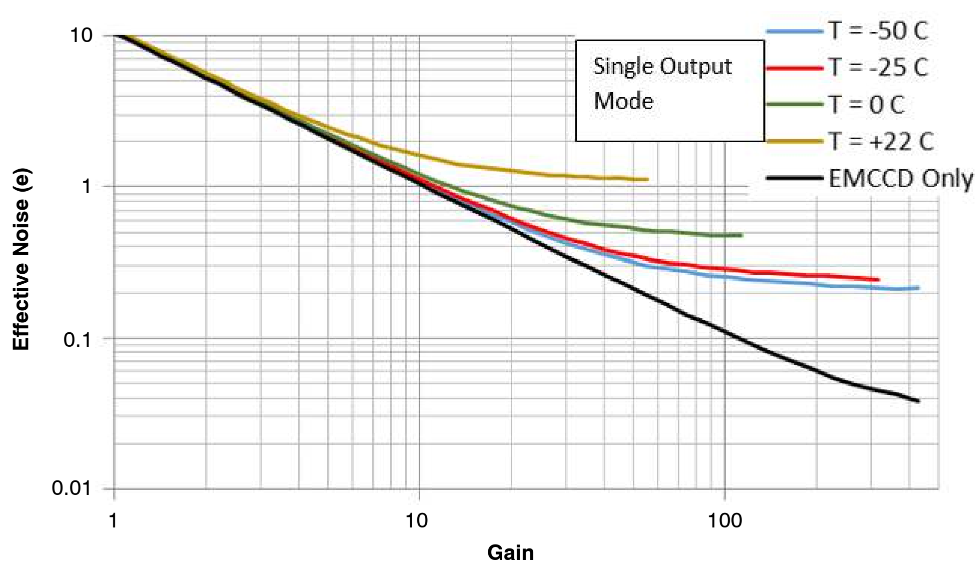


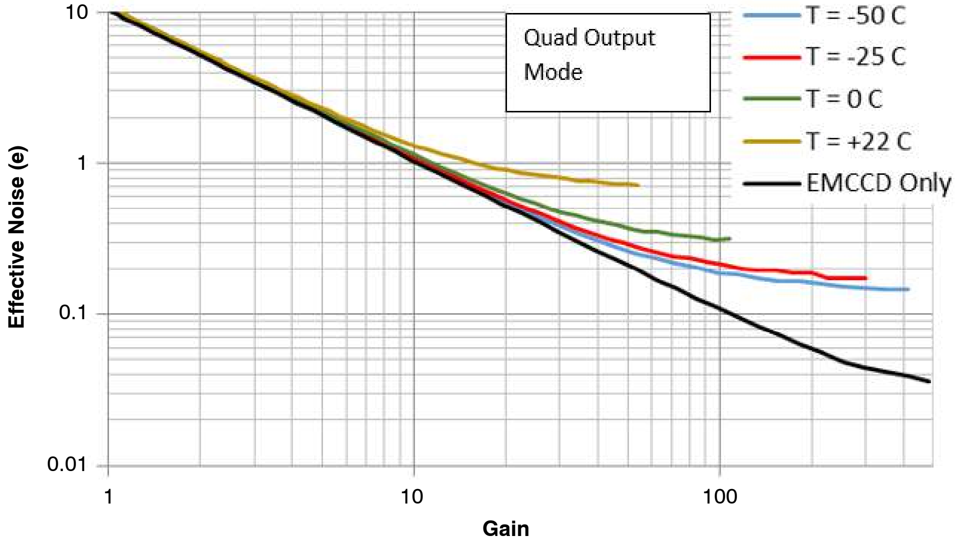
Figure 31. An Example Showing How Two Image Sensors Can Have Different Gain vs. Voltage Curves

The effective output noise of the image sensor is defined as the noise of the output signal divided by the gain. This is measured with zero input signal to the EMCCD. Figures 32 and 33 show the EMCCD by itself has a very low noise that goes as the noise at gain = 1 divided by the gain. The EMCCD has very little clock-induced charge and does not require elaborate sinusoidal waveform clock drivers. Simple square wave clock drivers with a resistor between the driver and sensor for a small RC time constant are all that is needed. However, the pixel array may acquire spurious charge as a function of VCCD clock driver characteristics. Also, the VCCD is sensitive to hot electron luminescence emitted from the output amplifiers during image readout. These two factors limit the noise floor of the total imaging array.



Note: This figure represents data from only one example image sensor, other image sensors will vary.

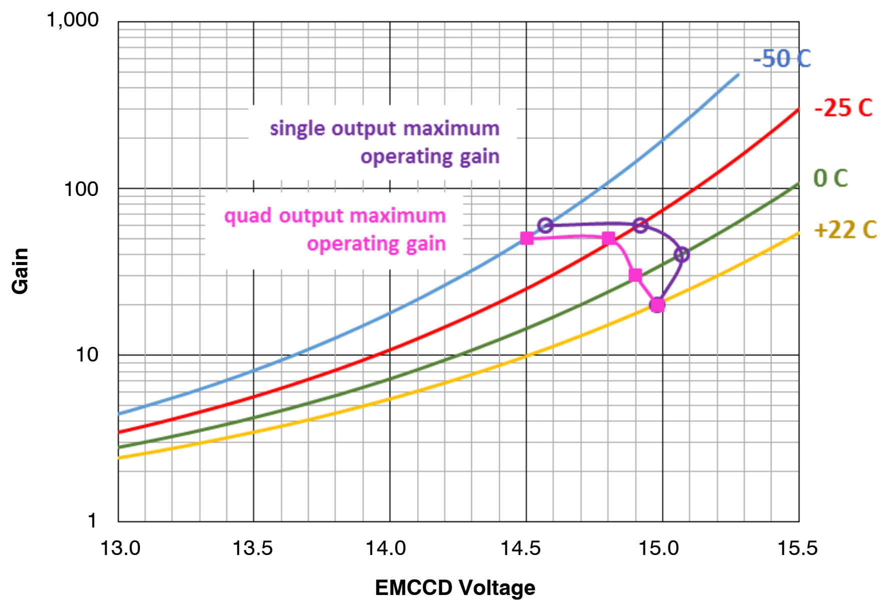
Figure 32. EMCCD Output Noise vs. EMCCD Gain in Single Output Mode at −50 to 22°C



Note: This figure represents data from only one example image sensor, other image sensors will vary.

Figure 33. EMCCD Output Noise vs. EMCCD Gain in Quad Output Mode at −50 to 22°C

Because of these pixel array noise sources, it is recommended that the maximum gain used be 40x at 0°C, which typically gives a noise floor between 1e and 0.4e. Using higher gains will provide limited benefit and will degrade the signal to noise ratio due to the EMCCD excess noise factor. Furthermore, the image sensor is not limited by dark current noise sources when the temperature is below 25°C. Therefore, cooling below 25°C will not provide a significant improvement to the noise floor. Lower temperatures will reduce the number of hot pixel defects observed only during image integration times longer than 1 s. Note the useful plot below:



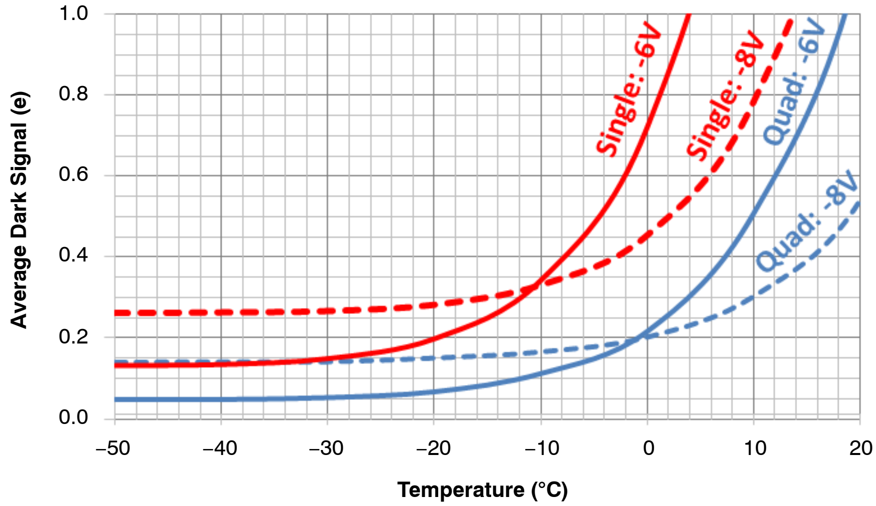
WARNING: The EMCCD should not be operated near saturation for an extended period, as this may result in gain aging and permanently reduce the gain. It should be noted that device degradation associated with gain aging is not covered under the device warranty.

Figure 34. Gain vs. Voltage with Maximum Recommended Operating Gains Marked

Choosing the Operating Temperature

The reasons for lowering the operating temperature are to reduce dark current noise and to reduce image defects. The average dark signal from the VCCD and photodiodes must be less than 1e in order to have a total system noise less than 1e when using the EMCCD. Figures 35 and 36 illustrate how the amount of dark signal in the VCCD is dependent on both temperature and voltage, and may be used to choose the operating temperature and VCCD clock low level voltage.

When operating in quad output mode at 0°C either −6 V or −8 V may be used for the VCCD clock low level voltage because the dark signal will be equal. But if the operating temperature is −20°C then the VCCD clock low level voltage should be set to −6 V for the lowest VCCD dark signal. For single output mode, the VCCD clock low level voltage should be set to −6 V for temperatures of −10°C or lower and −8 V for temperatures of −10°C or higher.



Note: Both are for a HCCD frequency of 20 MHz. The VCCD low level voltage is shown for each curve.

Figure 35. Dark Signal from VCCD in Quad and Single Output Modes

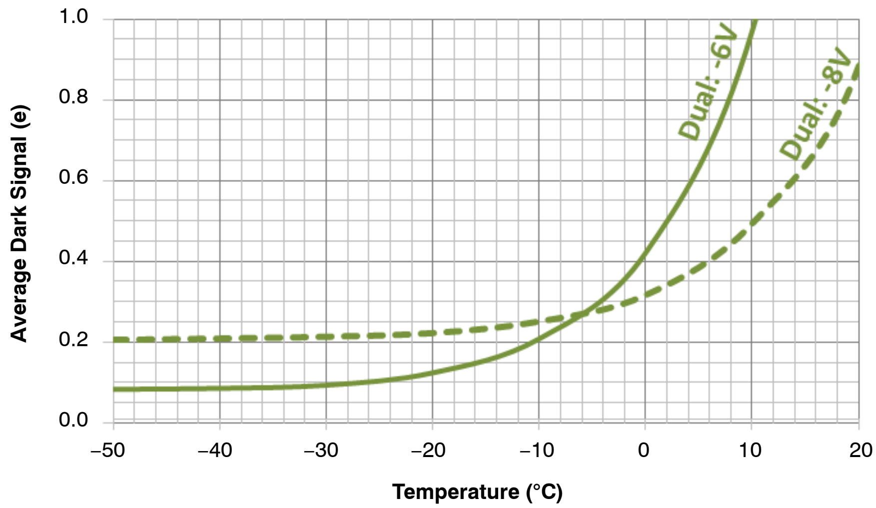


Figure 36. Dark Signal from VCCD in Dual Output Mode at HCCD Frequency 20 MHz

The reason for the different temperature dependencies with the VCCD low level voltage at −6 V vs. −8 V is spurious charge generation (sometimes called clock-induced charge). When the VCCD low level is at −8 V, the VCCD is accumulated with holes, which reduces the rate of dark current signal generation. However, the amount of clock induced charge is greater. At VCCD low level of −6 V, the VCCD is no longer accumulated with holes. So, clock-induced charge generation is less, but dark current is increased.

In quad output mode, the clock induced charge generated and the dark current signal are equal at T = 0°C. Below T = 0°C, the dark current signal is smaller than the clock induced charge, so −6 V is the best voltage. Above T = 0°C, the dark current signal dominates, and −8 V is the best voltage. The dark signal stops decreasing below T = −20°C because the VCCD is detecting hot electron luminescence from the output amplifiers during image readout.

In addition to dark noise, image defects also impact the optimum operating temperature. Although the average photodiode dark current is negligible at temperatures below 20°C, as shown by Figure 37, the number of photodiode hot-pixel defects is a function of temperature and will decrease with lower temperature.

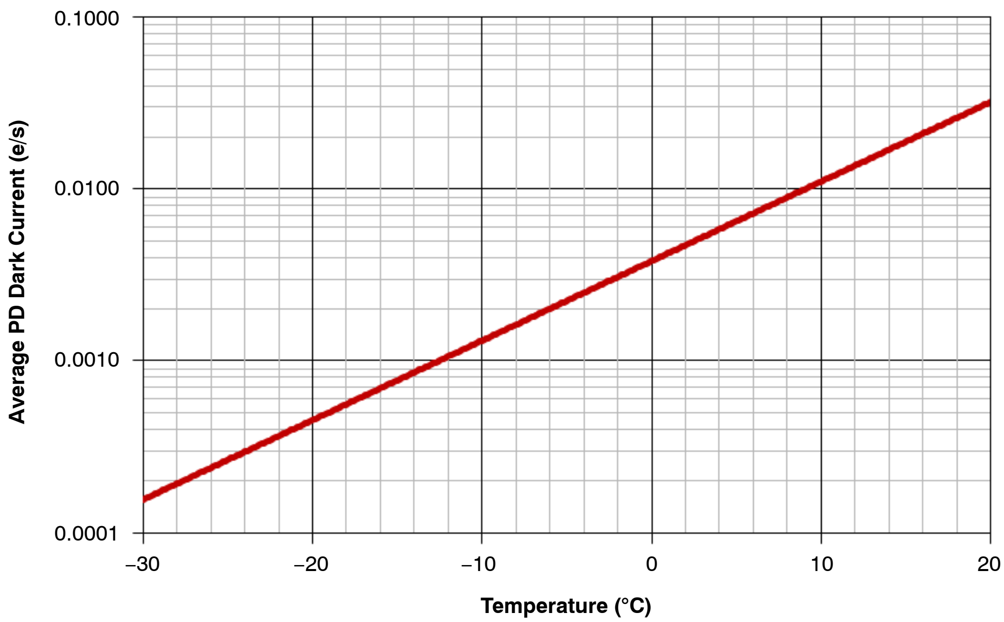


Figure 37. Photodiode Dark Current vs. Temperature

Note that the preceding figures are representative data only, and are not intended as a defect specification.

Choosing the Charge Switch Threshold

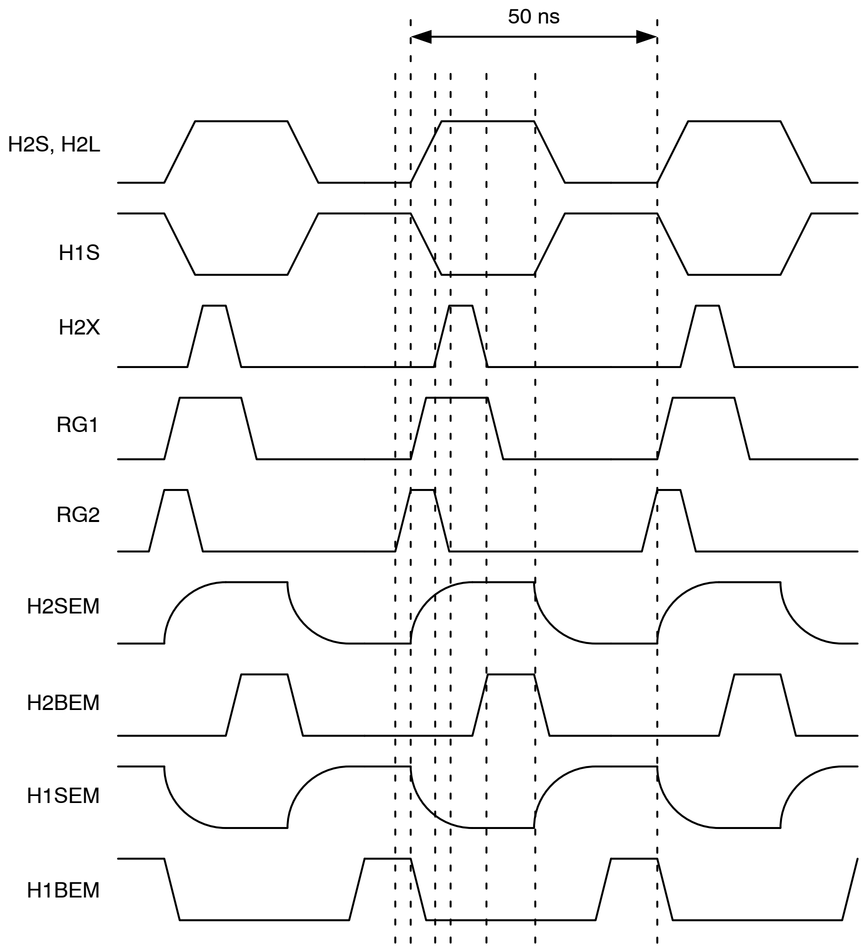
The floating gate output amplifier (VOUT1) is used to decide the routing of a pixel at the charge switch. Pixels with large signals should be routed to the normal floating diffusion amplifier at VOUT2. Pixels with small signals should be routed to the EMCCD and VOUT3. The routing of pixels is controlled by the timing on H2SW2 and H2SW3. The optimum signal threshold for that transition between VOUT2 and VOUT3 is when the signal to noise ratio (S/N) of VOUT2 is equal to the S/N of VOUT3. This signal is given by

$$S = \sigma_T^2 \cdot \frac{G + 1}{G} \qquad \text{(eq. 1)}$$

where *G* is the EMCCD gain, *S* is the signal level, and σ_T is the total system noise on VOUT2 in the dark. For values of *G* greater than 10, the optimum signal threshold occurs when then signal equals the square of the total system noise floor σ_T. Depending on the skill of the camera designer, σ_T will range from 8 to 12 e^-. If the camera has a total system noise of 10 e^-, then the threshold should be set to 100 e^-. However, the floating gate amplifier noise is approximately 60 e−, and so would dominate, making it preferable to set the threshold to at least 3 times the floating gate amplifier noise, or 180 e^-. Sending signals larger than 180 e^- into the EMCCD will produce images with lower S/N than if they were read out of the normal floating diffusion output of VOUT2. See Application Note AND9244.

TIMING DIAGRAMS

Pixel Timing



Note: The minimum time for one pixel is 50 ns.

Figure 38. Pixel Timing Pattern P1

Black Clamp, VOUT1, VOUT2, and VOUT3 Alignment at Line Start

The black level clamp should start 3 clock cycles into the line and be active for 28 clock cycles of each row. The first photoactive pixel will arrive at the VOUT1 (floating gate) output after 34 clock cycles. The first photoactive pixel will arrive at either the VOUT2 or VOUT3 after 68 clock cycles, depending on the timing of H2SW2 and H2SW3.

When in dual or quad output mode, each row must have exactly 1,036 HCCD clock cycles. The pixels arrive at VOUT3 on the same clock cycle and exactly two rows after they would have arrived at VOUT2.Changing the number of HCCD clock cycles with introduce an offset between when pixels arrive at VOUT2 or VOUT3.

When in single mode, each row must have exactly 2,072 HCCD clock cycles. The pixels arrive at VOUT3 on the same clock cycle and exactly one row after they would have arrived at VOUT2.Changing the number of HCCD clock cycles with introduce an offset between when pixels arrive at VOUT2 or VOUT3.

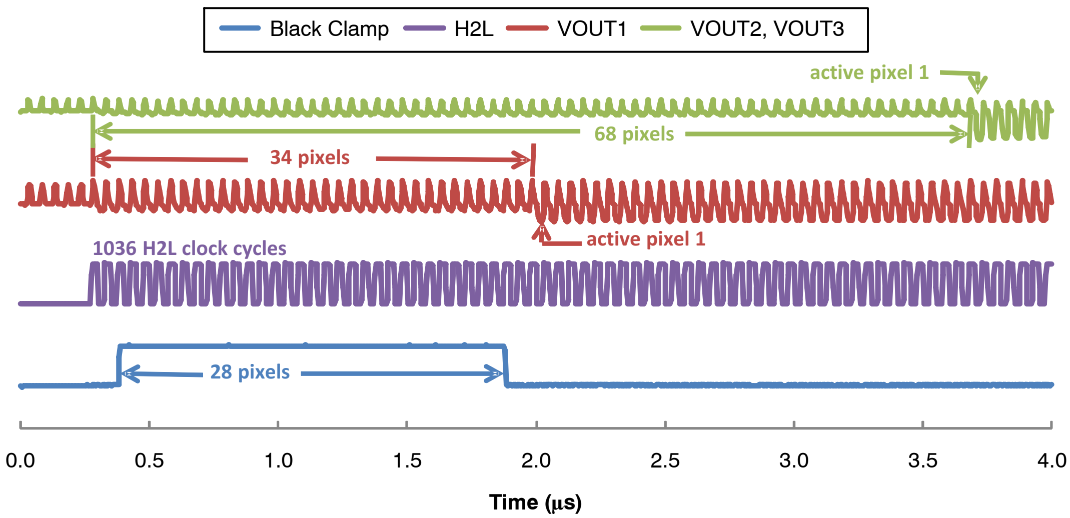


Figure 39. Video Output at Each Line Start

H2L, VOUT1, VOUT2, and VOUT3 Alignment at End of Line

The last active pixel (the center column of the image), arrives at VOUT2 or VOUT3 on the 1,036th clock cycle of the HCCD. The last photoactive pixel arrives at VOUT1 34 clock cycles before VOUT2 or VOUT3. When in single output mode, the pixels arrive at VOUT3 one line delayed from when they would have arrived at VOUT2. When in dual or quad output modes, the pixels arrive at VOUT3 two lines delayed from when they would have arrived at VOUT2.

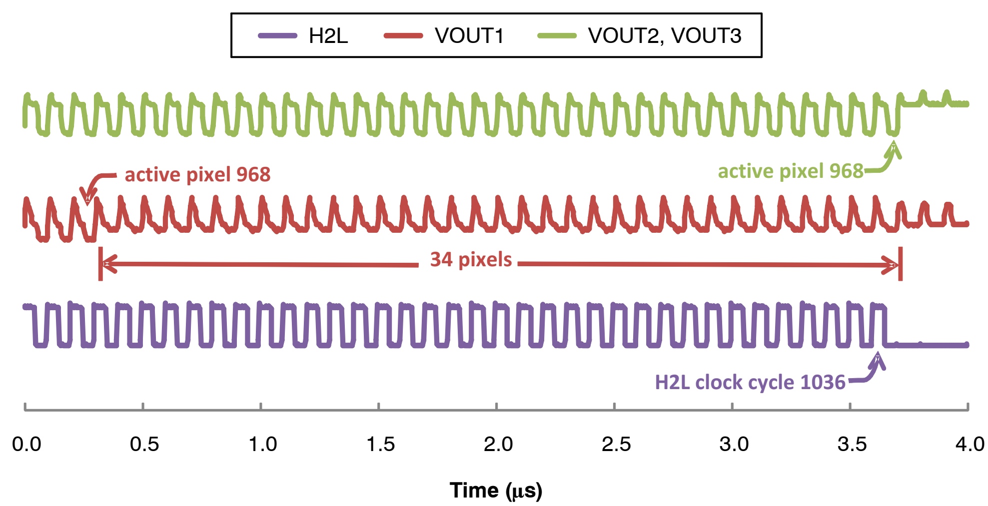


Figure 40. Video Output at End of Each Line for Dual or Quad Output Modes

VCCD Timing

Table 16. TIMING DEFINITIONS

Symbol	Note	Minimum	Nominal	Maximum	Units
t_{VA}	VCCD Transfer Time A	0.46	0.50	0.50	μs
t_{VB}	VCCD Transfer Time B	0.46	1.30	7.50	μs
t_{SUB}	Electronic Shutter Pulse	1.0	1.5	10.0	μs
t_3	Photodiode to VCCD Transfer Time	1.0	1.5	5.0	μs

V1, V2, V3, V4 Alignment

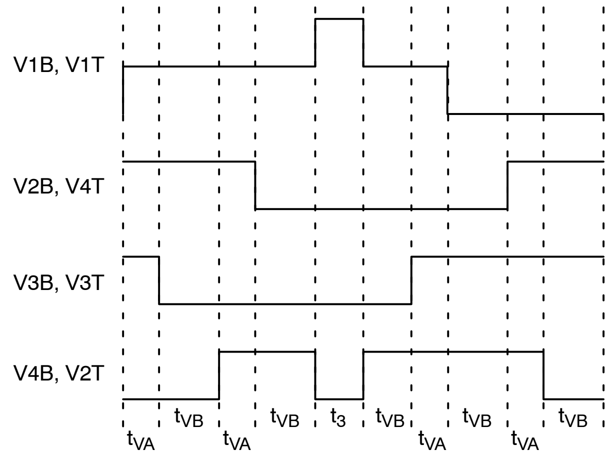


Figure 41. Timing Pattern F1. VCCD Frame Timing to Transfer Charge from Photodiodes to the VCCD when Using the Bottom HCCD, Outputs A or B

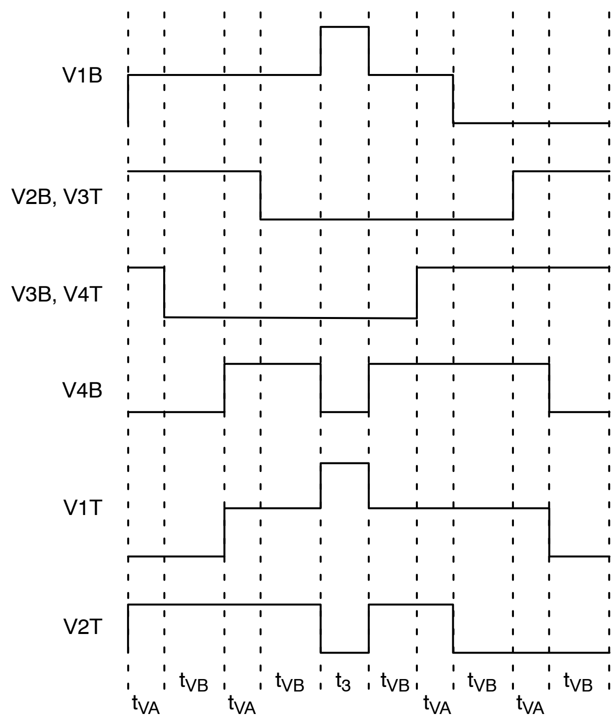


Figure 42. Timing Pattern F2. VCCD Frame Timing to Transfer Charge from Photodiodes to the VCCD when Using All Four Outputs in Quad Mode

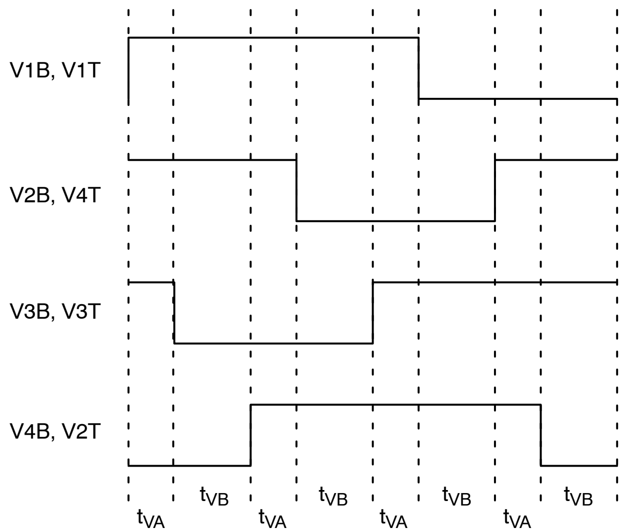


Figure 43. Line Timing L1. VCCD Line Timing to Transfer One Line of Charge from VCCD to the HCCD when Using the Bottom HCCD, Outputs A or B in Single or Dual Output Modes

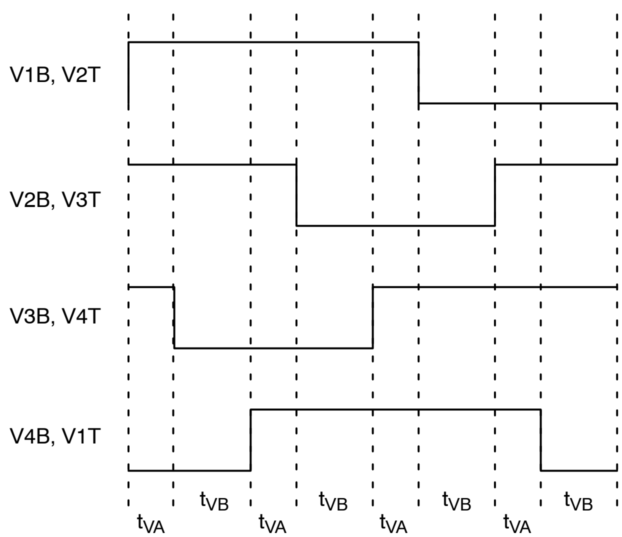
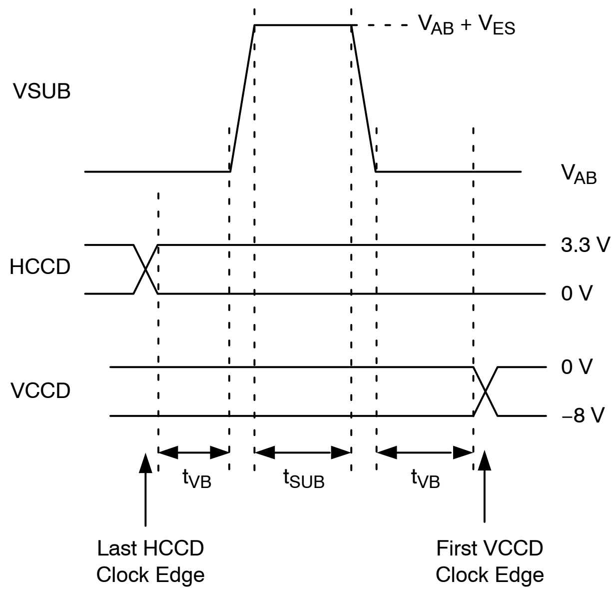


Figure 44. Line Timing L2. VCCD Line Timing to Transfer One Line of Charge from VCCD to the HCCD when Using All Four Outputs in Quad Mode

Electronic Shutter



WARNING: Do not clock the EMCCD register while the electronic shutter pulse is high.

Figure 45. Electronic Shutter Timing Pattern S1

Clock	State
H1S	High
H2S	Low
H2SW	Low
H2L	Low
H2X	Low
H1SEM	High
H1BEM	High
H2SEM	Low
H2BEM	Low

Figure 46. The State of the HCCD and EMCCD Clocks during the Frame, Line, and Electronic Shutter Timing Sequences

HCCD Timing

To reverse the direction of charge transfer in a Horizontal CCD, exchange the timing pattern of the H1B and H2B inputs of that HCCD. If a HCCD is not used, hold all of its gates at the high level.

When operating in single or dual output modes, the VDD23cd, VDD1c, and VDD1d amplifiers must still be powered. The outputs VOUT1, VOUT2, and VOUT3 for quadrants c and d may be left unloaded.

Table 17. HCCD TIMING

Mode	HCCD a, b Timing	HCCD c, d Timing
Single	H1Ba = H2Bb = H1Sa = H1Sb H2Ba = H1Bb = H2Sa = H2Sb	3.3 V
Dual	H1Ba = H1Bb = H1Sa = H1Sb H2Ba = H2Bb = H2Sa = H2Sb	3.3 V
Quad	H1Ba = H1Bb = H1Sa = H1Sb H2Ba = H2Bb = H2Sa = H2Sb	H1Bc = H1Bd = H1Sc = H1Sd H2Bc = H2Bd = H2Sc = H2Sd

Image Exposure and Readout

The flowchart for image exposure and readout is shown in Figure 47. The electronic shutter timing may be omitted to obtain an exposure time equal to the image read out time. NEXP is the number of lines exposure time and NV is the number of VCCD clock cycles (row transfers).

Table 18. IMAGE EXPOSURE AND READOUT

Mode	NH	NV	Line Timing	Frame Timing	Pixel Timing
Single	2,072	1,124	L1	F1	P1
Dual	1,036	562	L1	F1	P1
Quad	1,036	562	L2	F2	P1

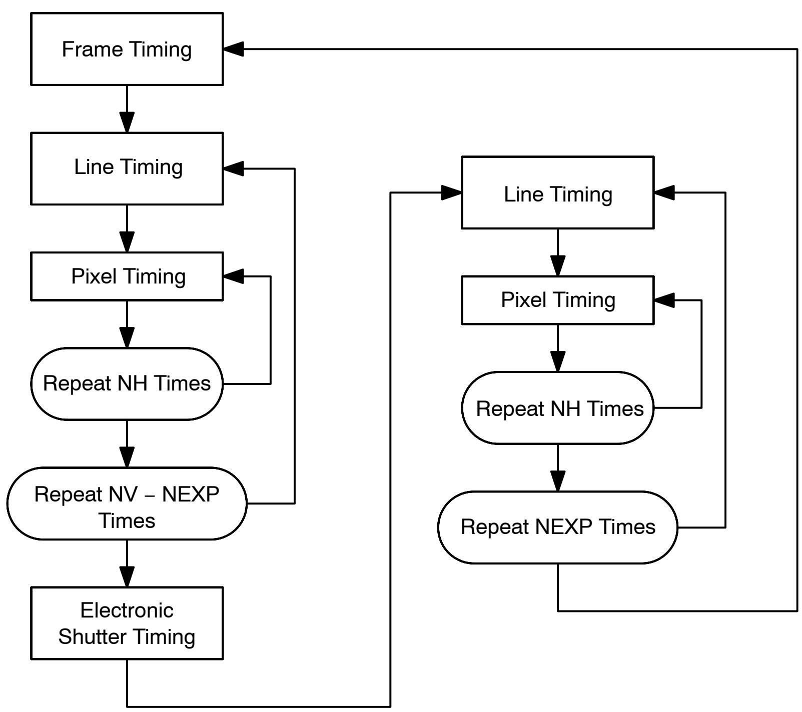


Figure 47. The Image Readout Timing Flow Chart

Long Integrations and Readout

For extended integrations the output amplifiers need to be powered down. When powered up, the output amplifiers emit near infrared light that is sensed by the photodiodes. It will begin to be visible in images of 30 second integrations or longer.

To power down the output amplifiers set VDD1 and VSS1 to 0 V, and VDD23 to +5 V. Do not set VDD23 to 0 V during the integration of an image. During the time the VDD2 supply is reduced to +5 V the substrate voltage reference output SUBV will be invalid. For cameras with long integration times, the value of SUBV will have to digitized by and ADC and stored at the time when VDD23 is +15 V. The SUB pin voltage would be set by a DAC. The HCCD and EMCCD may be continue to clock during integration. If they are stopped during integration then the EMCCD should be re-started at +7 V to flush out any undesired signal before increasing the voltage to charge multiplying levels.

The timing flow chart for long integration time is shown in Figure 48.

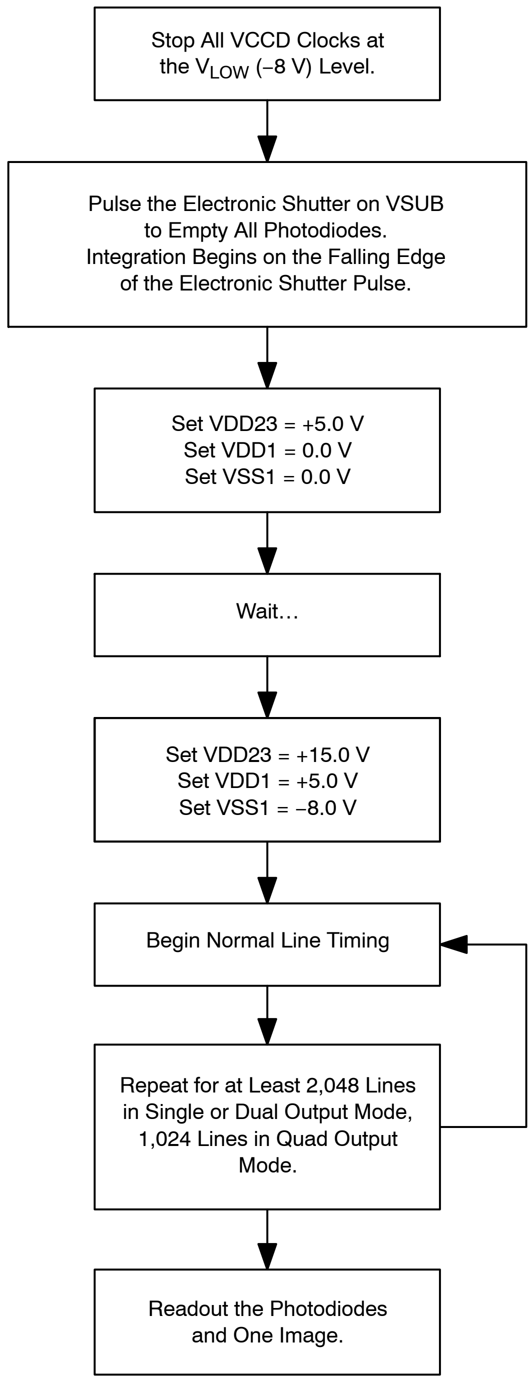


Figure 48. Timing Flow Chart for Long Integration Time

THERMOELECTRIC COOLER

As a step toward ensuring availability of high quality TECs for cooled image sensors, ON Semiconductor has adopted a dual source strategy. Fit and function have been verified equivalent. Customers may notice differences in the appearance of components.

Representative performance plots for the TEC are shown below:

Performance Plots of PGA Integrated TEC

For the performance plots below, the TEC was operated at maximum pulse width (DC mode) to maintain the cold side (sensor) temperature at 0°C, while the input signal to the EMCCD register of each or the four outputs was 20 mV, the EMCCD gain was 20X, and the horizontal clock rate was 20 MHz.

The recommended maximum input current (Imax) is 1.1 A, requiring an input voltage (Vmax) of 11.2 V, but the optimum current and voltage needed for a given temperature gradient may be lower.

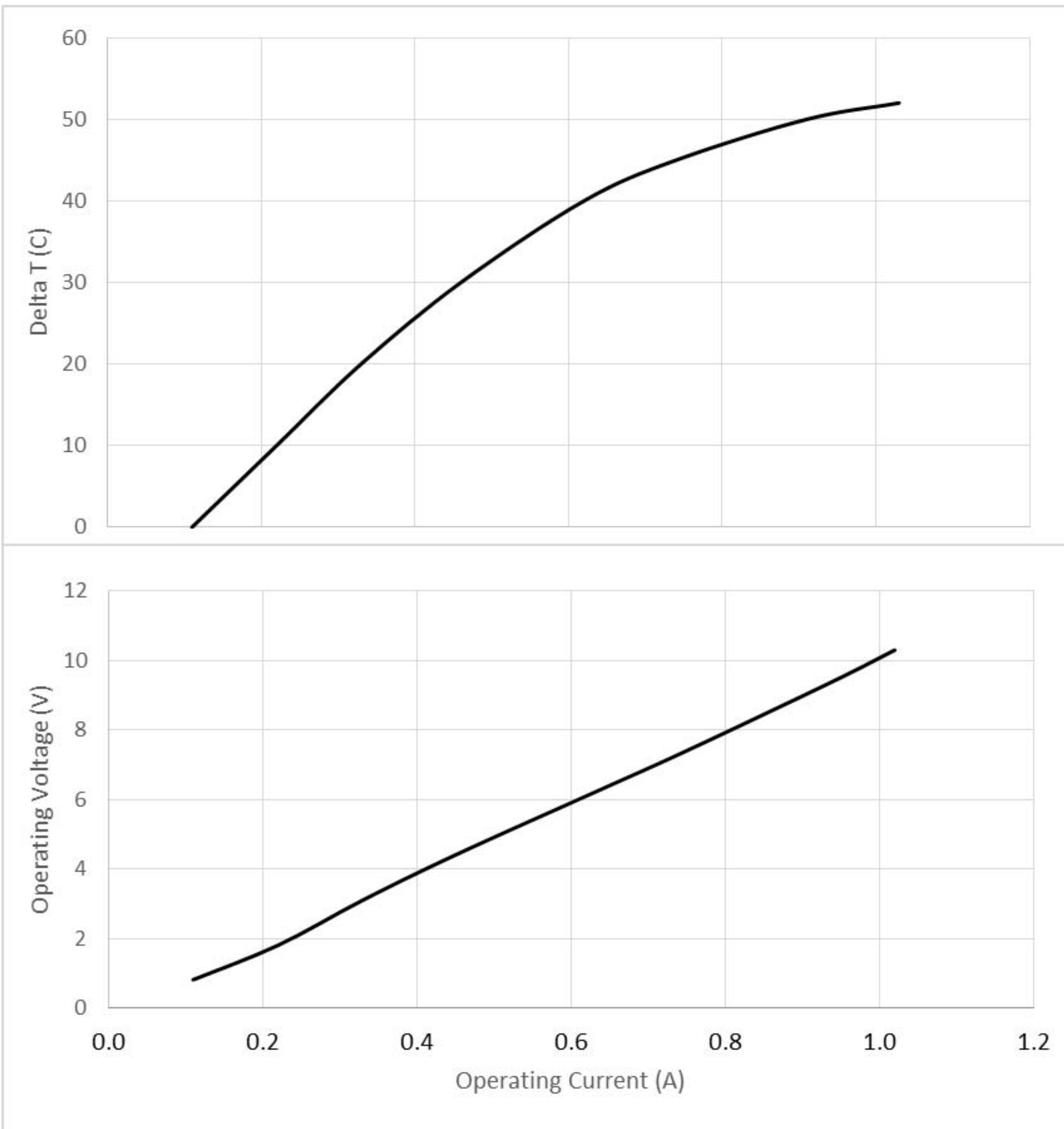


Figure 49. PGA with Integrated TEC, Temperature Gradient and Required Voltage vs. Applied Current

Performance Plots of Thermistor in PGA with Integrated TEC

The thermoelectric cooler (TEC) has an on−board thermistor with ±3% tolerance, and 10 kΩ (Ro) at 25°C (298K, T_o). Its performance follows the equation shown below, where T= temperature in °K, over the range of 233 to 398 °K, RT = thermistor resistance in ohms:

$$T = \frac{1}{\left\{(7.96 \times 10^{-4}) + (2.67 \times 10^{-4}) \times \ln(R_T) + (1.21 \times 10^{-7}) \times [\ln(R_T)]^3\right\}}$$

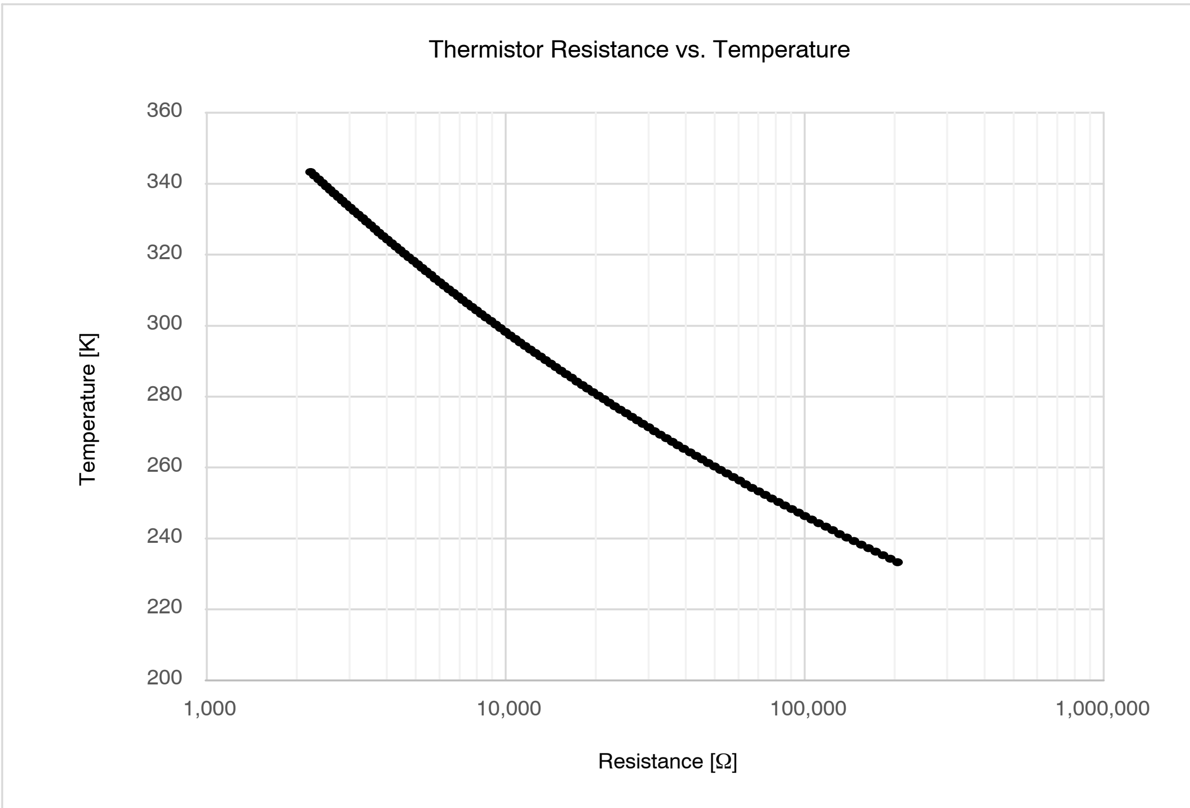


Figure 50. PGA with Integrated TEC, Thermistor Performance Plots of Thermistor in PGA with Integrated TEC

STORAGE AND HANDLING

Table 19. STORAGE CONDITIONS

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_{ST}	−55	80	°C	1
Humidity	RH	5	90	%	2, 3

1. Long-term storage toward the maximum temperature will accelerate color filter degradation.
2. T = 25°C. Excessive humidity will degrade MTF. The maximum humidity for storage is 50% for OPNs beginning with KAE−02152−ABB−SD, KAE−02152−FBB−SD, and KAE−02152−QBB−SD.
3. For the sensors with an integrated TEC, storage in a dry environment is recommended to avoid moisture ingress and possible condensation on the sensor when the device is cooled.

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from www.onsemi.com.

For information on environmental exposure, please download the *Using Interline CCD Image Sensors in High Intensity Lighting Conditions* Application Note (AND9183/D) from www.onsemi.com.

For information on soldering recommendations, please download the Soldering and Mounting Techniques Reference Manual (SOLDERRM/D) from www.onsemi.com.

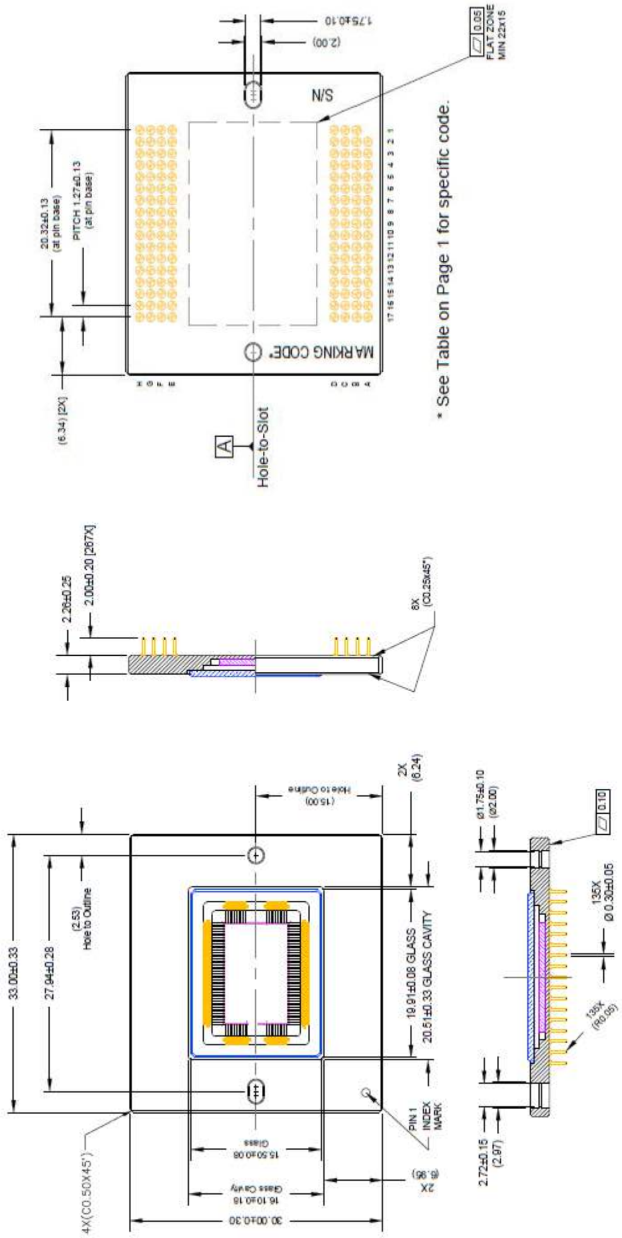
For quality and reliability information, please download the *Quality & Reliability* Handbook (HBD851/D) from www.onsemi.com.

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from www.onsemi.com.

For information on Standard terms and Conditions of Sale, please download Terms and Conditions from www.onsemi.com.

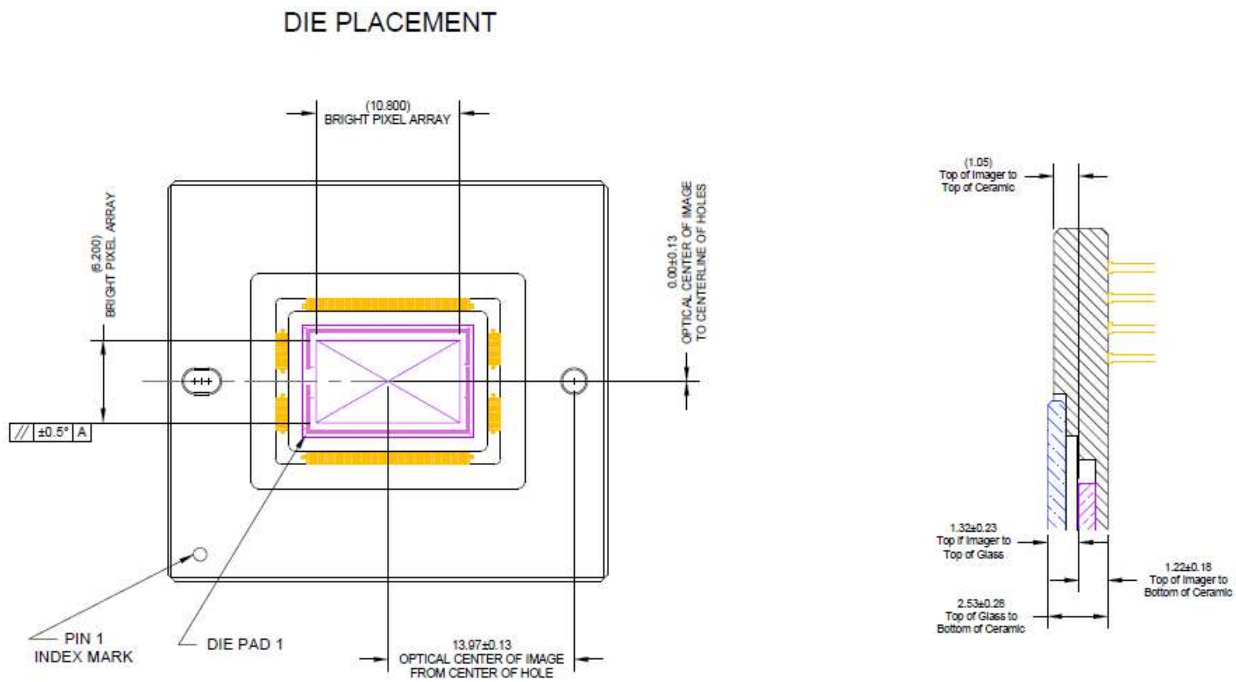
MECHANICAL INFORMATION

PGA Completed Assembly (no TEC)



Notes:
1. Substrate is a 141-pin ceramic PGA package.
2. Body is black alumina.
3. Pins are Kovar or equivalent, plated with 1.00 microns of gold over 2.00 microns of nickel.
4. Wire is wedge bonded aluminum (1% Si).
5. Ablebond 967−1 epoxy for die attach.
6. No materials to obstruct the clearance through the package holes.
7. Exposed metal is 1.00 micron minimum gold over 2.00 micron minimum nickel.
8. Glass lid is Schott E263Teco, n_D 1.5231. Thickness 0.76 ± 0.05 mm.
9. Recommended mounting screws: 1.6 × 0.35 mm (ISO standard), 0−80 (unified fine thread standard).
10. See Ordering Information for Marking Code.
11. Pin to pin distances are measured at the pin base.
12. Units: mm

Figure 51. PGA Completed Assembly (1/2, no TEC)

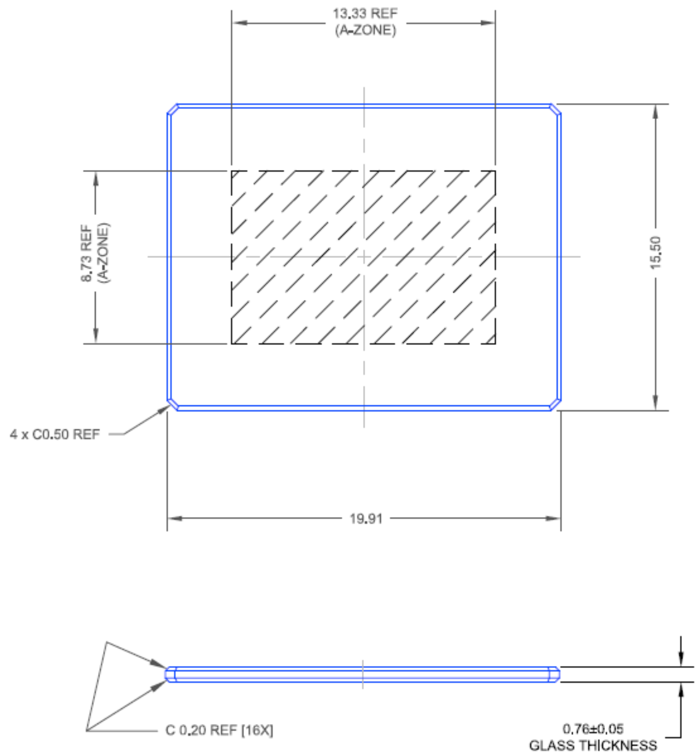


Notes:

1. Die is standard thickness for 150 mm silicon wafer: 0.675 ± 0.020 mm.
2. Singulated die is approximately 12.910 × 8.500 mm, for a 50 micron saw kerf.
3. The optical center of the image area is at the center of the die and the center of the package.
4. Units: mm

Figure 52. PGA Completed Assembly (2/2, no TEC)

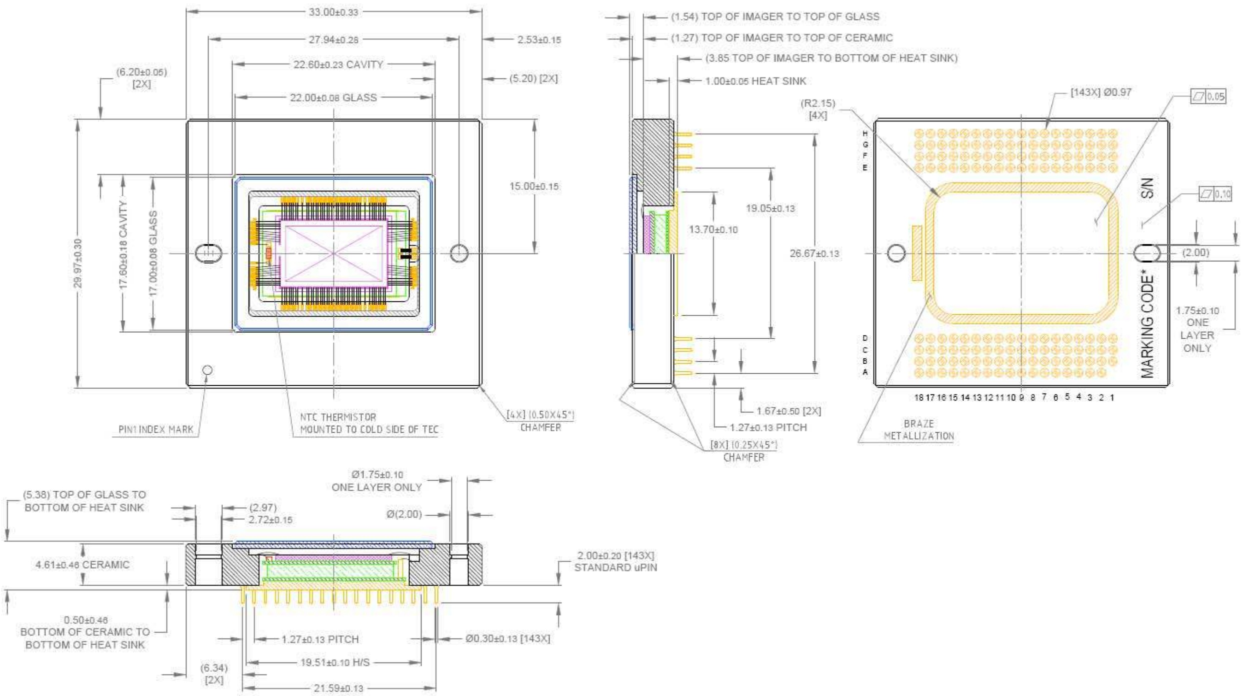
Clear Cover Glass for PGA (no TEC)



Notes:
1. Glass Material: Schott D263T eco
2. Units: mm

Figure 53. Clear Cover Glass for PGA (no TEC)

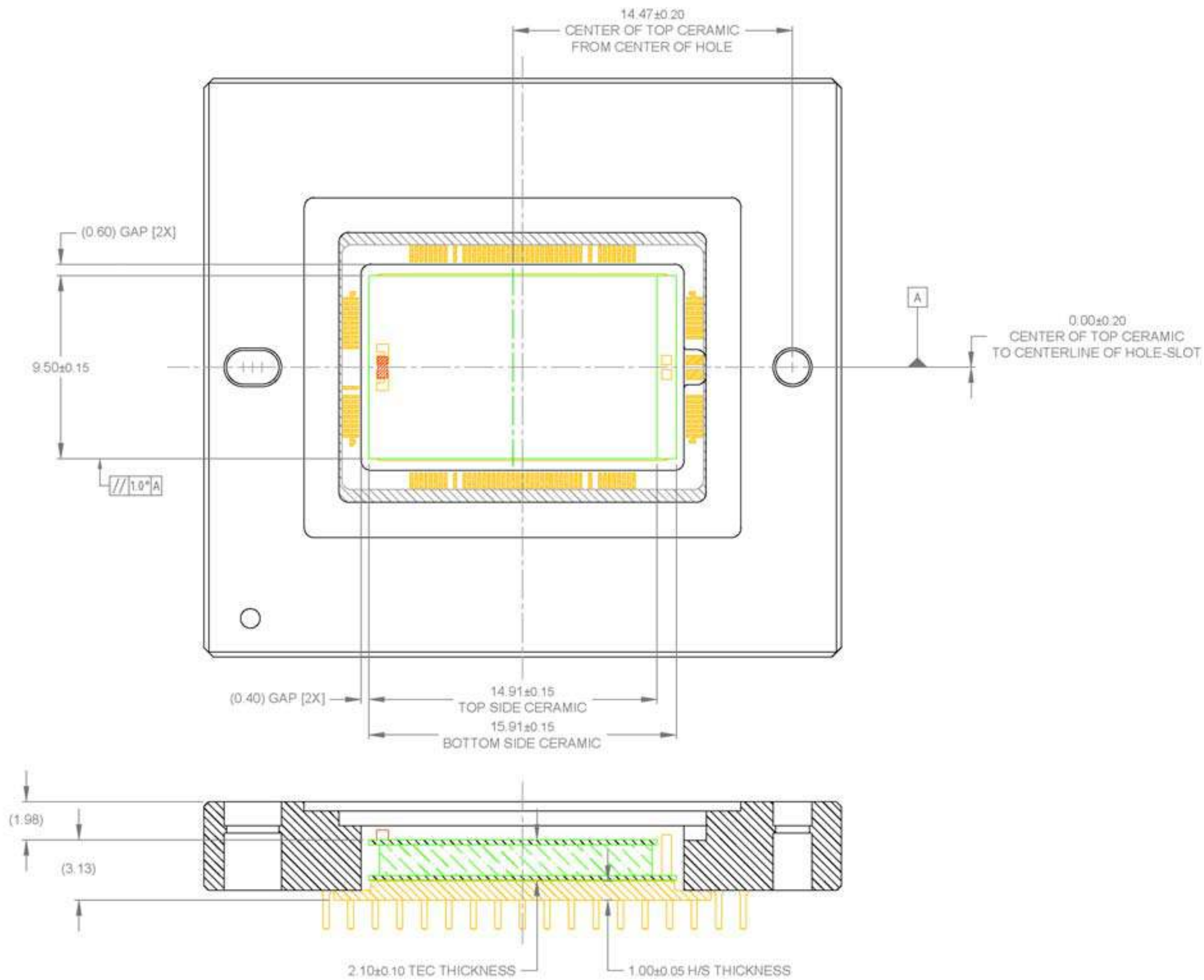
PGA Completed Assembly with Integrated TEC



Notes:

1. See Ordering Information for Marking Code.
2. Pin to pin distances are measured at the pin base.
3. No material to interfere with clearance through package holes.
4. Units: mm

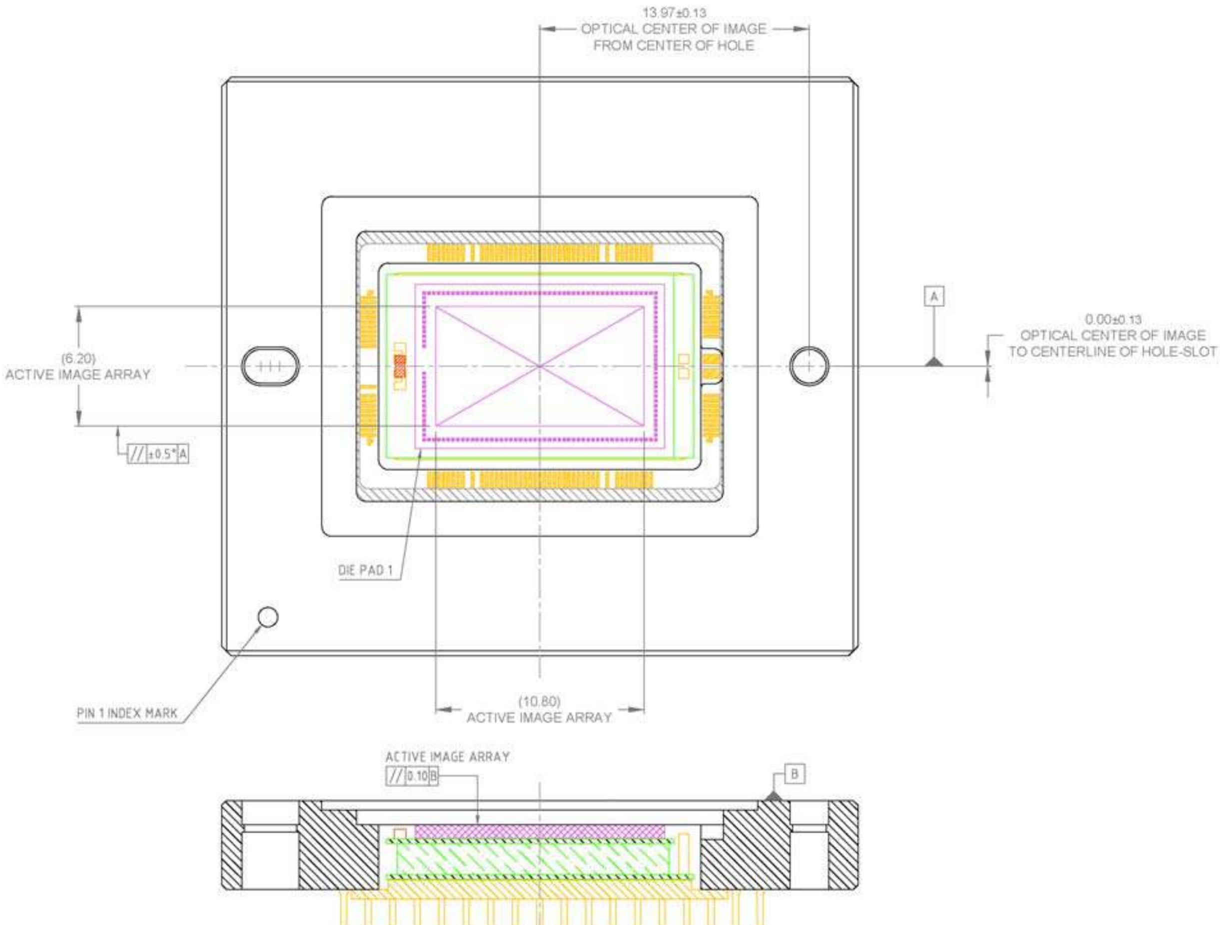
Figure 54. PGA Completed Assembly with Integrated TEC (1 of 3)



Notes:

1. Units: mm

Figure 55. PGA Completed Assembly with Integrated TEC – TEC Placement (2 of 3)

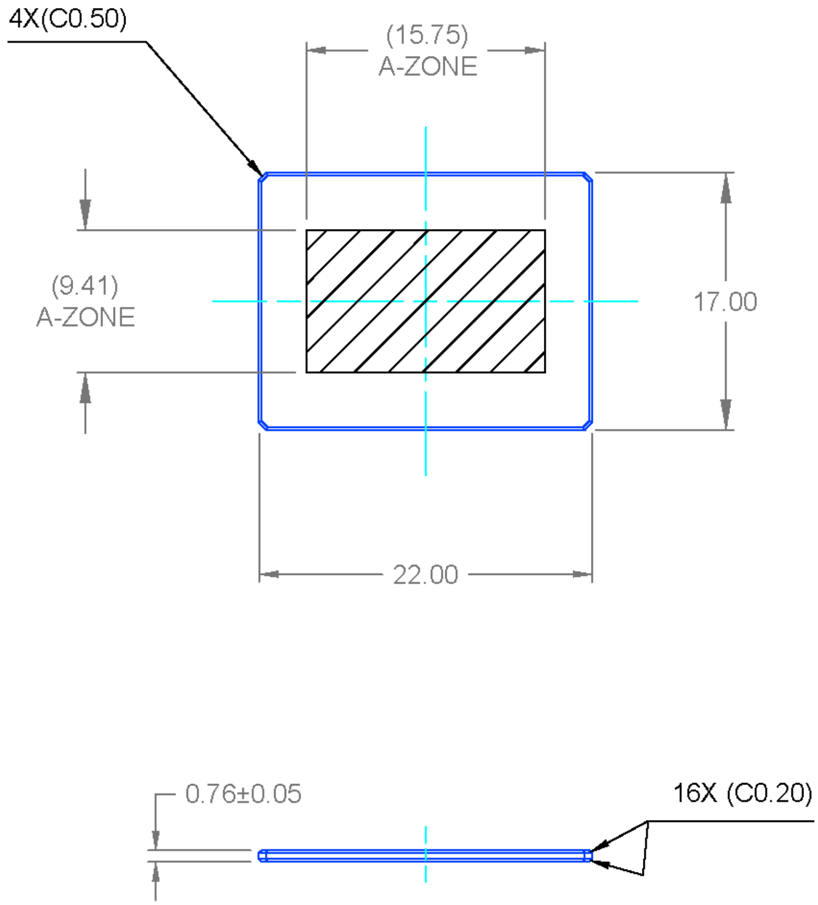


Notes:

1. The optical center of the image is at the center of the die and nominally at the center of the package.
2. Datum −A− is through the center of the package holes.
3. Units: mm

Figure 56. PGA Completed Assembly with Integrated TEC – Die Placement (3 of 3)

Clear Cover Glass for PGA with Integrated TEC



Notes:
1. Substrate = Schott D263T eco
2. No epoxy
3. Units: mm

Figure 57. Clear Cover Glass for PGA with Integrated TEC

MAR Cover Glass for PGA with Integrated TEC

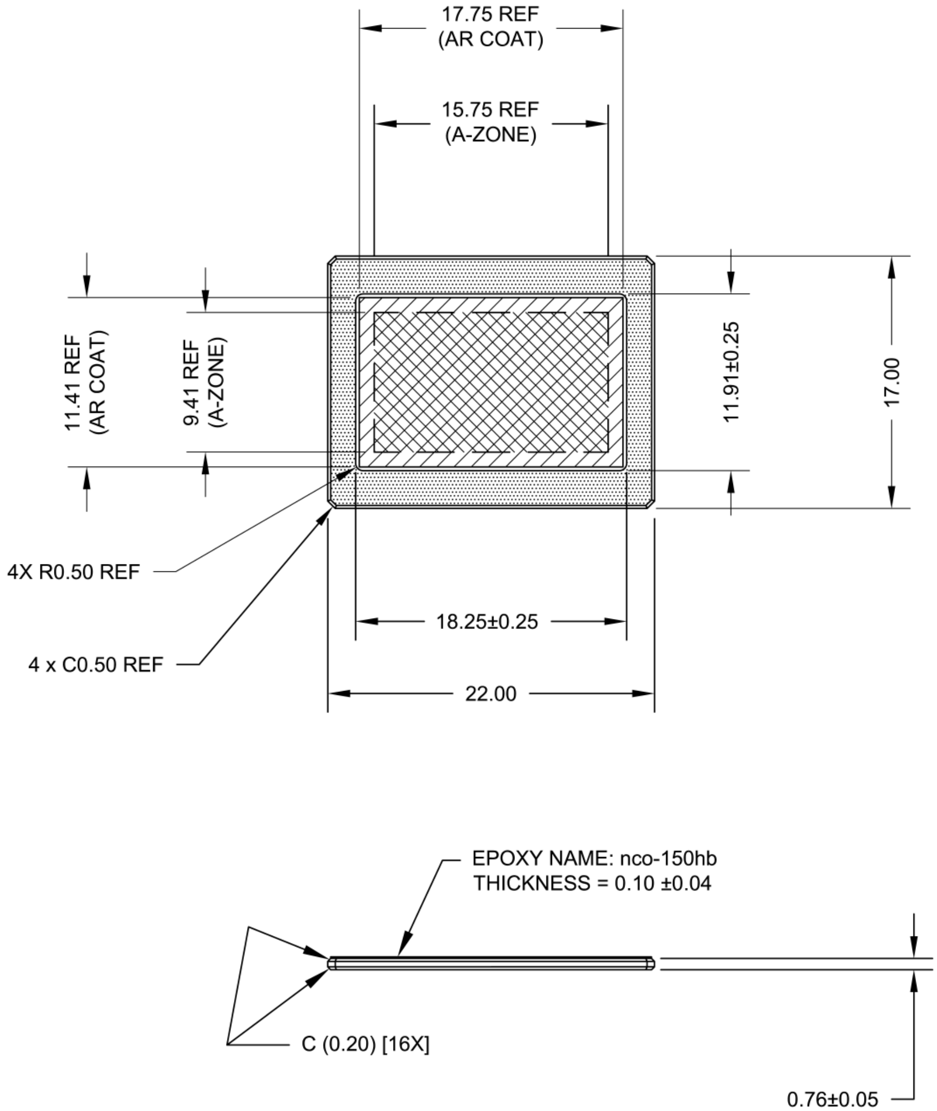


Figure 58. MAR Cover Glass for PGA with Integrated TEC

Notes:

1. Substrate = Schott D263T eco
2. Dust, Scratch, Inclusion Specification: 10μm maximum size in Zone A
3. MAR coated both sides
4. Spectral Transmission
   - T > 98.0% 420−435 nm
   - T > 99.2% 435−630 nm
   - T > 98.0% 630−680 nm
5. Units: mm

Cover Glass Transmissions

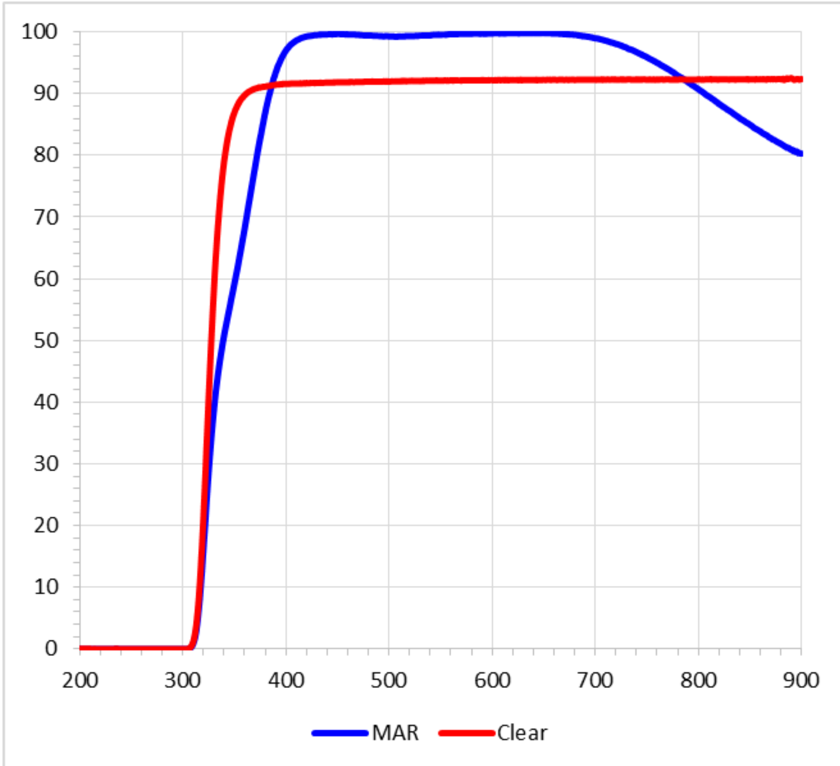


Figure 59. Cover Glass Transmission

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