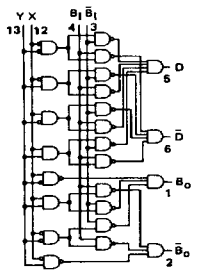
MC1021
MC1221

Provides the DIFFERENCE, $\overline{\text{DIFFERENCE}}$, BORROW OUT, and $\overline{\text{BORROW OUT}}$ functions while requiring only MINUEND (X) and SUBTRAHEND (Y) inputs with BORROW IN and $\overline{\text{BORROW IN}}$.

POSITIVE LOGIC



$D = YXB_I + Y\bar{X}\bar{B}_I + \bar{Y}XB_I + \bar{Y}\bar{X}B_I$

$\bar{D} = \bar{Y}\bar{X}\bar{B}_I + \bar{Y}XB_I + Y\bar{X}B_I + YXB_I$

$B_O = \bar{Y}\bar{X}B_I + \bar{Y}X\bar{B}_I + Y\bar{X}B_I + YXB_I$

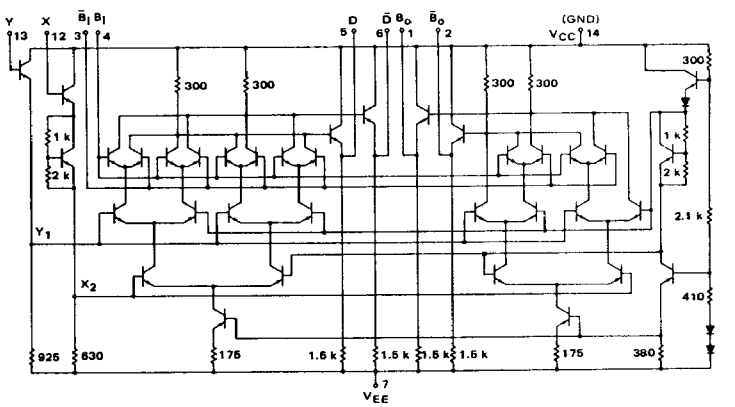
$\bar{B}_O = \bar{Y}\bar{X}\bar{B}_I + \bar{Y}X\bar{B}_I + \bar{Y}XB_I + YX\bar{B}_I$

DC Input Loading Factor: X, Y = 1 B_I, $\bar{B}_I$ = 2
DC Output Loading Factor = 25
Power Dissipation = 145 mW typical

TRUTH TABLE

INPUT LOGIC LEVEL				OUTPUT LOGIC LEVEL			
X	Y	B_I	$\bar{B}_I$	D	$\bar{D}$	B_O	$\bar{B}_O$
0	0	0	1	0	1	0	1
0	0	1	0	1	0	1	0
0	1	0	1	1	0	1	0
0	1	1	0	0	1	1	0
1	0	0	1	1	0	0	1
1	0	1	0	0	1	0	1
1	1	0	1	0	1	0	1
1	1	1	0	1	0	1	0

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC1221 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC1021 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	I_E	7	-	-	-	35	-	-	mAdc	-	-	-	35	-	-	mAdc
Input Current	$2\,I_{in}$	3	-	-	-	200	-	-	μAdc	-	-	-	200	-	-	μAdc
	$2\,I_{in}$	4	-	-	-	200	-	-		-	-	-	200	-	-	
	$1.5\,I_{in}$	12	-	-	-	150	-	-		-	-	-	150	-	-	
	$1.5\,I_{in}$	13	-	-	-	150	-	-		-	-	-	150	-	-	
Input Leakage Current	I_R	12	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc
		13	-	-	-	0.2	-	1.0		-	-	-	0.2	-	1.0	
		3	-	-	-	1.0	-	5.0		-	-	-	1.0	-	5.0	
		4	-	-	-	1.0	-	5.0		-	-	-	1.0	-	5.0	
"DIFFERENCE" Logic "1" Output Voltage‡	V_{OH}‡	5	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"DIFFERENCE" Logic "0" Output Voltage	V_{OL}	5	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
"BORROW" Logic "1" Output Voltage‡	V_{OH}‡	1	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"BORROW" Logic "0" Output Voltage	V_{OL}	1	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
Switching Times			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Minuend Input Propagation Delay	t_{12-5+}	5	9.0	14	8.0	13	9.0	16.5	ns	8.0	13	8.0	13	8.0	13	ns
	t_{12+5-}	5	8.0	13	8.0	13.5	11	17		8.0	13.5	8.0	13.5	9.0	15	
	t_{12-1+}	1		14	7.0	12.5	9.0	14.5		7.0	12.5	7.0	12.5	8.0	13	
	t_{12+1-}	1		13.5	8.0	13.5	11	17		8.0	13.5	8.0	13.5	9.0	15	
Rise Time	t_{5+}	5		13	9.0	14	10	14		9.0	14	9.0	14	9.0	14	
	t_{1+}	1		13	7.0	12	9.0	14		7.0	12	7.0	12	8.0	13	
Fall Time	t_{5-}	5	5.0	8.0	5.0	8.5	7.0	11.5		5.0	8.5	5.0	8.5	6.0	9.5	
	t_{1-}	1	5.0	8.0	5.0	8.0	7.0	11.0		5.0	8.0	5.0	8.0	6.0	9.0	
Subtrahend Input Propagation Delay	t_{13+5-}	5	5.0	8.5	5.0	8.5	7.0	13	ns	5.0	8.5	5.0	8.5	6.0	9.5	ns
	t_{13-5+}		6.0	9.0	5.0	8.5	7.0	11.5		5.0	8.5	5.0	8.5	6.0	9.0	
Rise Time	t_{5+}		5.0	8.5	6.0	9.0	8.0	11		6.0	9.0	6.0	9.0	7.0	9.5	
Fall Time	t_{5-}		5.0	8.5	5.0	8.5	7.0	11		5.0	8.5	5.0	8.5	6.0	9.5	
Borrow Input Propagation Delay	t_{4-5+}	5	3.0	5.5	3.0	5.0	4.0	6.0	ns	3.0	5.0	3.0	5.0	3.0	5.0	ns
	t_{4+5-}		4.0	7.5	4.0	7.5	6.0	10		4.0	7.5	4.0	7.5	5.0	8.5	
Rise Time	t_{5+}		5.0	8.0	6.0	8.5	8.0	10.5		6.0	8.5	6.0	8.5	7.0	10	
Fall Time	t_{5-}		5.0	8.0	5.0	8.5	7.0	11		5.0	8.5	5.0	8.5	6.0	9.5	

‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

* V_{OH} and V_{OL} limits apply only if not more than one input (pin 3, 4, 12 or 13) is at a Threshold Voltage ($V_{IL\ max}$ or $V_{IH\ min}$). Conduct tests with one input at a Threshold Voltage and apply appropriate $V_{OL\ max}$ or $V_{OH\ min}$ voltages to all other inputs.

	@Test Temperature	TEST VOLTAGE/CURRENT VALUES Vdc ± 1.0%						mAdc	
		$V_{IL\ min}$ to $V_{IL\ max}$	$V_{OL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{OH\ min}$	$V_{IH\ max}$	V_{EE}	I_L	
MC1221	−55°C	-5.2 to -1.405	-1.580	-1.165 to -0.825	-0.990	-	-5.2	-2.5	
	+25°C	-5.2 to -1.325	-1.500	-1.025 to -0.700	-0.850	-0.200	-5.2	-2.5	
	+125°C	-5.2 to -1.205	-1.380	-0.875 to -0.530	-0.700	-	-5.2	-2.5	
MC1021	0°C	-5.2 to -1.350	-1.520	-1.070 to -0.740	-0.895	-	-5.2	-2.5	
	+25°C	-5.2 to -1.325	-1.500	-1.025 to -0.700	-0.850	-0.700	-5.2	-2.5	
	+75°C	-5.2 to -1.260	-1.435	-0.950 to -0.615	-0.775	-	-5.2	-2.5	

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: $V_{IL\ min}$ to $V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7	3	4	-	7,12,13	-	14
Input Current	$2\ I_{in}$	3	4,12,13		3	7	-	14
	$2\ I_{in}$	4	3,12,13		4		-	
	$1.5\ I_{in}$	12	3,13	4	12		-	
	$1.5\ I_{in}$	13	3,12	4	13		-	
Input Leakage Current	I_R	12	4	3	-	7,12,13	-	14
		13	4	3	-	7,12,13	-	
		3	-	4	-	3,7,12,13	-	
		4	-	3	-	4,7,12,13	-	
"DIFFERENCE" Logic "1" Output Voltage‡	V_{OH}‡	5	3, 12, 13* 4, 13* 4, 12* 3*	4* 3, 12* 3, 13* 4, 12, 13*	- - - -	7	5	14
"DIFFERENCE" Logic "0" Output Voltage	V_{OL}	5	4, 12, 13* 3, 13* 3, 12* 4*	3* 3, 12* 3, 13* 3, 12, 13*	- - - -	7	- - - -	14
"BORROW" Logic "1" Output Voltage‡	V_{OH}‡	1	3, 12, 13* 3, 12* 4, 12* 3*	4* 4, 13* 3, 13* 4, 12, 13*	- - - -	7	1	14
"BORROW" Logic "0" Output Voltage	V_{OL}	1	4, 12, 13* 4, 13* 3, 13* 4*	3* 3, 12* 4, 12* 3, 12, 13*	- - - -	7	- - - -	14
Switching Times			Pulse In	Pulse Out		$V_{EE} = -4.0$ Vdc		+1.2V
Minuend Input Propagation Delay	t_{12-5+}	5	12	5	-	7	-	14
	t_{12+5-}	5		5	-		-	
	t_{12-1+}	1		1	-		-	
	t_{12+1-}	1		1	-		-	
Rise Time	t_{5+}	5		5	-		-	
	t_{1+}	1		1	-		-	
Fall Time	t_{5-}	5		5	-		-	
	t_{1-}	1		1	-		-	
Subtrahend Input Propagation Delay	t_{13+5-}	5	13	5	-	7	-	14
	t_{13-5+}				-		-	
Rise Time	t_{5+}				-		-	
Fall Time	t_{5-}				-		-	
Borrow Input Propagation Delay	t_{4-5+}	5	4	5	-	7	-	14
	t_{4+5-}				-		-	
Rise Time	t_{5+}				-		-	
Fall Time	t_{5-}				-		-	

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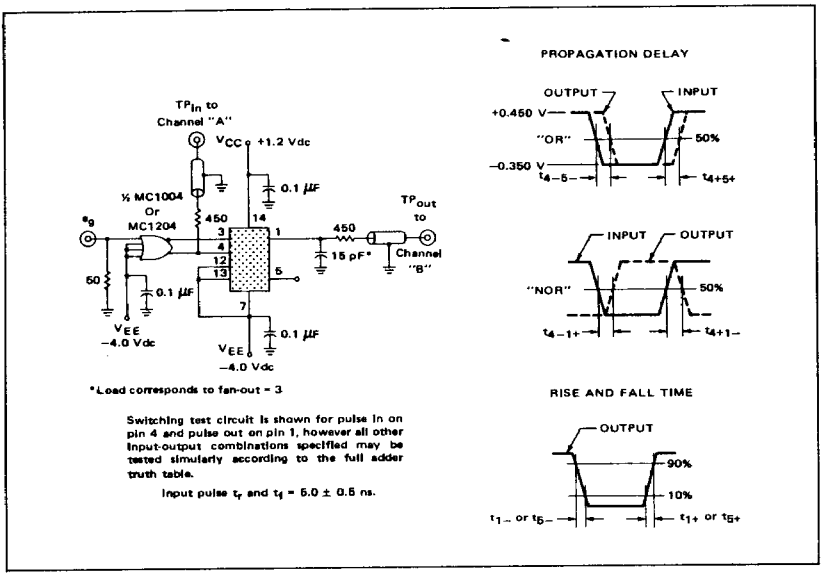
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



Switching test circuit is shown for pulse in on pin 4 and pulse out on pin 1, however all other input-output combinations specified may be tested simularly according to the full adder truth table.

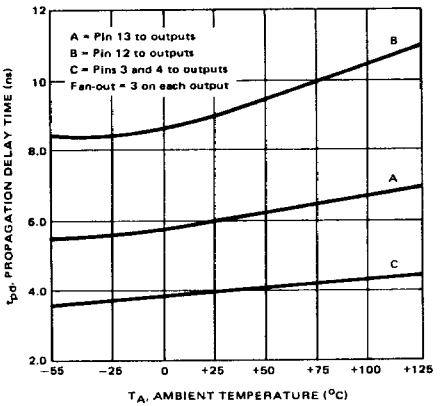
Input pulse t_r and t_f = 5.0 ± 0.5 ns.

APPLICATIONS INFORMATION

The MC1021/MC1221 full subtractor is identical to the full adder except for the interconnection metalization. It exhibits an average propagation delay time of 5.0 ns per stage in a system employing ripple Borrow. This device permits building of ripple-through dividers.

The schematic of the full subtractor illustrates the techniques employed to obtain the necessary logic equations. A compensated current source drives a transistor "tree" with three levels of branching. The X input is translated negative two levels, to switch current between either the left or right branch of the tree. The Y input is translated negative one level to switch current at the second level of branching. Depending upon the eight possible combinations of inputs, one specific branch level in the Difference generating tree will be carrying current. Thus the proper output state is determined. The Borrow generating tree operates in the same manner. This series gating technique results in the best speed-power product obtainable with bipolar technology. Typical propagation delay times from the inputs to outputs are shown.

TYPICAL PROPAGATION DELAY TIMES



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