TL317 100-mA 3-Terminal Adjustable Positive Voltage Regulator

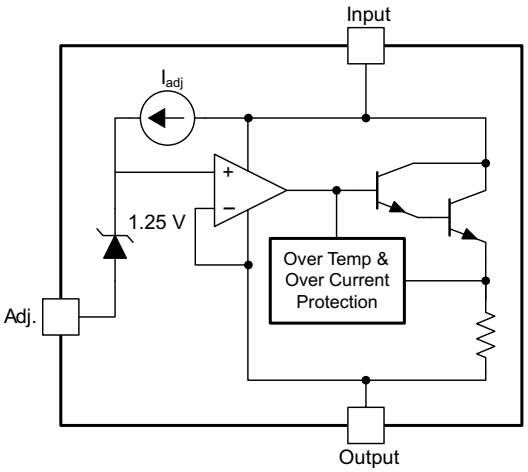
1 Features

- Output Voltage Range Adjustable From 1.25 V to 32 V When Used With an External Resistor Divider
- Output Current Capability of 100 mA
- Input Regulation Typically 0.01% Per Input-Voltage Change
- Output Regulation Typically 0.5%
- Ripple Rejection Typically 80 dB

2 Applications

- Power Supplies
- Portable Devices
- Computing and Servers
- Telecommunications
- HVAC: Heating, Ventilation, and Air Conditioning
- Desktop PC
- Digital Signage
- Programmable Logic Controller
- Appliances

Functional Block Diagram



3 Description

The TL317 is an adjustable three-terminal positive-voltage regulator capable of supplying 100 mA over an output-voltage range of 1.25 V to 32 V. It is exceptionally easy to use and requires only two external resistors to set the output voltage.

This regulator offers full overload protection available only in integrated circuits. Included on the chip are current-limiting and thermal-overload protection. All overload-protection circuitry remains fully functional, even when ADJUSTMENT is disconnected. Normally, no capacitors are required unless the device is situated far from the input filter capacitors, in which case an input bypass is required. An optional output capacitor can be added to improve transient response. ADJUSTMENT can be bypassed to achieve very high ripple rejection.

In addition to replacing fixed regulators, the TL317 regulator is useful in a wide variety of other applications. Because the regulator is floating and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input-to-output differential is not exceeded. Its primary application is that of a programmable output regulator, but by connecting a fixed resistor between ADJUSTMENT and OUTPUT, this device can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping ADJUSTMENT to ground, programming the output to 1.25 V, where most loads draw little current.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TL317D	SOIC (8)	4.90 mm × 3.90 mm
TL317PW	TSSOP (8)	4.30 mm × 3.00 mm
TL317PS	SOP (8)	6.20 mm × 5.30 mm
TL317LP	TO-92 (3)	4.83 mm × 3.68 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (September 2011) to Revision I **Page**

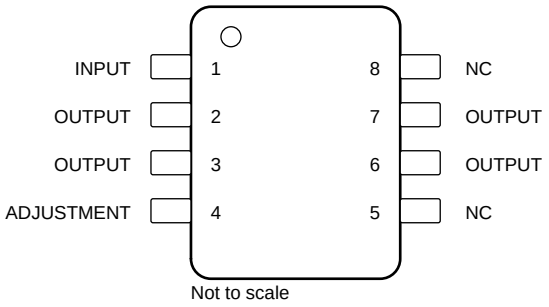
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted *Ordering Information* table, see POA at the end of the datasheet ... 3

Changes from Revision G (September 2009) to Revision H **Page**

- Changed datasheet format from QuickSilver to DocZone ... 1
- Changed low end output voltage range from 1.2 V to 1.25 ... 1
- Added MIN value of 2.5 V for $V_I - V_O$ parameter in the Recommended Operating Conditions table ... 4

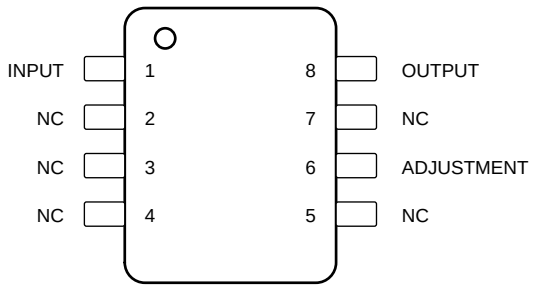
5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Not to scale

PS Package
8-Pin SOP
Top View



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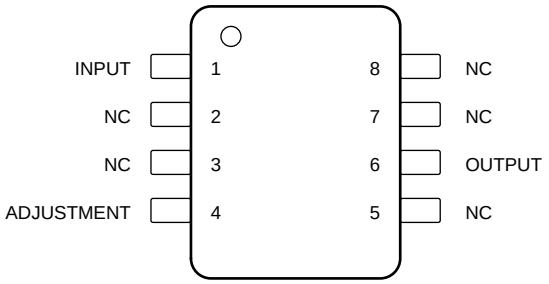
PW Package
8-Pin TSSOP
Top View



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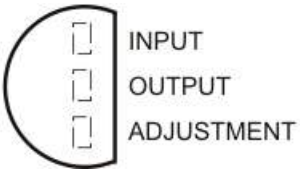
LP Package
3-Pin TO-92
Top View



Pin Functions

PIN					I/O	DESCRIPTION
NAME	SOIC	TSSOP	SOP	TO-92		
ADJUSTMENT	4	4	6	3	—	Supply reference voltage
INPUT	1	1	1	1	I	Input supply voltage
NC	5, 8	2, 3, 5, 7, 8	2, 3, 4, 5, 7	—	—	No internal connection
OUTPUT	2, 3, 6, 7	6	8	2	O	Output voltage, output terminals are all internally connected.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Input-to-output differential voltage, $V_I - V_O$		35	V
Operating virtual-junction temperature, T_J		150	°C
Storage temperature range, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000(3)	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) Tested on PW package.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
$V_I - V_O$	Input-to-output voltage differential		2.5		35	V
I_O	Output current		2.5		100	mA
T_J	Operating virtual-junction temperature	TL317C	0		125	°C
		TL317	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TL317				UNIT
		D (SOIC)	PW (TSSOP)	PS (SOP)	LP (TO-92)	
		8 PINS	8 PINS	8 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	109.9	170	115.3	157.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.8	51	67.1	81.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58.5	101.5	64.4	—	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.5	3.7	27.7	25.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	57.9	99.1	63.5	137.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating virtual-junction temperature range (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input voltage regulation(2)	$V_I - V_O$ = 5 V to 35 V	T_J = 25°C		0.01%	0.02%	V
		I_O = 2.5 mA to 100 mA		0.02%	0.05%	
Ripple regulation	V_O = 10 V, f = 120 Hz			65		dB
	V_O = 10 V, 10-µF capacitor between ADJUSTMENT and ground		66	80		
Output voltage regulation	V_I = 5 V to 35 V, I_O = 2.5 mA to 100 mA, T_J = 25°C	$V_O \le 5$ V		25		mV
		$V_O \ge 5$ V		5		mV/V
	V_I = 5 V to 35 V, I_O = 2.5 mA to 100 mA	$V_O \le 5$		50		mV
		$V_O \ge 5$ V		10		mV/V
Output voltage change with temperature	T_J = 0°C to 125°C			10		mV/V
Output voltage long-term drift	After 1000 hours at T_J = 125°C and $V_I - V_O$ = 35 V			3	10	mV/V
Output noise voltage	f = 10 Hz to 10 kHz, T_J = 25°C			30		µV/V
Minimum output current to maintain regulation	$V_I - V_O$ = 35			1.5	2.5	mA
Peak output current	$V_I - V_O \le 35$ V		100	200		mA
ADJUSTMENT current				50	100	µA
Change in ADJUSTMENT current	$V_I - V_O$ = 2.5 V to 35 V, I_O = 2.5 mA to 100 mA			0.2	5	µA
Reference voltage (output to ADJUSTMENT)	I_O = 2.5 mA to 100 mA, $V_I - V_O$ = 5 V to 35 V, P ≤ rated dissipation		1.2	1.25	1.3	V

(1) Unless otherwise noted, these specifications apply for the following test conditions: $V_I - V_O$ = 5 V and I_O = 40 mA. Pulse-testing techniques must be used that maintain the junction temperature as close to the ambient temperature as possible. All characteristics are measured with a 0.1-µF capacitor across the input and a 1-µF capacitor across the output.
(2) Input voltage regulation is expressed here as the percentage change in output voltage per 1-V change at the input.

6.6 Typical Characteristic

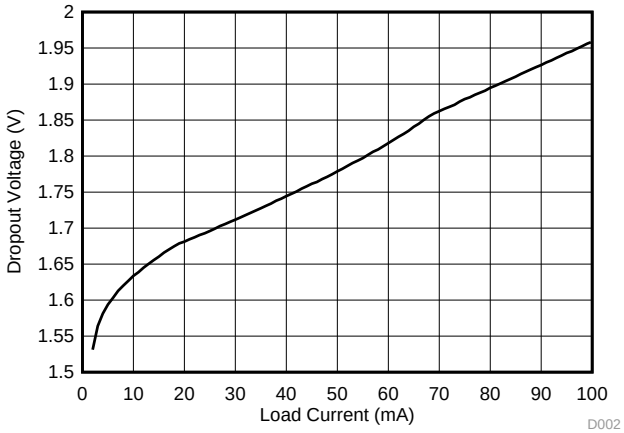


Figure 1. Dropout Voltage vs Load Current (T_J = 25°C)

7 Detailed Description

7.1 Overview

The TL317 device is an adjustable three-terminal positive-voltage regulator capable of supplying up to 100 mA over an output-voltage range of 1.25 V to 32 V. It requires only two external resistors to set the output voltage. The TL317 device is versatile in its applications, including uses in programmable output regulation and local on-card regulation. Also, by connecting a fixed resistor between the ADJUSTMENT and OUTPUT terminals, the TL317 device can function as a precision current regulator. An optional output capacitor can be added to improve transient response. The ADJUSTMENT terminal can be bypassed to achieve very high ripple-rejection ratios, which are difficult to achieve with standard three-terminal regulators.

7.2 Functional Block Diagrams

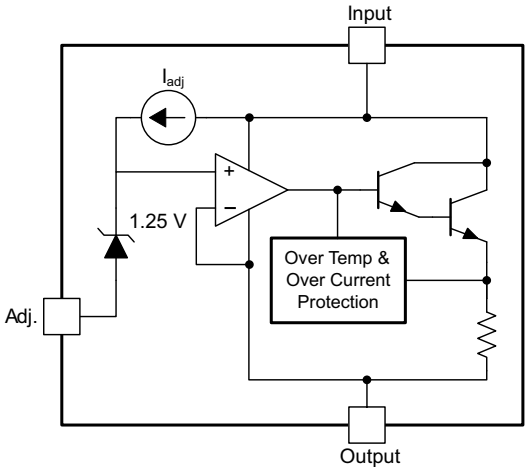
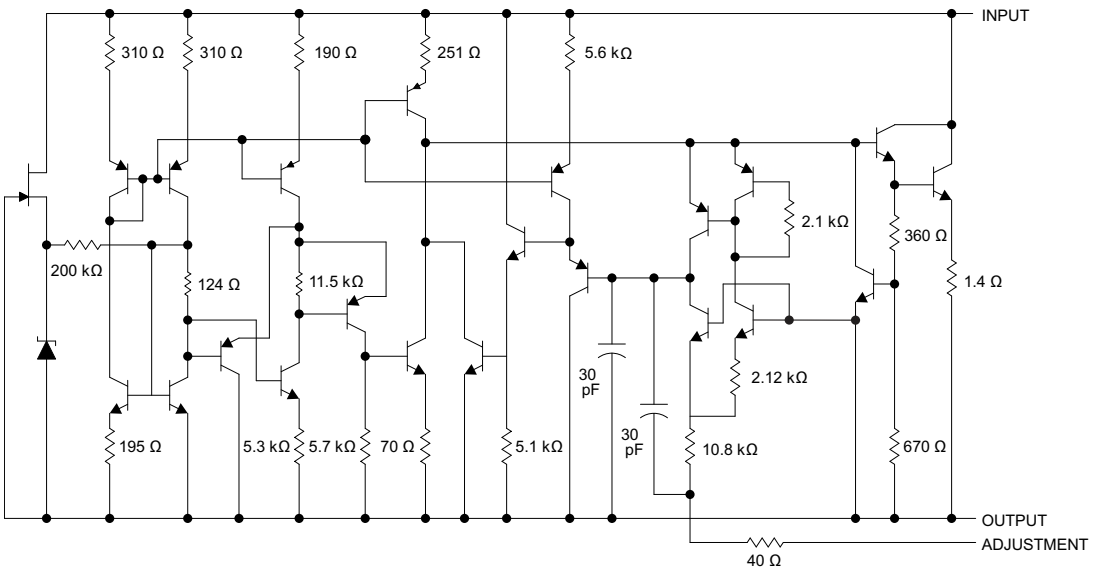


Figure 2. Equivalent Schematic



All component values shown are nominal

Figure 3. Detailed Schematic

7.3 Feature Description

7.3.1 NPN Darlington Output Drive

NPN Darlington output topology provides naturally low output impedance and an output capacitor is optional.

7.3.2 Programmable Feedback

An internal amplifier with 1.25-V offset input at the ADJUSTMENT terminal provides easy output voltage or current (not both) programming. For current regulation applications, a single resistor whose resistance value is 1.25 V / I_O and power rating is greater than $(1.25\ V)^2$ / R must be used. For voltage regulation applications, two resistors set the output voltage as described in *Adjustable Voltage Regulator*.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device OUTPUT pin sources current necessary to make the OUTPUT pin 1.25 V greater than the ADJUSTMENT pin to provide output regulation

7.4.2 Operation With Low Input Voltage

The device requires 2.5 V of headroom (VI – VO) to regulate the OUTPUT. With less headroom, the OUTPUT voltage of the device may be below the desired setpoint.

7.4.3 Operation in Light Loads

The device passes its bias current to the OUTPUT pin. The load or feedback must consume this minimum current for regulation or the output may be too high. The minimum current require to regulate is provided in the *Electrical Characteristics*, so the series resistance used to set the output voltage is recommended to be V_O / I_{MIN} to ensure regulation at all times.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The flexibility of the TL317 allows it to be configured to take on many different functions in DC power applications.

8.2 Typical Applications

8.2.1 Adjustable Voltage Regulator

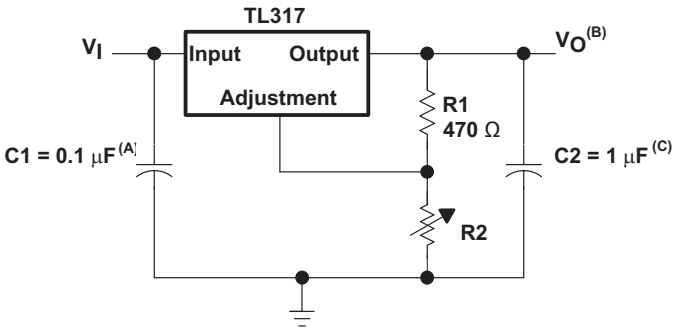


Figure 4. Adjustable Voltage Regulator

8.2.1.1 Design Requirements

- R1 and R2 are required to set the output voltage.
- C1 is recommended, particularly if the regulator is not in close proximity to the power-supply filter capacitors. A 0.1-µF ceramic or 1-µF tantalum capacitor provides sufficient bypassing for most applications, especially when adjustment and output capacitors are used.
- Use of an output capacitor, C2, improves transient response, but is optional.

8.2.1.2 Detailed Design Procedure

V_O is calculated as shown in Equation 1. I_{ADJ} is typically 50 µA and negligible in most applications.

Power dissipation for linear regulators is calculated as shown in Equation 2. I_{ADJ} is typically 50 µA and negligible in most applications, so a typical way to calculate power dissipation for linear regulators is simplified to Equation 3.

$$V_O = V_{REF} (1 + R2 / R1) + (I_{ADJ} \times R2) \quad (1)$$

$$P = (V_I - V_O) \times I_O + (V_I - V_{ADJ}) \times I_{ADJ} \quad (2)$$

$$P = (V_I - V_O) \times I_O \quad (3)$$

Typical Applications (continued)

8.2.1.3 Application Curve

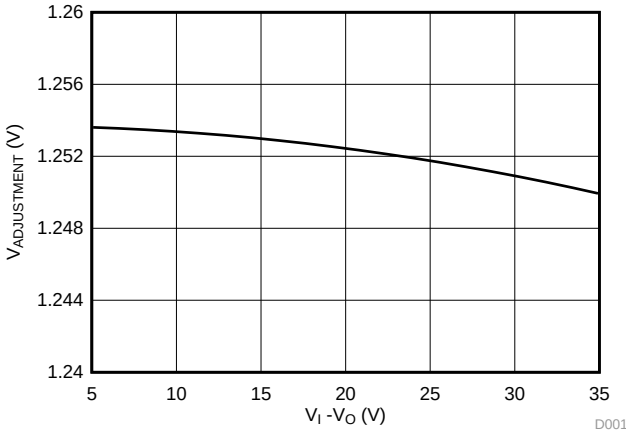


Figure 5. Line Regulation

8.2.2 0-V to 30-V Regulator Circuit

V_O is calculated as shown in Equation 4, where V_{ref} equals the difference between OUTPUT and ADJUSTMENT voltages (approximately 1.25 V).

$$V_{OUT} = V_{REF}\left(1 + \frac{R_2 + R_3}{R_1}\right) - 10\,V \tag{4}$$

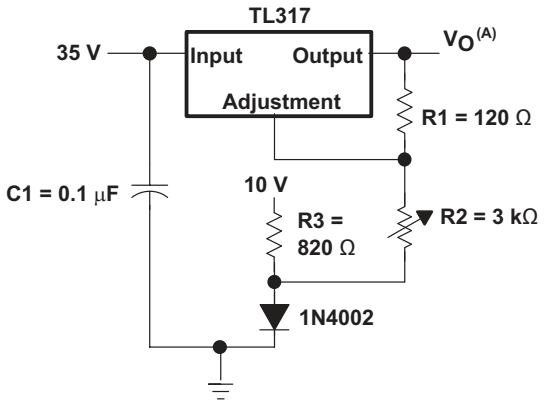


Figure 6. 0-V to 30-V Regulator Circuit Schematic

Typical Applications (continued)

8.2.3 Regulator Circuit With Improved Ripple Rejection

- Protection diode D1 is recommended if C2 is used. The diode provides a low-impedance discharge path to prevent the capacitor from discharging into the output of the regulator
- Use of an output capacitor, C2, improves transient response, but is optional.

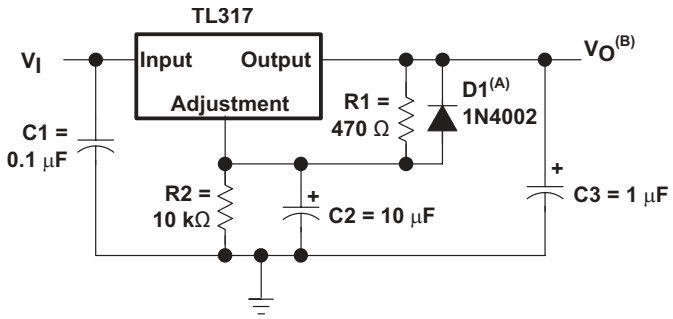


Figure 7. Regulator Circuit With Improved Ripple Rejection Schematic

8.2.4 Precision Current-Limiter Circuit

The use of the TL317 in this configuration limits the output current to I_{limit} shown in Figure 8.

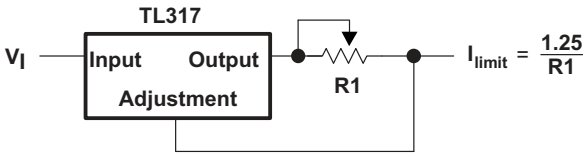


Figure 8. Precision Current-Limiter Circuit

8.2.5 Tracking Preregulator Circuit

This application keeps a constant voltage across the second TL317 in the circuit.

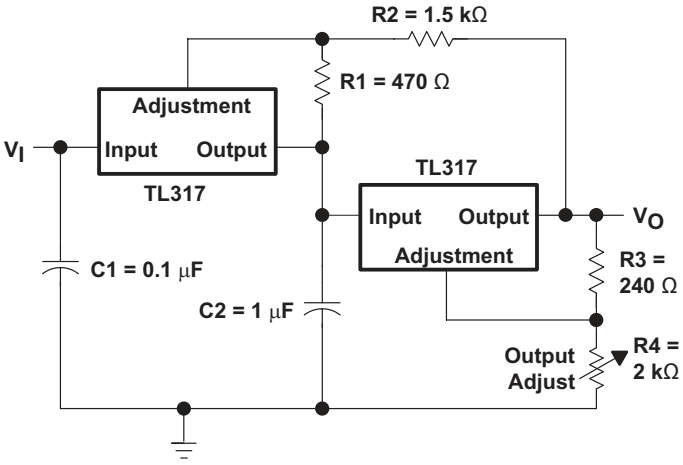


Figure 9. Tracking Preregulator Circuit Schematic

Typical Applications (continued)

8.2.6 Slow-Turnon 15-V Regulator Circuit

The capacitor C1, in combination with the PNP transistor, helps the circuit to slowly start supplying voltage. In the beginning, the capacitor is not charged. Therefore, output voltage starts at V_{C1}+ V_{BE} + 1.25 V = 0 V + 0.65 V + 1.25 V = 1.9 V. As the capacitor voltage rises, V_{OUT} also rises at the same rate. When the output voltage reaches the value determined by R1 and R2, the PNP is turned off.

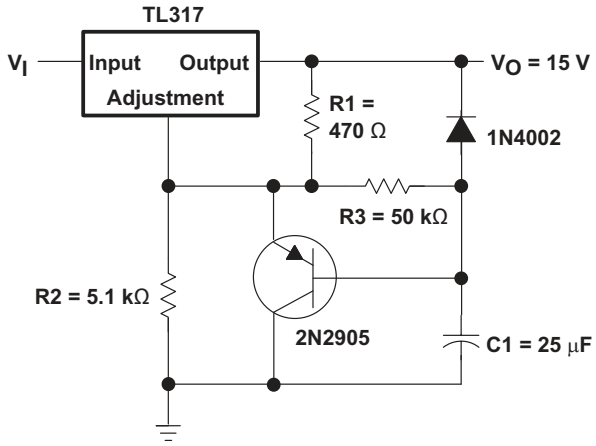


Figure 10. Slow-Turnon 15-V Regulator Circuit Schematic

8.2.7 50-mA Constant-Current Battery-Charger Circuit

The current limit operation mode can be used to trickle charge a battery at a fixed current. I_{CHG} = 1.25 V / 24 Ω. V_I must be greater than V_{BAT} + 4.25 V (1.25 V [V_{REF}] + 3 V [headroom]).

Power dissipation through resistor R1 is calculated as shown in Equation 5, so a resistor with the appropriate power rating must be chosen for this application.

$$P(R1) = I_O^2 \times R1[\Omega] \quad (5)$$

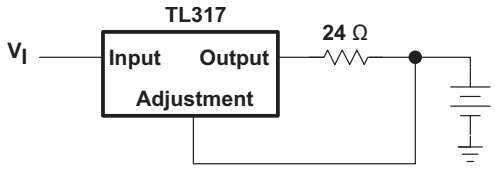


Figure 11. 50-mA Constant-Current Battery-Charger Circuit

Typical Applications (continued)

8.2.8 Current-Limited 6-V Charger

As the charge current increases, the voltage at the bottom resistor increases until the NPN starts sinking current from the adjustment pin. The voltage at the adjustment pin drops, and consequently the output voltage decreases until the NPN stops conducting.

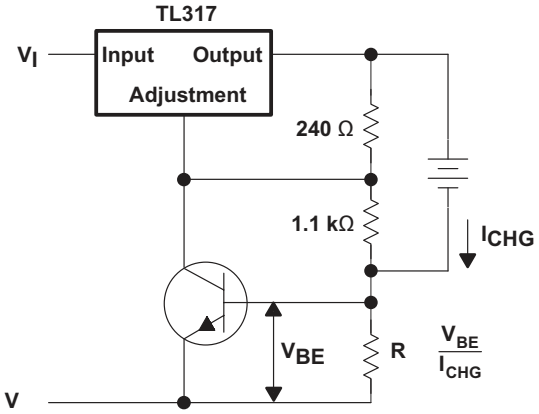
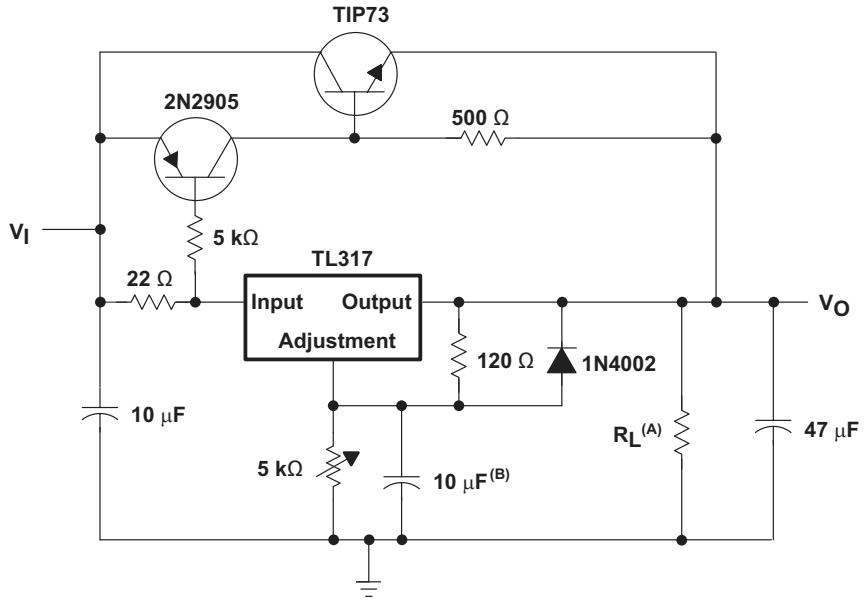


Figure 12. Current-Limited 6-V Charger Schematic

8.2.9 High-Current Adjustable Regulator

The NPNs at the top of the schematic allow higher currents at V_{OUT} than the LM317 can provide, while still keeping the output voltage at levels determined by the adjustment pin resistor divider of the LM317.



A. Minimum load current is 30 mA.

B. Optional capacitor improves ripples rejection.

Figure 13. High-Current Adjustable Regulator Schematic

9 Power Supply Recommendations

The TL317 is designed to operate from an input voltage supply range between 1.25 V to 35 V greater than the output voltage. If the device is more than six inches from the input filter capacitors, an input bypass capacitor, 0.1-µF (or greater), of any type is required for stability.

10 Layout

10.1 Layout Guidelines

- It is recommended that the input terminal be bypassed to ground with a bypass capacitor.
- The optimum placement for the bypass capacitor is closest to the input terminal of the device and the system GND. Take care to minimize the loop area formed by the bypass-capacitor connection, the input terminal, and the system GND.
- For operation at full rated load, it is recommended to use wide trace lengths to eliminate I × R drop and heat dissipation.

10.2 Layout Example

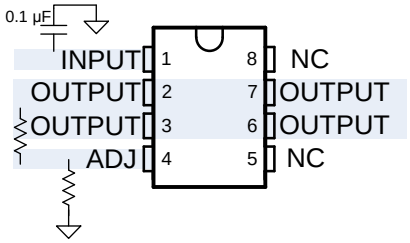


Figure 14. TL317D Layout Example

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL317CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	TL317C	Samples
TL317CDE4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	TL317C	Samples
TL317CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 125	TL317C	Samples
TL317CDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	TL317C	Samples
TL317CDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	TL317C	Samples
TL317CLP	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	TL317C	Samples
TL317CLPE3	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	TL317C	Samples
TL317CLPR	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	TL317C	Samples
TL317CLPRE3	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	TL317C	Samples
TL317CPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 125	T317	Samples
TL317PS	ACTIVE	SO	PS	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T317	Samples
TL317PSR	LIFEBUY	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T317	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

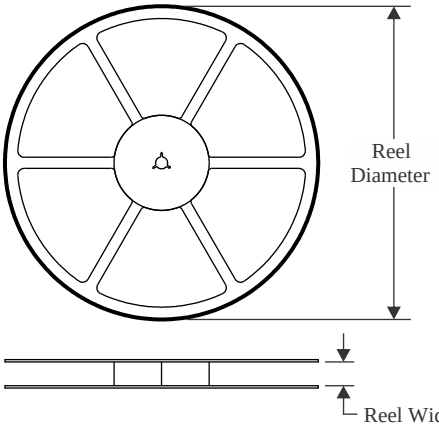
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

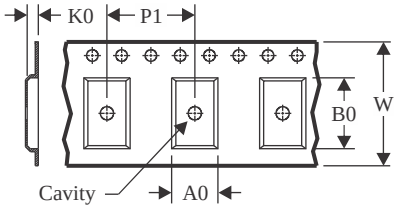
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

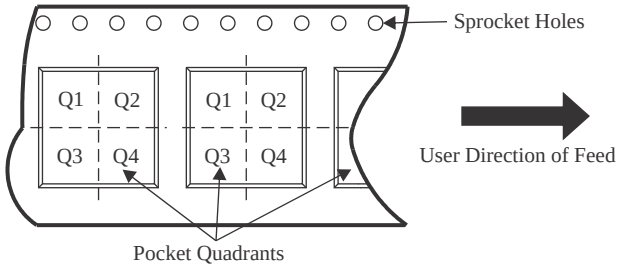


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

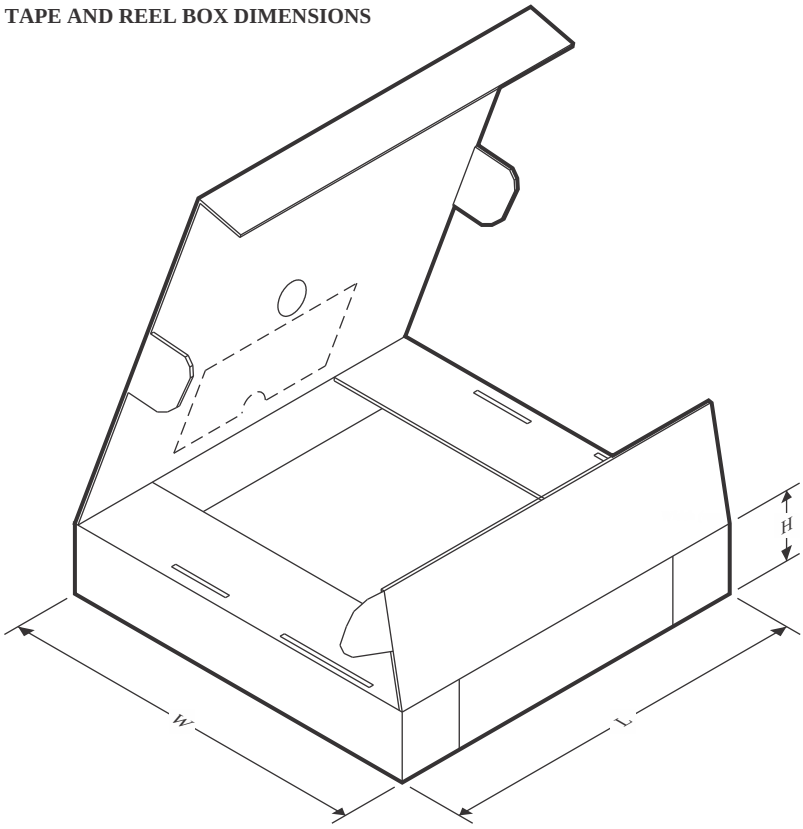
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL317CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL317CDR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
TL317CDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL317CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL317PSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1

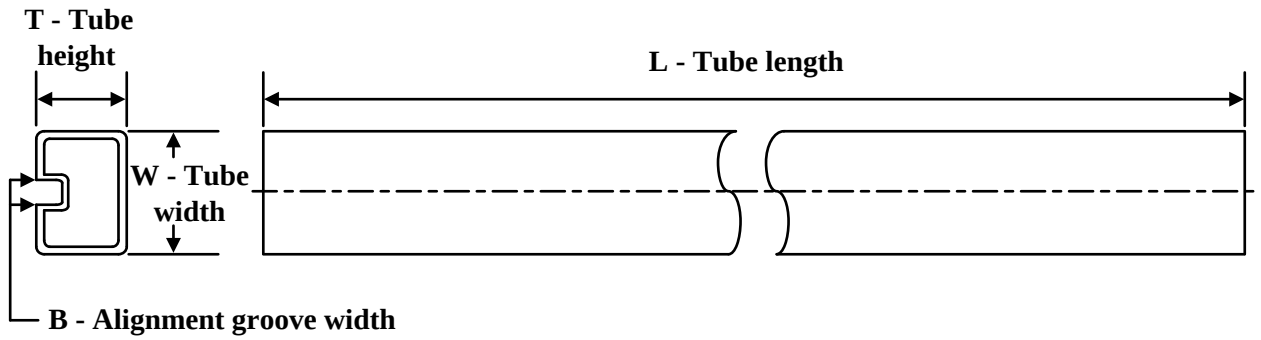
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

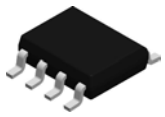
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL317CDR	SOIC	D	8	2500	340.5	336.1	25.0
TL317CDR	SOIC	D	8	2500	364.0	364.0	27.0
TL317CDRG4	SOIC	D	8	2500	340.5	336.1	25.0
TL317CPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
TL317PSR	SO	PS	8	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL317CD	D	SOIC	8	75	507	8	3940	4.32
TL317CDE4	D	SOIC	8	75	507	8	3940	4.32
TL317PS	PS	SOP	8	80	530	10.5	4000	4.1

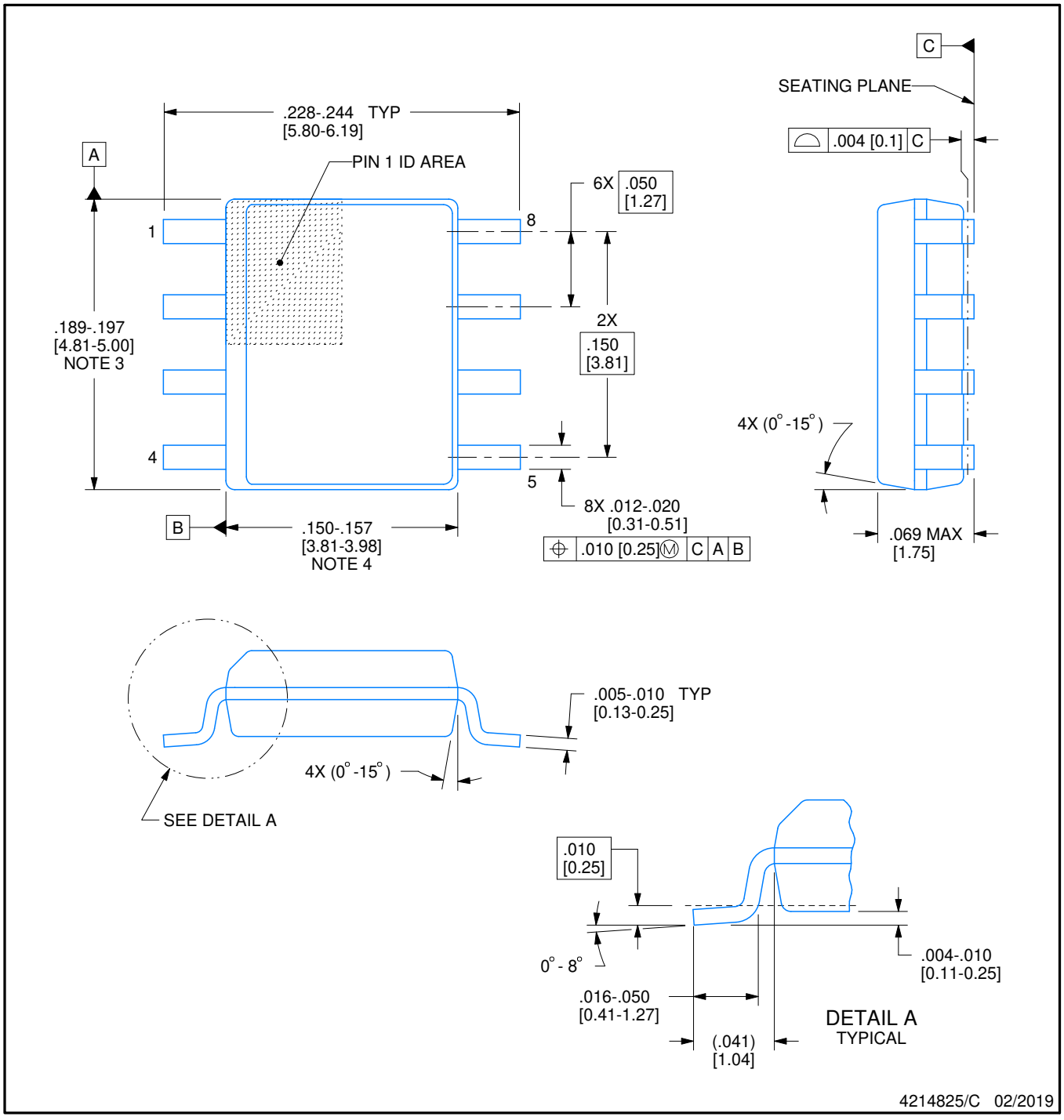


PACKAGE OUTLINE

D0008A

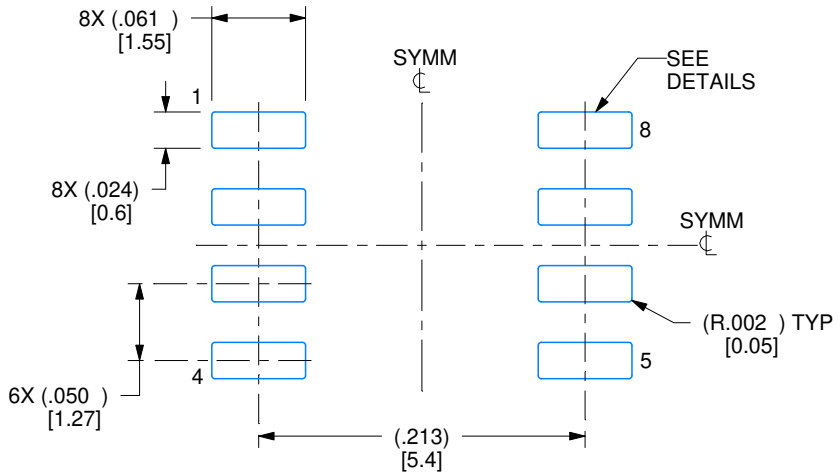
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

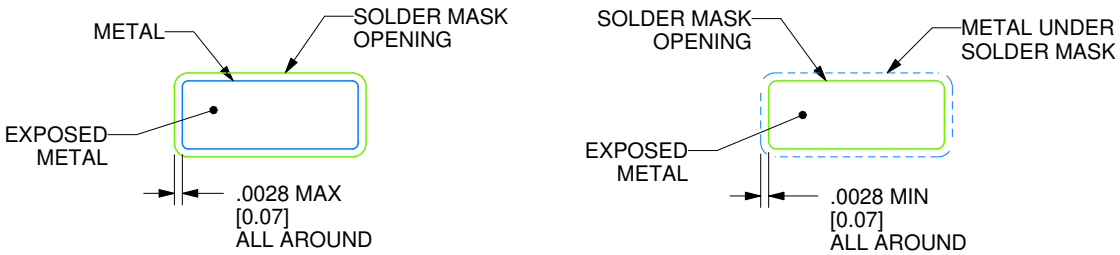


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

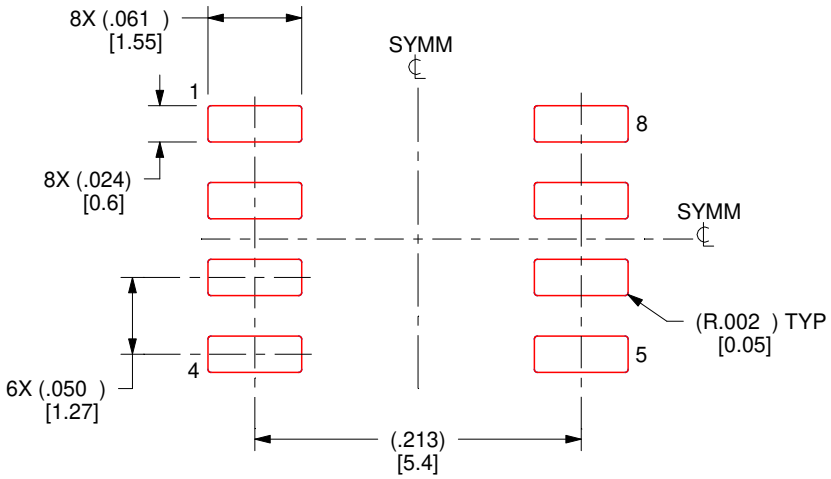
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

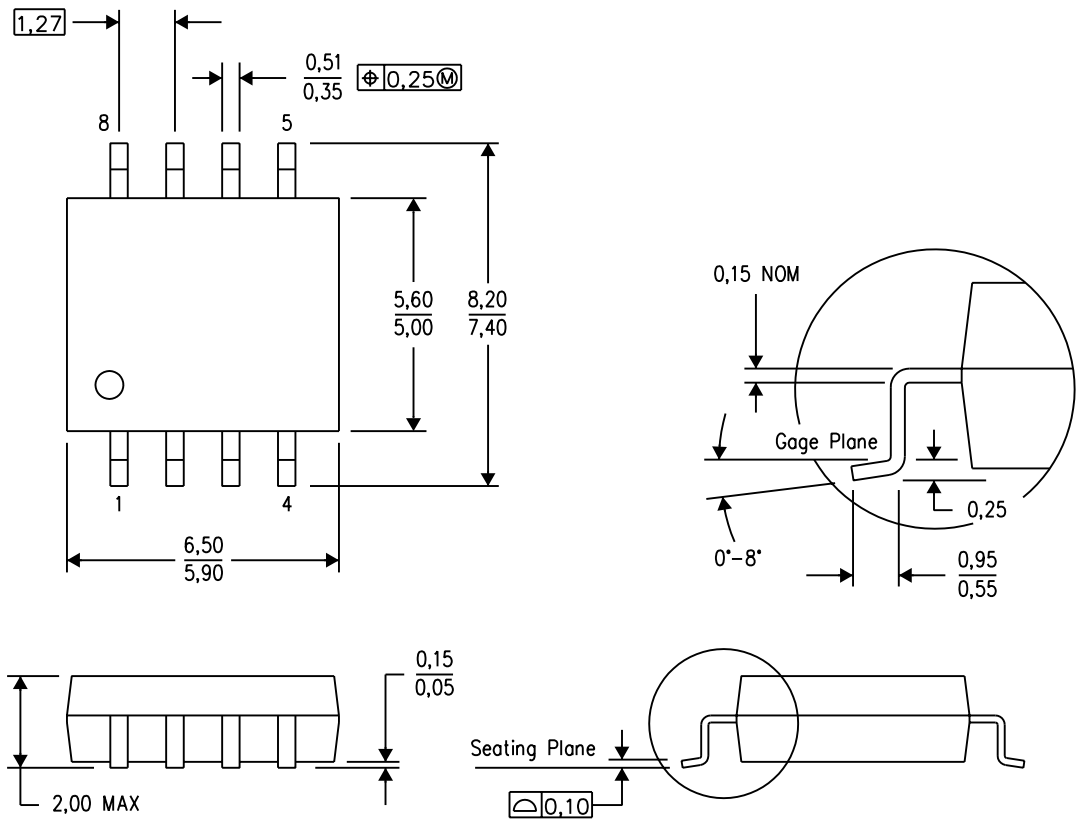
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

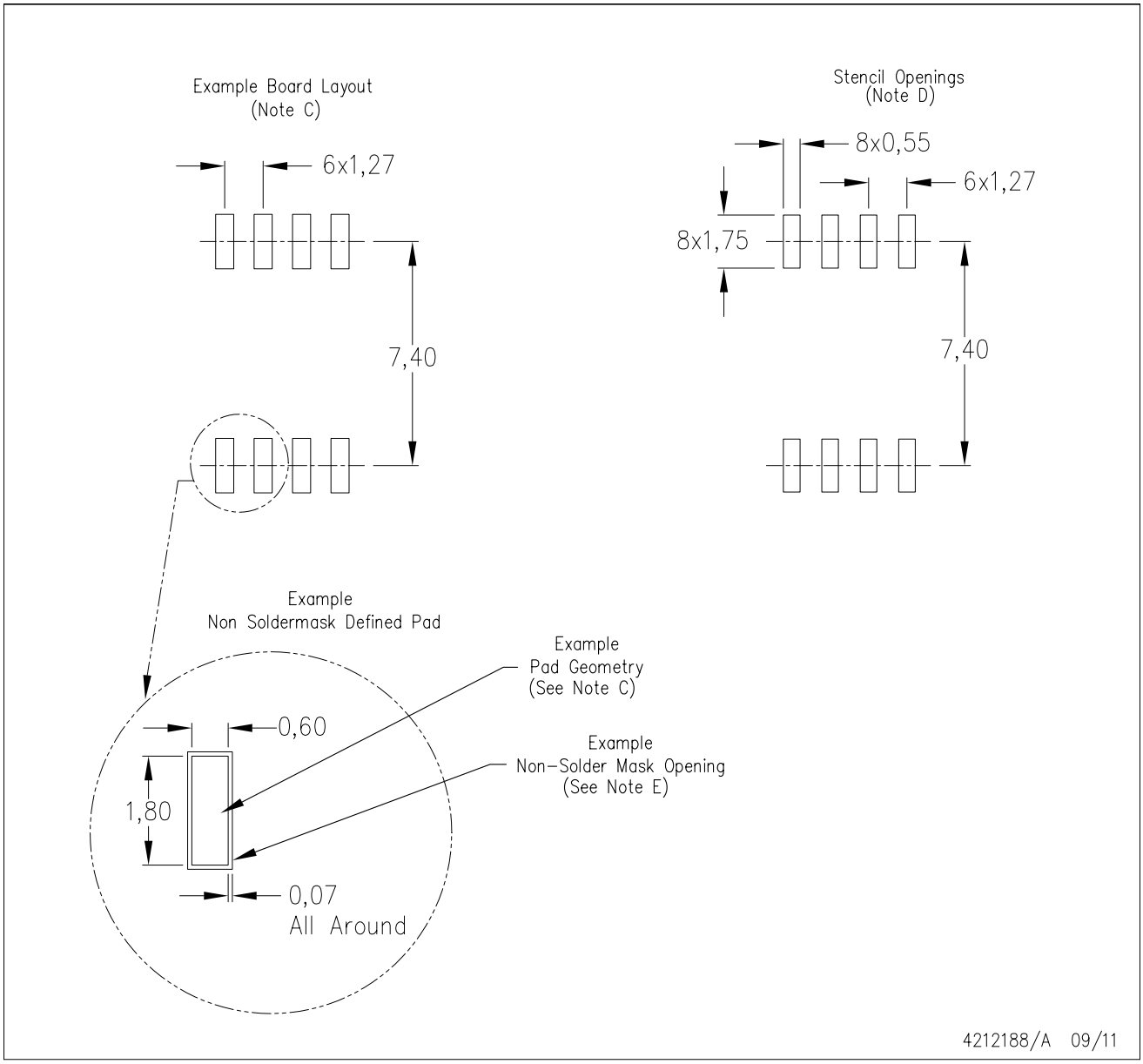
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



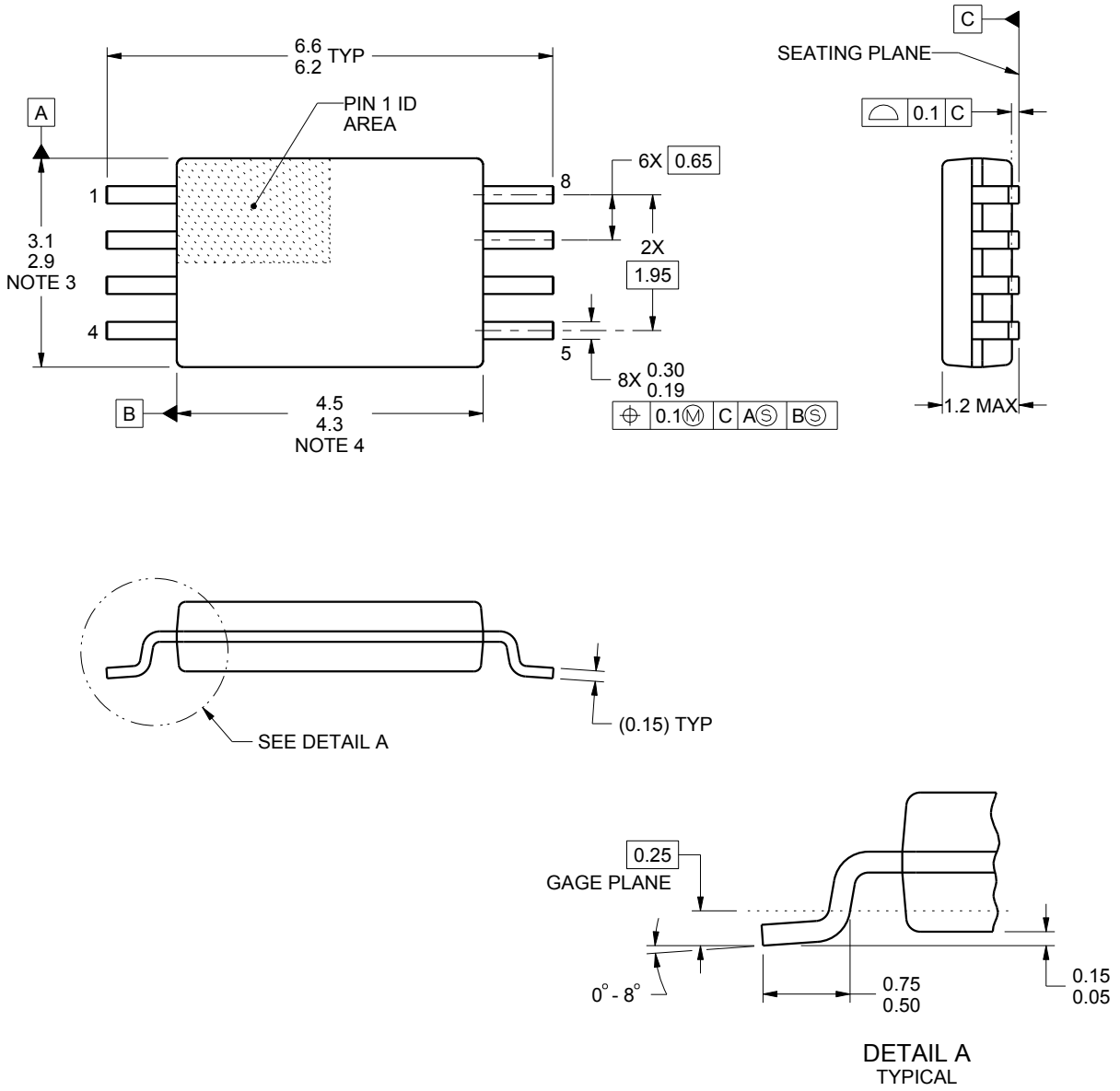
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0008A

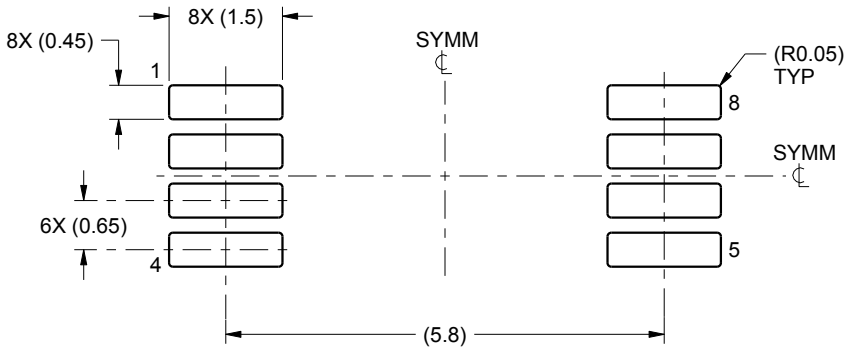
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

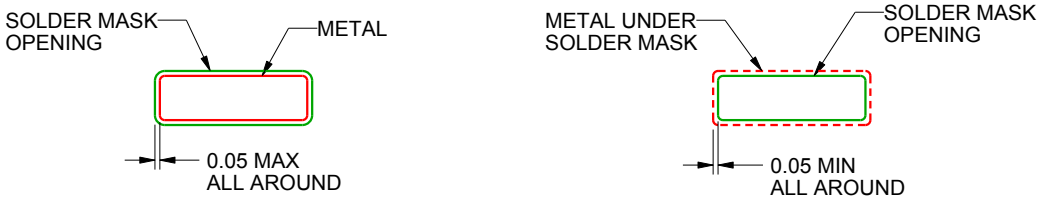


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

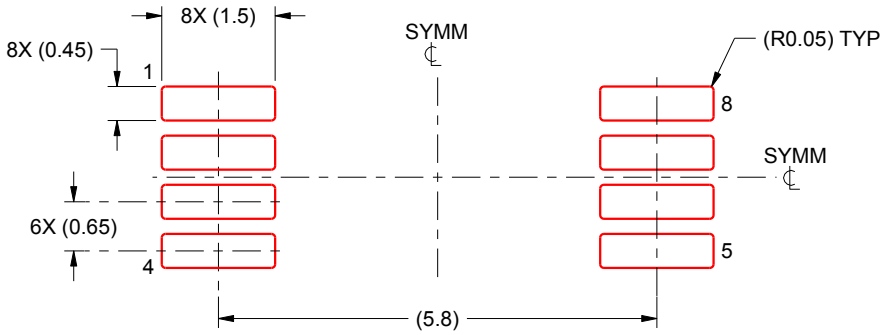


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

LP 3 TO-92 - 5.34 mm max height

TRANSISTOR OUTLINE

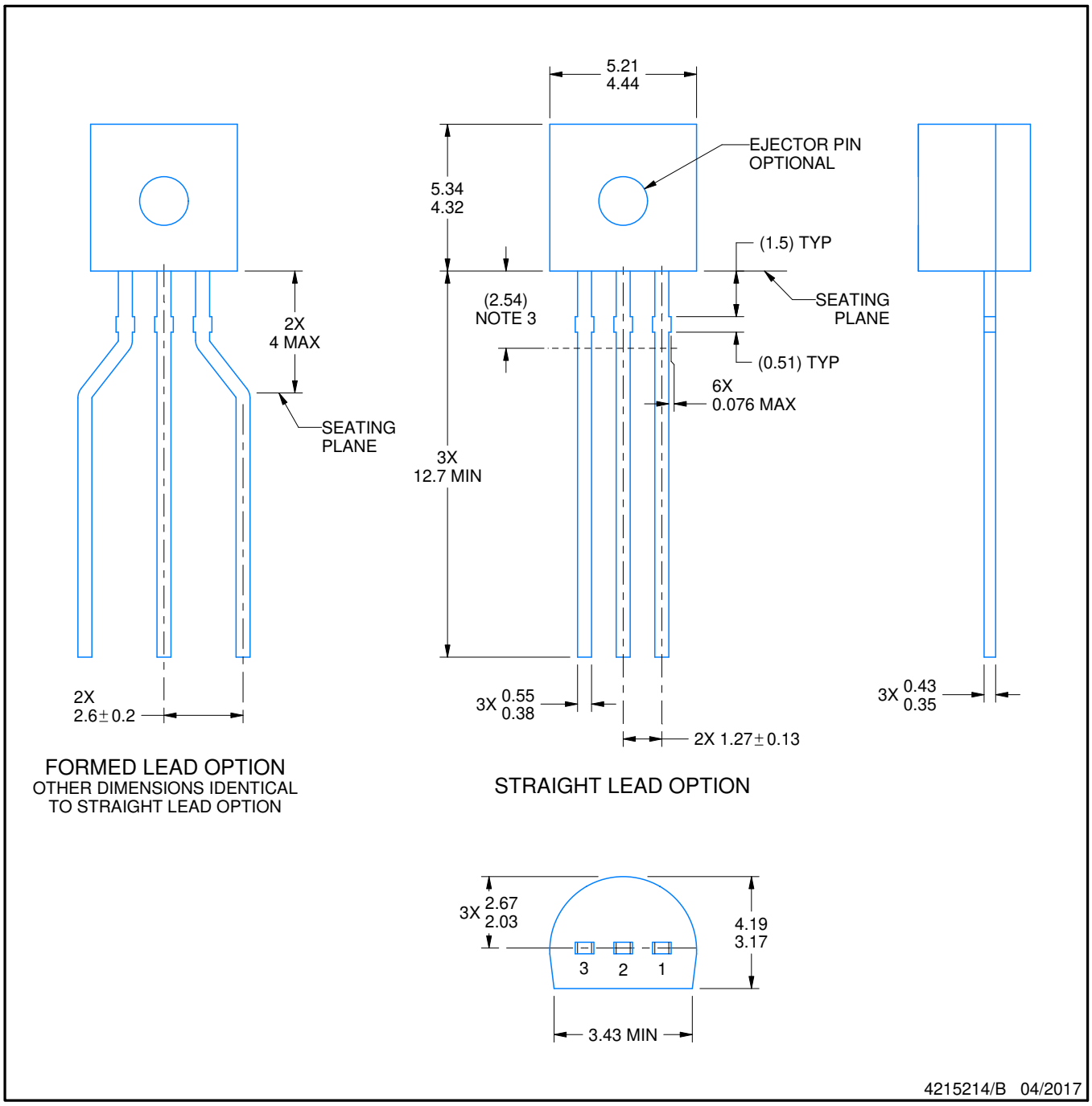
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

LP0003A

PACKAGE OUTLINE

TO-92 - 5.34 mm max height

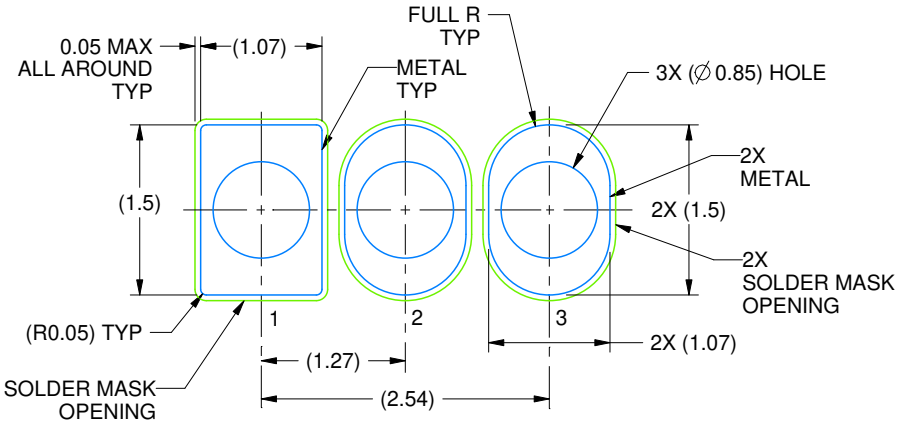
TO-92



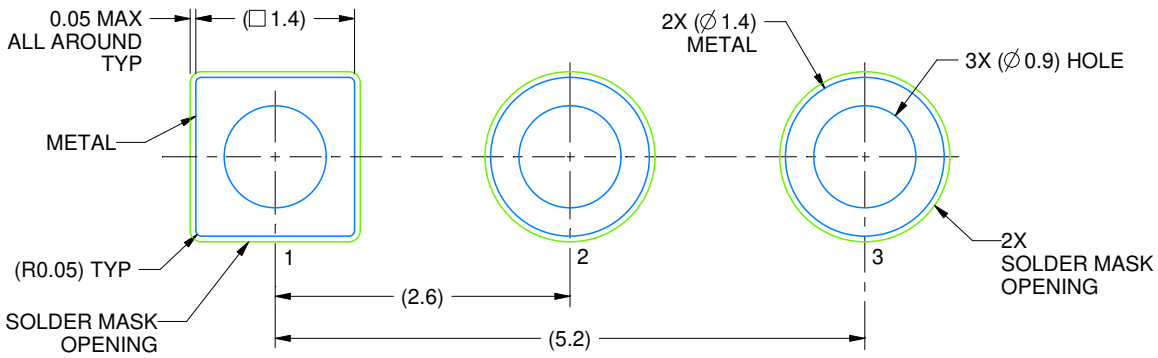
4215214/B 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead dimensions are not controlled within this area.
4. Reference JEDEC TO-226, variation AA.
5. Shipping method:
   a. Straight lead option available in bulk pack only.
   b. Formed lead option available in tape and reel or ammo pack.
   c. Specific products can be offered in limited combinations of shipping medium and lead options.
   d. Consult product folder for more information on available options.



LAND PATTERN EXAMPLE
STRAIGHT LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X



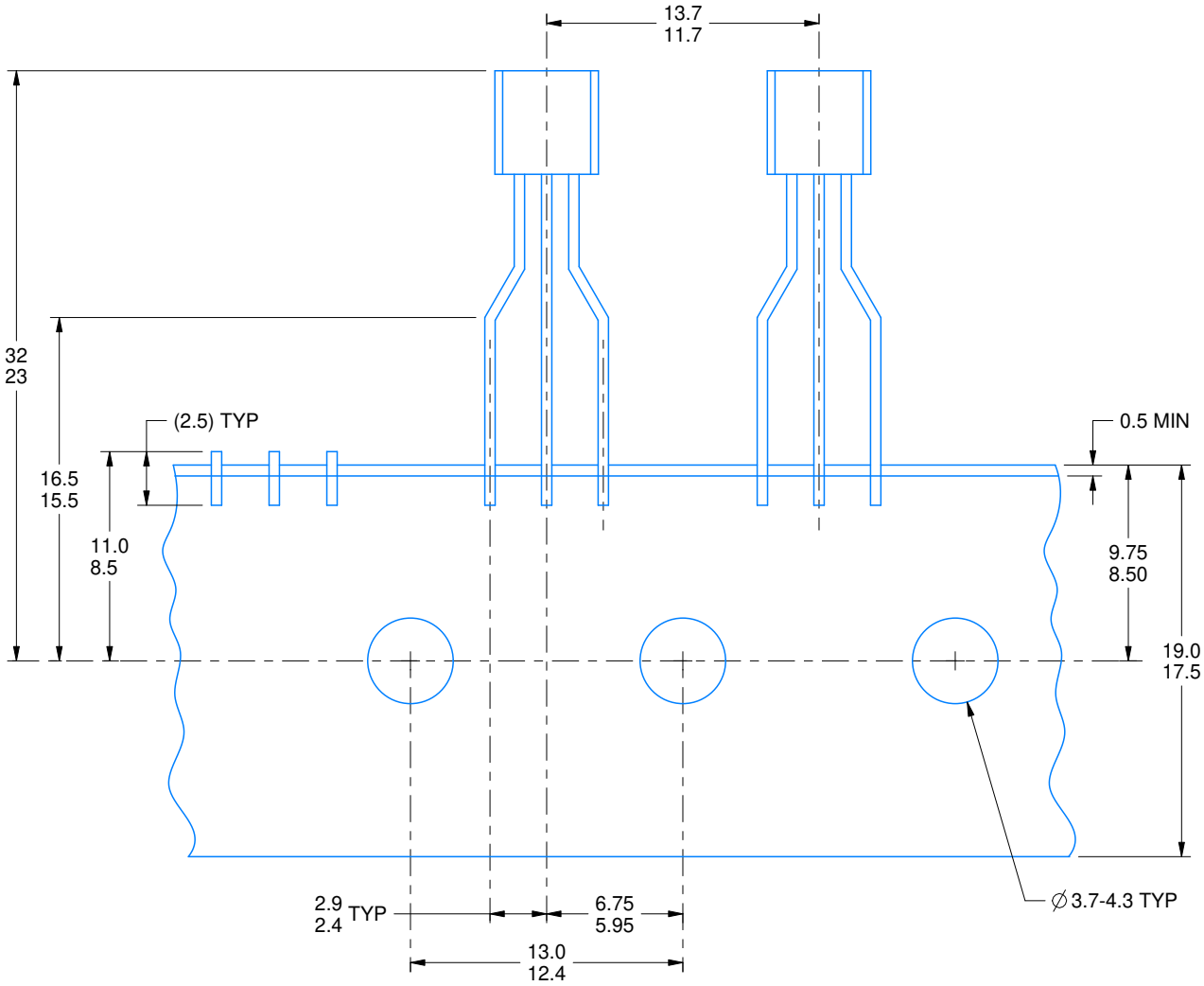
LAND PATTERN EXAMPLE
FORMED LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X

4215214/B 04/2017

LP0003A

TO-92 - 5.34 mm max height

TO-92



FOR FORMED LEAD OPTION PACKAGE

4215214/B 04/2017

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