ON Semiconductor

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Test Procedure for the AMIS492X0GEVB

Test Fixture

This procedure assumes that all measurements are made with the test unit connected to the provided test fixture. The schematic of the test fixture is shown in figure 1.

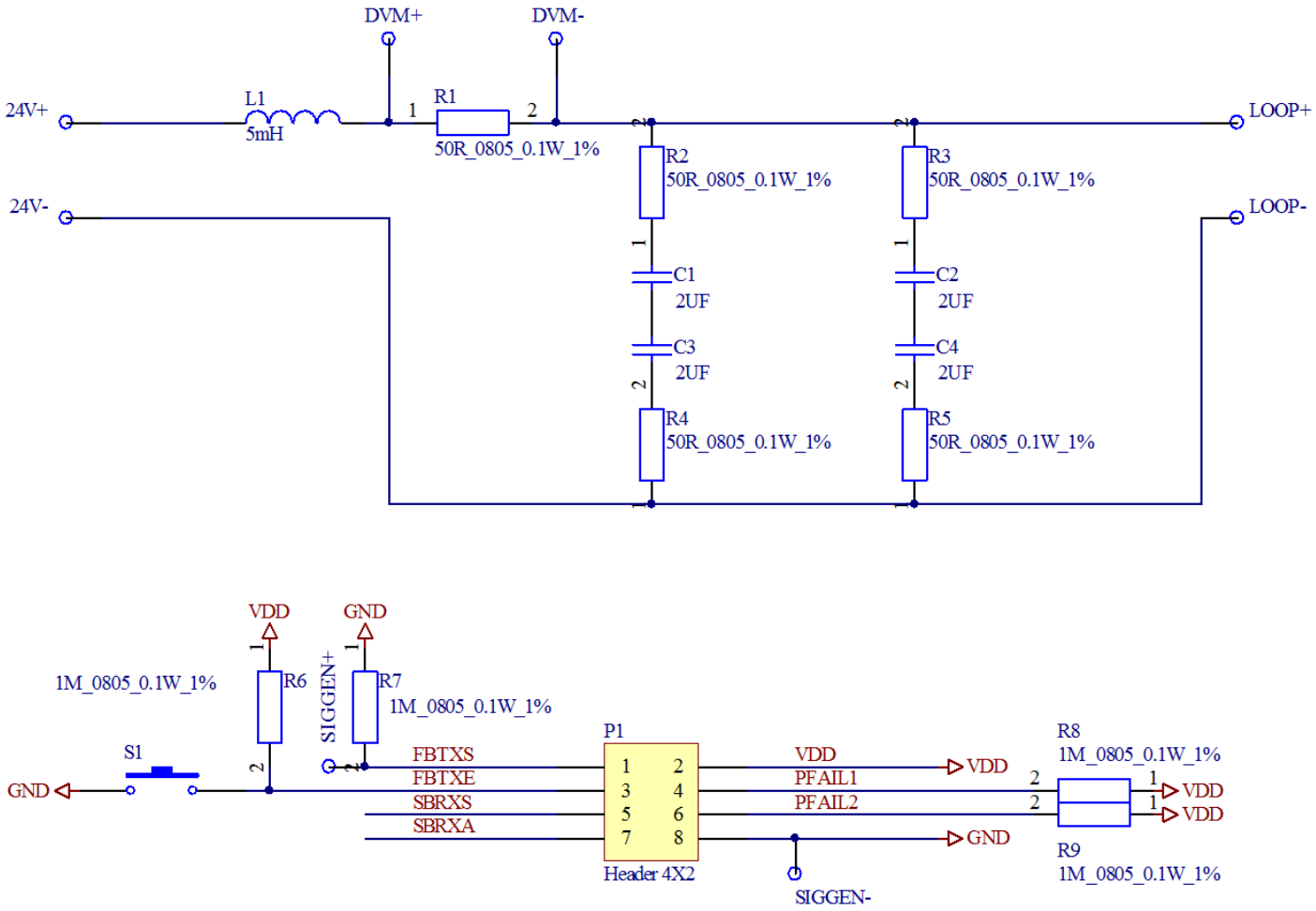

Figure 1 – Test Fixture

Equipment Required

The following test equipment is required to follow the test procedure

- + 24 V power supply
- Oscilloscope
- Square wave generator
- 3 digits DMM

Test Procedure

1. Connect header cable connector to JP1 (See white mark line)
2. Connect Field bus wires to J2 at the AMIS-49200 Ref Design Board
3. Connect power supply to +24 V jacks on fixture (White dots)
4. Connect DMM to Loop current jacks on fixture (Green 50R-resistor)
5. Turn S1 off (Marker visible)
6. Turn on +24V power supply
7. Measure loop current (~10 mA)
8. Measure VDD on JP1 pin 2 (~3V)
9. Measure VAA on J1 Pin 2 (~5V)
10. Measure Pfail1 on JP1 pin 4 (~VDD - 0.5V)
11. Measure Pfail2 on JP1 pin 6 (~VDD - 0.5V)
12. Connect signal generator to generator jacks on fixture
13. Set signal generator to 31.25 kHz 3V p-p (0 to VDD p-p)
14. Measure loop signal with scope = 0 V AC
15. Measure SBRXA = 0 V
16. Turn on S1.
17. Measure SBRXA = VDD
18. Measure SBRXS with scope = 31.25 kHz square wave 0 to VDD
19. Measure loop signal with scope DC Couple
20. Measure loop signal low value referenced to no signal with scope DC value in step 14
21. Measure loop signal high value referenced to no signal with scope DC value in step 14
22. Difference signal high to signal low (step 21 – step 20)
23. Loop rise time = < 8us (10%-90%)
24. Loop fall time = < 8us (90%-10%)

Test Results

See table 1 for minimum and maximum allowed values of the measured parameters.

Step Number	Measured Variable Name	Minimum value	Nominal Value	Maximum Value	Units
7	Loop Current (Across 50 ohm)	435 (8.7 mA)	500 (10 mA)	565 (11.3 mA)	mV dc
8	VDD	2.80	3.00	3.20	V dc
9	VAA	4.85	5.00	5.15	V dc
10	Pfail1	VDD-0.5	-	-	V dc
11	Pfail2	VDD-0.5	-	-	V dc
14	Loop Signal	-	-	5	mV ac
15	SBRXA	-	0	-	mV p-p
17	SBRXA	-	VDD	-	V dc
18	SBRXS (325 kHz Square wave)	0	-	VDD	V
19	Loop Signal (peak-peak)	750	850	1000	mV p-p
20	Loop Signal (zero to positive peak)	-	375	-	mV peak
21	Loop Signal (zero to positive peak)	-	375	-	mV peak
22	Loop Signal asymmetry (step 21 – step 20)	-50	0	+50	mV
23	Loop signal rise time (10% to 90%)	-	-	8	µs
24	Loop Signal fall time (10% to 90%)	-	-	8	µs

Table 1 – Test limits