PGA300 Signal Conditioner and Transmitter for Pressure Sensors

1 Features

- Analog features:
  - Analog front-end for resistive bridge sensors
  - Accommodates sensor sensitivities from 1 mV/V to 135 mV/V
  - On-chip temperature sensor
  - Programmable gain
  - 16-bit sigma-delta analog-to-digital converter for signal channel
  - 16-bit sigma-delta analog-to-digital converter for temperature channel
  - 14-bit output DAC
- Digital Features:
  - <0.1% FSO accuracy across temperature
  - System response time <220 µs
  - Third-order temperature and nonlinearity compensation
  - Diagnostic functions
  - Integrated EEPROM for device operation, calibration data, and user data
- Peripheral features:
  - One-wire interface enables communication through the power-supply pin
  - 4-mA to 20-mA current-loop output
  - Ratiometric and absolute voltage output
- Power supply:
  - On-chip power management accepts wide power-supply voltage from 3.3 V to 30 V
  - Integrated reverse voltage protection circuit
- Industrial temperature range: –40°C to +150°C

2 Applications

- Pressure transmitters
- Temperature transmitters
- Flow transmitters
- Level transmitters

3 Description

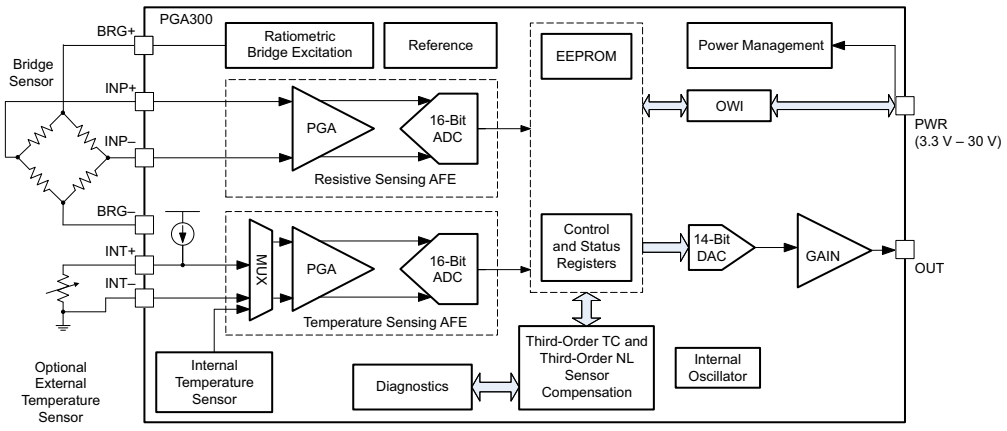
The PGA300 provides an interface for piezoresistive and strain-gauge pressure-sense elements. The device is a full system-on-chip (SoC) solution that incorporates a programmable analog front-end (AFE), ADC, and digital signal processing that enable direct connection to the sense element. Further, the PGA300 includes integrated voltage regulators and an oscillator, thus minimizing the number of external components. The device achieves high accuracy by employing third-order temperature and nonlinearity compensation. External communication is achieved by using a one-wire serial interface (OWI) through the power-supply pin in order to simplify the system calibration process. An Integrated DAC supports absolute-voltage, ratiometric-voltage, and 4-mA to 20-mA current-loop outputs.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
PGA300	VQFN (36)	6.00 mm × 6.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

PGA300 Simplified Block Diagram



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- Changed document for flow, structure, correcting incorrect data, addition of missing data, and for clarification of device and how the device functions ... 1
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- Changed pin descriptions in *Pin Functions* table for clarity and functionality ... 5
- Changed *Absolute Maximum Ratings* table ... 6
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Revision History (continued)

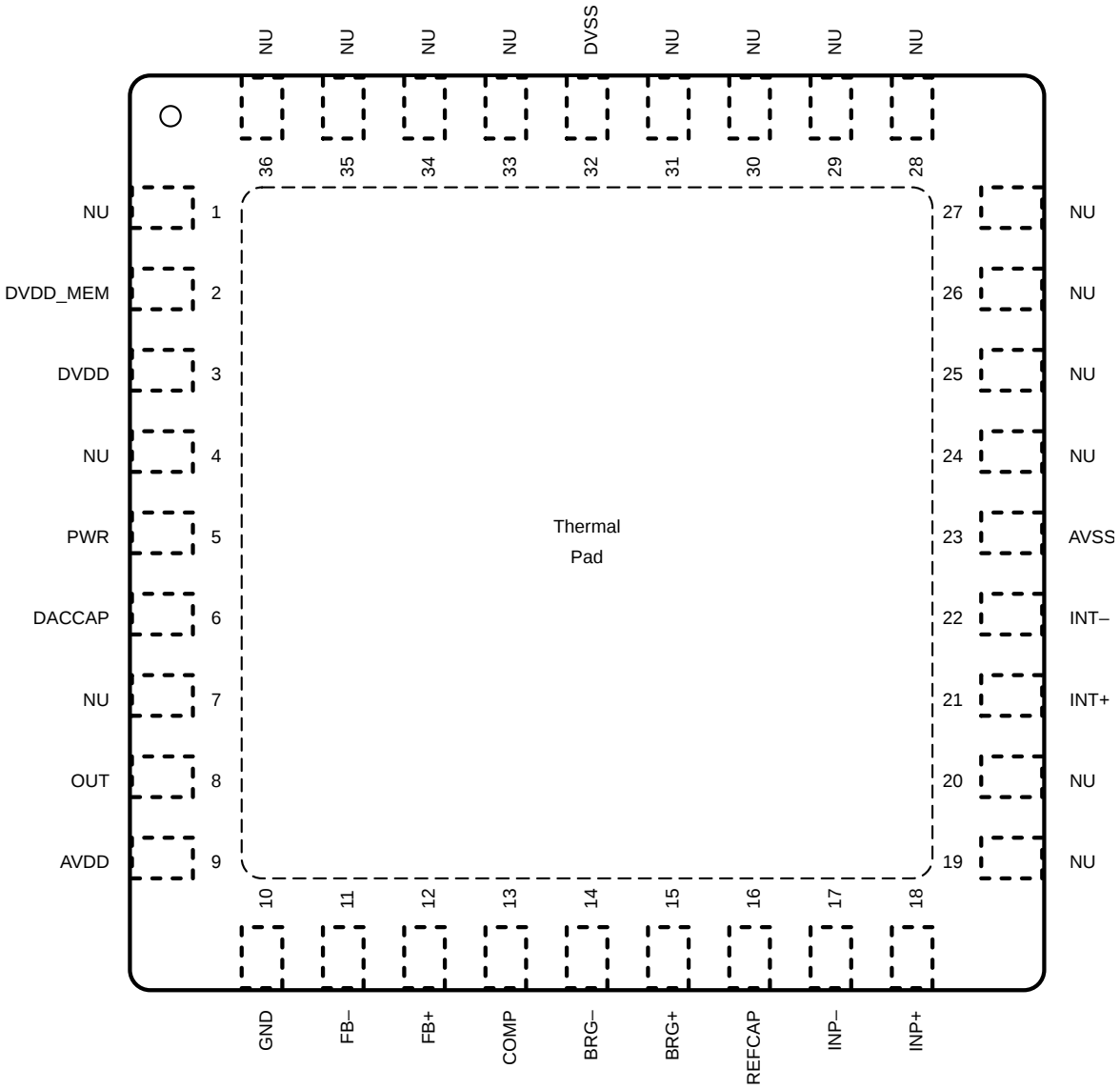
- Changed *Layout Guidelines* section 71
- Added *Related Documentation* section 73

Changes from Original (October 2014) to Revision A **Page**

- Changed data sheet from PRODUCT PREVIEW to PRODUCTION DATA 1

5 Pin Configuration and Functions

RHH Package
36-Pin VQFN With Thermal Pad
Top View



NU – Make no external connection

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AVDD	9	O	AVDD regulator output. Connect a 100-nF capacitor to AVSS.
AVSS	23	—	Analog ground(1)
BRG+	15	O	Bridge drive, positive
BRG–	14	O	Bridge drive, negative
COMP	13	I	Output amplifier compensation
DACCAP	6	O	DAC capacitor
DVDD	3	O	DVDD regulator output. Connect a 100-nF capacitor to DVSS.
DVDD_MEM	2	O	Power supply for EEPROM and OTP. Connect to DVDD.
DVSS	32	—	Digital ground(1)
FB+	12	I	Feedback, positive
FB–	11	I	Feedback, negative
GND	10	—	Ground(1)
INP+	18	I	Resistive sensor positive input
INP–	17	I	Resistive sensor negative input
INT+	21	I	External temperature sensor positive input
INT–	22	I	External temperature sensor negative input
NU	1, 4, 7, 19, 20, 24 to 31, 33 to 36	—	Leave floating; solder to PCB but do not connect electrically to any net.
OUT	8	O	DAC gain stage output
PWR	5	I	Input power supply. Connect a 100-nF capacitor to GND.
REFCAP	16	O	Accurate reference capacitor. Connect a 100-nF capacitor to AVSS.
Thermal pad	—	—	Connect to AVSS

(1) Tie AVSS, DVSS and GND together.

6 Specifications

6.1 Absolute Maximum Ratings

see (1)

		MIN	MAX	UNIT
V_{PWR}	Supply voltage	–28	33	V
	Voltage at sensor input pins: INP+, INP–, INT+, INT–	–0.3	2	V
	Voltage at AVDD, AVSS, BRG+, BRG–, COMP, DACCAP, DVDD, DVDD_MEM, DVSS, FB–, REFCAP pins	–0.3	3.6	V
	Voltage at FB+ pin	–2	V_{PWR} + 0.3	V
	Voltage at OUT pin	–0.3	33	V
I_{PWR}	Supply current (OUT pin short to GND)		25	mA
T_{Jmax}	Maximum junction temperature		155	°C
T_{stg}	Storage temperature	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{PWR}	Power supply voltage		3.3		30	V
	Slew rate	V_{PWR} = 0 V to 30 V			0.5	V/µs
	Capacitor value on PWR pin		10	100		nF
	Capacitor value on REFCAP pin		10	100	1000	nF
T_A	Operating ambient temperature		–40		150	°C
	EEPROM programming temperature		–40		140	°C

6.4 Thermal Information

THERMAL METRIC (1)		PGA300 RHH (VQFN) 36 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.5 Electrical Characteristics: Reverse Voltage Protection

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Reverse voltage		–28			V
	Voltage drop across reverse voltage protection element			20		mV

6.6 Electrical Characteristics: Regulators

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{AVDD}	AVDD voltage	C_{AVDD} = 100 nF		3		V
V_{DVDD}	DVDD voltage – operating	C_{DVDD} = 100 nF		1.8		V

6.7 Electrical Characteristics: Internal References

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	High-voltage reference voltage			1.2		V
	Accurate reference voltage			2.5		V

6.8 Electrical Characteristics: Bridge Sensor Supply

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BRG+} – $V_{BRG–}$	Bridge supply voltage	VBRDG_CTRL[1:0] = 0b00, no load		2.5		V
		VBRDG_CTRL[1:0] = 0b01, no load		2		
		VBRDG_CTRL[1:0] = 0b10, no load		1.25		
I_{BRG}	Current supply to the bridge				1.5	mA
C_{BRG}	Capacitive load	R_{BRG} = 20 kΩ			2	nF

6.9 Electrical Characteristics: External Temperature Sensor Supply

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{TEMP}	Current supply to external temperature sensor	ITEMP_CTRL[2:0] = 0b000		25		µA
		ITEMP_CTRL[2:0] = 0b001		50		
		ITEMP_CTRL[2:0] = 0b010		100		
		ITEMP_CTRL[2:0] = 0b011		500		
		ITEMP_CTRL[2:0] = 0b1xx		OFF		
C_{TEMP}	Capacitive load				100	nF
	Output impedance			15		MΩ

6.10 Electrical Characteristics: Internal Temperature Sensor

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Temperature range		–40		150	°C
	Zero-temperature T ADC output code	T_A = 0°C, T Gain = 5 V/V		6680		DEC
	Temperature coefficient	T Gain = 5 V/V		25.9		Codes/°C

6.11 Electrical Characteristics: P Gain Stage (Chopper Stabilized)

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Gain steps (5 bits)	P_GAIN[4:0] = 0b00000		5		V/V
		P_GAIN[4:0] = 0b00001		5.48		
		P_GAIN[4:0] = 0b00010		5.97		
		P_GAIN[4:0] = 0b00011		6.56		
		P_GAIN[4:0] = 0b00100		7.02		
		P_GAIN[4:0] = 0b00101		8		
		P_GAIN[4:0] = 0b00110		9.09		
		P_GAIN[4:0] = 0b00111		10		
		P_GAIN[4:0] = 0b01000		10.53		
		P_GAIN[4:0] = 0b01001		11.11		
		P_GAIN[4:0] = 0b01010		12.5		
		P_GAIN[4:0] = 0b01011		13.33		
		P_GAIN[4:0] = 0b01100		14.29		
		P_GAIN[4:0] = 0b01101		16		
		P_GAIN[4:0] = 0b01110		17.39		
		P_GAIN[4:0] = 0b01111		18.18		
		P_GAIN[4:0] = 0b10000		19.05		
		P_GAIN[4:0] = 0b10001		20		
		P_GAIN[4:0] = 0b10010		22.22		
		P_GAIN[4:0] = 0b10011		25		
		P_GAIN[4:0] = 0b10100		30.77		
		P_GAIN[4:0] = 0b10101		36.36		
		P_GAIN[4:0] = 0b10110		40		
		P_GAIN[4:0] = 0b10111		44.44		
		P_GAIN[4:0] = 0b11000		50		
		P_GAIN[4:0] = 0b11001		57.14		
		P_GAIN[4:0] = 0b11010		66.67		
		P_GAIN[4:0] = 0b11011		80		
		P_GAIN[4:0] = 0b11100		100		
		P_GAIN[4:0] = 0b11101		133.33		
		P_GAIN[4:0] = 0b11110		200		
		P_GAIN[4:0] = 0b11111		400		
	Gain-bandwidth product			10		MHz
	Input-referred noise density(1)	f = 0.1 Hz to 2 kHz, P Gain = 400 V/V		15		nV/√Hz
	Input offset voltage			10		µV
	Input bias current			5		nA
	Frequency response	P Gain = 400 V/V, <1 kHz			±0.1	%V/V
	Common-mode voltage range		Depends on selected gain, bridge supply and sensor span(2)			V
	Common-mode rejection ratio	f_{CM} = 50 Hz, P Gain = 5 V/V		110		dB
	Input impedance		10			MΩ

(1) Total input-referred noise including P Gain noise, ADC reference noise, P ADC thermal noise, and P ADC quantization noise.
(2) **Common Mode at P Gain Input and Output:** There are two constraints:
(a) The single-ended voltage of the positive and negative pins at the P Gain input must be between 0.3 V and 1.8 V
(b) The single-ended voltage of the positive and negative pins at the P Gain output must be between 0.1 V and 2 V

6.12 Electrical Characteristics: P Analog-to-Digital Converter

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Sigma-delta modulator frequency			1		MHz
	Differential input voltage range		–2.5		2.5	V
	Number of bits			16		Bits
INL	Integral nonlinearity				±0.5	LSB
	ADC two's complement code	Differential input = –2.5 V		0x8000		
		Differential input = 0 V		0x0000		
		Differential input = 2.5 V		0x7FFF		

6.13 Electrical Characteristics: T Gain Stage (Chopper Stabilized)

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Gain steps (2 bits)	T_GAIN[1:0] = 0b00		1.33		V/V
		T_GAIN[1:0] = 0b01		2		
		T_GAIN[1:0] = 0b10		5		
		T_GAIN[1:0] = 0b11		20		
	Gain-bandwidth product			350		kHz
	Input-referred noise density(1)	f = 0.1 Hz to 100 Hz, T Gain = 5 V/V		110		nV/√Hz
	Input offset voltage			95		µV
	Input bias current			5		nA
	Frequency response	T Gain = 20 V/V, <100 Hz			0.335	%V/V
	Common-mode voltage range		Depends on selected gain and current supply(2)			V
	Common-mode rejection ratio	f_{CM} = 50 Hz		110		dB
	Input impedance		1			MΩ

(1) Total input-referred noise including T Gain noise, ADC reference noise, T ADC thermal noise, and T ADC quantization noise.
(2) **Common Mode at T Gain Input and Output:** There are two constraints:
(a) The single-ended voltage of the positive and negative pins at the T Gain input must be between 5 mV and 1.8 V
(b) The single-ended voltage of the positive and negative pins at the T Gain output must be between 0.1 V and 2 V

6.14 Electrical Characteristics: T Analog-to-Digital Converter

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Sigma-delta modulator frequency			1		MHz
	Differential input voltage range		–2.5		2.5	V
	Number of bits			16		Bits
INL	Integral nonlinearity				±0.5	LSB
	ADC two's complement code	Differential input = –2.5 V		0x8000		
		Differential input = 0 V		0x0000		
		Differential input = 2.5 V		0x7FFF		

6.15 Electrical Characteristics: DAC Output

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	DAC reference voltage	DAC_RATIOMETRIC = 0b0 (ratiometric)		0.25 × V_{PWR}		V
		DAC_RATIOMETRIC = 0b1		1.25		
	DAC resolution			14		Bits

6.16 Electrical Characteristics: DAC Gain Stage

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Buffer gain (see Figure 6)	DAC_GAIN[2:0] = 0b100		2		V/V
		DAC_GAIN[2:0] = 0b010		4		
		DAC_GAIN[2:0] = 0b110		6.67		
		DAC_GAIN[2:0] = 0b001		10		
	Current loop gain			1001		mA/mA
	Gain-bandwidth product			1		MHz
	Zero-code voltage (gain = 4 V/V)	DAC code = 0x0000, I_{DAC} = 2.5 mA			20	mV
	Full-scale code voltage (gain = 4 V/V)	DAC code is 0x1FFF, I_{DAC} = –2.5 mA	4.8			V
	Output current	DAC code = 0x1FFF, DAC code = 0x0000			±2.5	mA
	Short-circuit source current	DAC code = 0x1FFF		27		mA
	Short-circuit sink current	DAC code = 0x0000		27		mA
	Maximum capacitance	Without compensation			100	pF
		With compensation			100	nF

6.17 Electrical Characteristics: Diagnostics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OSC_PWR_OV	Oscillator circuit supply overvoltage threshold				3.3		V
OSC_PWR_UV	Oscillator circuit supply undervoltage threshold				2.7		V
BRG_OV	Resistive bridge sensor supply overvoltage threshold				10		% V_{BRG}
BRG_UV	Resistive bridge sensor supply undervoltage threshold				–10		% V_{BRG}
AVDD_OV	AVDD overvoltage threshold				3.3		V
AVDD_UV	AVDD undervoltage threshold				2.7		V
DVDD_OV	DVDD overvoltage threshold				2		V
DVDD_UV	DVDD undervoltage threshold				1.53		V
REF_OV	Reference overvoltage threshold				2.75		V
REF_UV	Reference undervoltage threshold				2.25		V
P_DIAG_PD	P Gain input diagnostics pulldown resistor value	PD[1:0] = 0b00			4		MΩ
		PD[1:0] = 0b01			3		
		PD[1:0] = 0b10			2		
		PD[1:0] = 0b11			1		
T_DIAG_PU	T Gain input diagnostics pullup resistor value				1		MΩ
INP_OV	P Gain input overvoltage threshold[1]	V_{BRG} = 2.5 V	THRS[2:0] = 0b000		72.5		% V_{BRG}
			THRS[2:0] = 0b001		70		
			THRS[2:0] = 0b010		65		
		V_{BRG} = 2 V	THRS[2:0] = 0b011		90		
			THRS[2:0] = 0b100		87.5		
			THRS[2:0] = 0b101		82.5		
		V_{BRG} = 1.25 V	THRS[2:0] = 0b110		100		
			THRS[2:0] = 0b111		95		
INP_UV	P Gain input undervoltage threshold[1]	V_{BRG} = 2.5 V	THRS[2:0] = 0b000		7.5		% V_{BRG}
			THRS[2:0] = 0b001		10.0		
			THRS[2:0] = 0b010		15.0		
		V_{BRG} = 2 V	THRS[2:0] = 0b011		10.0		
			THRS[2:0] = 0b100		12.5		
			THRS[2:0] = 0b101		17.5		
		V_{BRG} = 1.25 V	THRS[2:0] = 0b110		17.5		
			THRS[2:0] = 0b111		22.5		
INT_OV	T Gain input overvoltage threshold[2]				2.1		V
PGAIN_OV	Output overvoltage (single-ended) threshold for P Gain				2.25		V
PGAIN_UV	Output undervoltage (single-ended) threshold for P Gain				0.15		V
TGAIN_OV	Output overvoltage (single-ended) threshold for T Gain				2.25		V
TGAIN_UV	Output undervoltage (single-ended) threshold for T Gain				0.15		V
HARNESS_FAULT1	Open-wire leakage current 1. Open PWR with pullup on OUT				2		µA
HARNESS_FAULT2	Open-wire leakage current 2. Open GND with pulldown on OUT				20		µA

(1) INP+ and INP– each have individual threshold comparators.
(2) INT+ and INT– each have individual threshold comparators.

6.18 Electrical Characteristics: One-Wire Interface

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Communication baud rate(1)		600		9600	Bits per second
OWI_ENH	OWI activation high		5.95			V
OWI_ENL	OWI activation low				5.75	V
OWI_VIH	OWI transceiver Rx threshold for high		4.8		5.1	V
OWI_VIL	OWI transceiver Rx threshold for low		3.9		4.2	V
OWI_IOH	OWI transceiver Tx threshold for high		500		1379	µA
OWI_IOL	OWI transceiver Tx threshold for low		2		5	µA

(1) OWI over power line does not work if there is an LDO between the supply to the sensor and the PWR pin, or if the OWI high and low voltages are greater than the regulated voltage.

6.19 Electrical Characteristics: EEPROM (Non-Volatile Memory)

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Size			128		Bytes
	Erase-write cycles				1000	Cycles
	Programming time	Per 8-byte page			8	ms
	Data retention		10			Years

6.20 Electrical Characteristics: Power-Supply Currents

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{PWR}	Power-supply current	Normal operation. No load on BRG, no load on DAC.		2.5		mA
		EEPROM programming. While EEPROM is being programmed, no load on BRG, no load on DAC.			9	

6.21 Electrical Characteristics: Timing

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Power-up time (including analog and digital)	V_{PWR} ramp rate 0.5 V/µs			1	ms
	Start-up time	No IIR filter(1)		180		µs
		IIR filter = 1000 Hz(2)		1158		
	Response time	No IIR filter(3)		211		µs
		IIR filter = 1000 Hz(4)		1050		
	Output rate			128		µs

(1) Time from power up to reach 90% of valid output.
(2) Time from power up to reach valid output, including settling time.
(3) Time to reach 90% of valid output.
(4) Time to reach valid output, including settling time.

6.22 Electrical Characteristics: Accuracy

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Absolute-voltage output mode, overall accuracy (PGA300 only, no sense element) (1)	3 pressure - 1 temperature calibration, overall accuracy calculated using points different from points used for calibration		0.2		%FSO
		3 pressure - 3 temperature calibration, input voltage not subject to temperature variation, overall accuracy calculated using points different from points used for calibration		0.1		%FSO
		4 pressure - 4 temperature calibration, input voltage not subject to temperature variation, overall accuracy calculated using points different from points used for calibration		0.08		%FSO
	Ratiometric-voltage output mode, overall accuracy (PGA300, no sense element) (1)	3 pressure - 1 temperature calibration, overall accuracy calculated using points different from points used for calibration		0.5		%FSO
		3 pressure - 3 temperature calibration, input voltage not subject to temperature variation, overall accuracy calculated using points different from points used for calibration		0.25		%FSO
		4 pressure - 4 temperature calibration, input voltage not subject to temperature variation, overall accuracy calculated using points different from points used for calibration		0.2		%FSO
	Current output mode, overall accuracy (PGA300, no sense element) (1)	3 pressure - 1 temperature calibration, overall accuracy calculated using points different from points used for calibration		0.2		%FSO
		3 pressure - 3 temperature calibration, input voltage not subject to temperature variation, overall accuracy calculated using points different from points used for calibration		0.1		%FSO
		4 pressure - 4 temperature calibration, input voltage not subject to temperature variation, overall accuracy calculated using points different from points used for calibration		0.09		%FSO

(1) Sense element held at constant temperature while the PGA300 was calibrated at –25ºC, 25ºC, 85ºC and 125ºC. Accuracy was then measured at –40ºC, 50ºC and 150 ºC.

6.23 Typical Characteristics

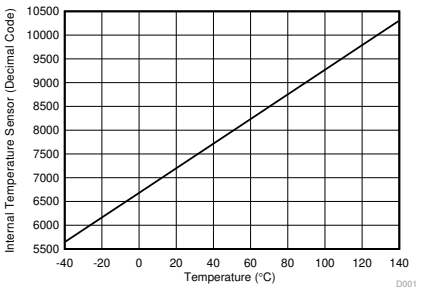


Figure 1. Internal Temperature Sensor Code vs Temperature

7 Detailed Description

7.1 Overview

The PGA300 can be used in a variety of applications. The most common ones are for pressure and temperature measurement. Depending on the application, the device itself can be configured in different modes. The following sections provide details regarding these configurations.

The PGA300 is a high-accuracy, low-drift, low-noise, low-power, and easily programmable signal-conditioner device for resistive bridge pressure and temperature sensing applications. The PGA300 implements a third-order temperature coefficient (TC) and nonlinearity (NL) compensation algorithm to linearize the analog output. The PGA300 accommodates various sensing element types, such as piezoresistive, ceramic film, and steel membrane. The device supports sensor element sensitivities ranging from 1 mV/V to 135 mV/V. The typical applications supported are pressure sensor transmitters, transducers, liquid-level meters, flow meters, strain gauges, weight scales, thermocouples, thermistors, 2-wire resistance thermometers (RTDs), and resistive field transmitters. The device can also be used in accelerometer and humidity sensor signal-conditioning applications.

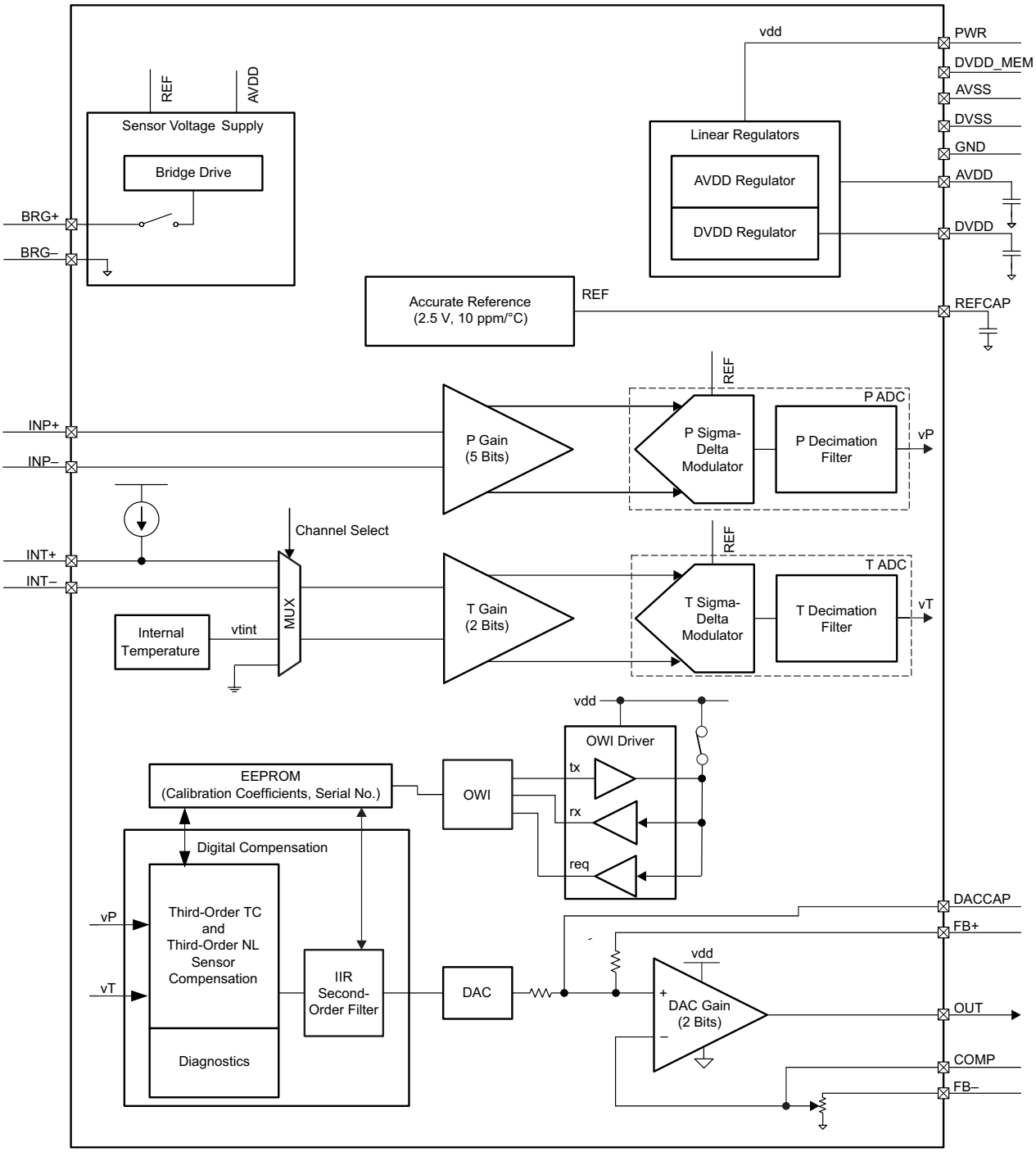
The PGA300 provides bridge excitation voltages of 2.5 V, 2 V, and 1.25 V, all ratiometric to the ADC reference level. The PGA300 has a unique one-wire interface (OWI) that supports communication and configuration through the power-supply line during the calibration process. This feature minimizes the number of wires needed for an application.

The PGA300 contains two separated analog front-end (AFE) signal chains; one for resistive-bridge inputs and one for temperature-sensing inputs. Each AFE has its own gain amplifier and a 16-bit ADC operating at a 7.8-kHz output rate. The resistive-bridge input AFE consists of a programmable gain with 32 steps ranging from 5 V/V to 400 V/V. For the temperature-sensing AFE, the PGA300 provides a current source that can supply up to 500 µA for optional external temperature sensing. This current source can also be used as a constant-current bridge excitation. The programmable gain in the temperature sensing AFE has four steps ranging from 1.33 V/V to 20 V/V. In addition, the PGA300 integrates an internal temperature sensor which can be configured as the input of the temperature-sensing AFE.

A 128-byte EEPROM is integrated in the PGA300 to store the calibration coefficients and the PGA300 configuration settings as needed. The PGA300 has a 14-bit DAC followed by a buffer gain stage of 2 V/V to 10 V/V. The device supports three industrial-standard outputs: ratiometric voltage, absolute voltage, and 4-mA to 20-mA current loop.

The diagnostic functions monitor the operating condition of the PGA300. The device can operate with a 3.3-V to 30-V power supply directly, without using an external LDO. The PGA300 has a wide ambient-temperature operating range from –40°C to 150°C. The package form is 6-mm × 6-mm 36-pin VQFN. Within this small package size, the PGA300 integrates all the functions needed for resistive-bridge sensing applications to minimize PCB area and simplify the overall application design.

7.2 Functional Block Diagram



7.3 Feature Description

This section describes individual functional blocks of the PGA300.

7.3.1 Reverse-Voltage Protection Circuit

The PGA300 includes a reverse-voltage protection circuit. This circuit protects the device from reverse-battery conditions on the external power supply.

7.3.2 Linear Regulators

The PGA300 has two main linear regulators: an AVDD regulator and a DVDD regulator. The AVDD regulator provides the 3-V voltage source for internal analog circuitry, whereas the DVDD regulator provides the 1.8-V regulated voltage for the digital circuitry. Connect 100-nF bypass capacitors between AVDD and AVSS and between DVDD and DVSS of the device.

7.3.3 Internal References

The PGA300 has two internal references. These references are described in the following subsections.

7.3.3.1 High-Voltage Reference

The high-voltage reference is an inaccurate reference used for the diagnostic thresholds.

7.3.3.2 Accurate Reference

The accurate reference is used to generate the reference voltage for the P ADC, T ADC and DAC. Place a 100-nF capacitor between the REFCAP pin and AVSS to limit the bandwidth of reference noise.

NOTE

The accurate reference is valid 50 µs after the digital core starts running at power up.

7.3.4 Bridge Sensor Supply for Resistive Bridges (BRG+ to BRG–)

The bridge sensor voltage-supply block of the PGA300 provides power to the resistive-bridge sensor. The bridge sensor supply in the PGA300 is configurable to a nominal output voltage of 2.5-V, 2-V, or 1.25-V using the VBRDG_CTRL[1:0] bits in the BRDG_CTRL register to accommodate bridge sense elements with different resistor values. The bridge sensor supply is ratiometric to the accurate reference, as illustrated in Figure 2.

Feature Description (continued)

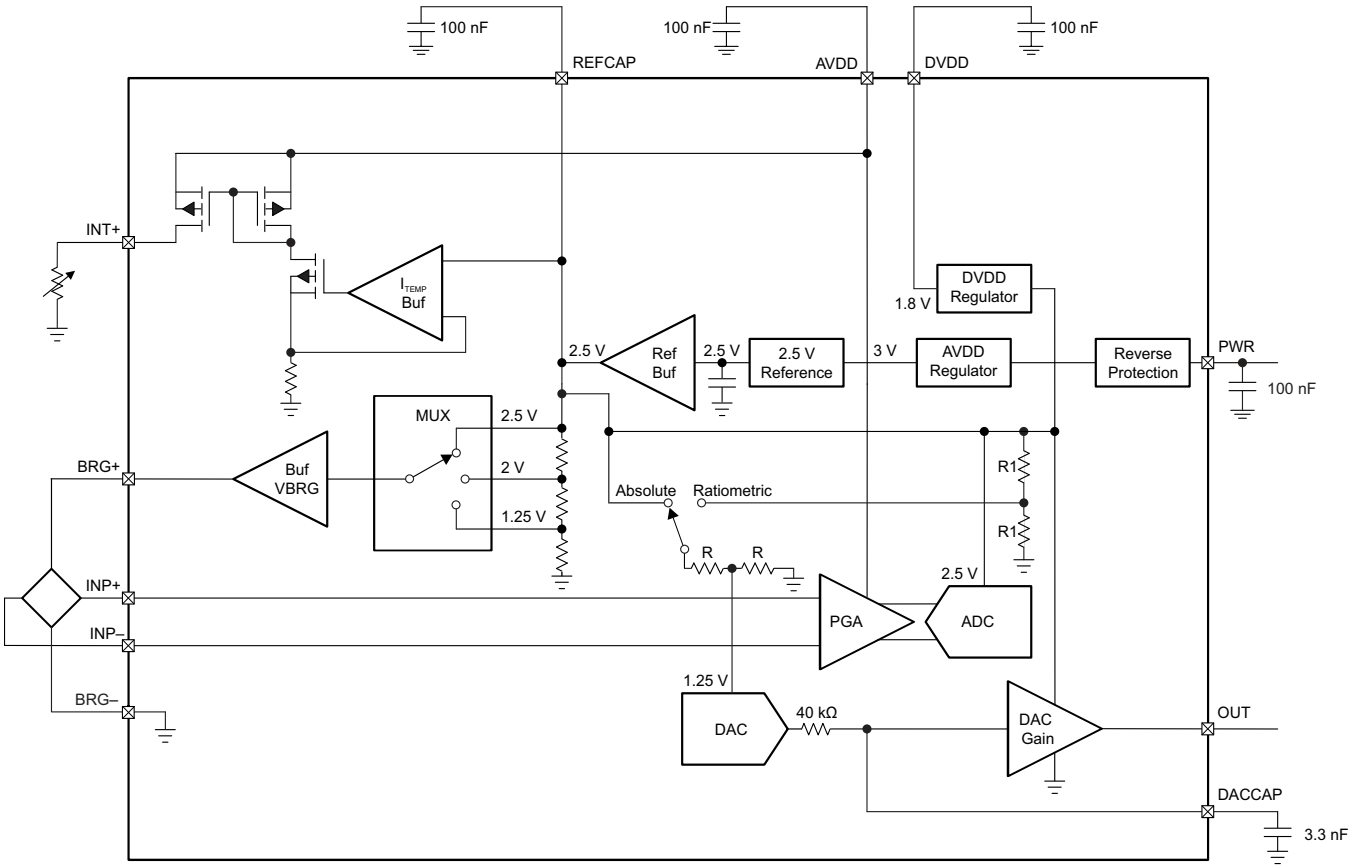


Figure 2. Bridge Sensor Supply and P ADC Reference Are Ratiometric

7.3.5 ITEMP Supply for External Temperature Sensors

The ITEMP block in the PGA300 supplies a programmable current to an external temperature sensor such as an RTD temperature probe or NTC or PTC thermistor. The temperature-sensor current source is ratiometric to the accurate reference.

The value of the current can be programmed using the ITEMP_CTRL[2:0] bits in the TEMP_CTRL register.

7.3.6 Internal Temperature Sensor

The PGA300 includes an internal temperature sensor whose voltage output is digitized by the T ADC. This digitized value is used to implement temperature compensation algorithms in software. The voltage generated by the internal temperature sensor is proportional to the device junction temperature.

Figure 3 shows the internal temperature sensor AFE.

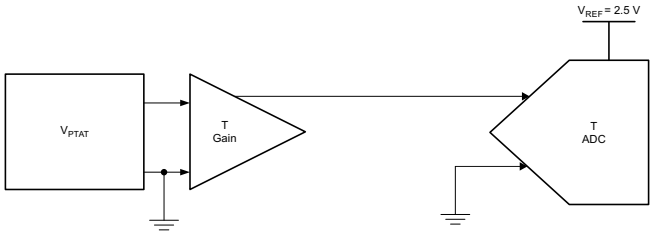


Figure 3. Temperature Sensor AFE

Feature Description (continued)

7.3.7 Pressure Measurement Signal Chain

The pressure measurement signal chain of the PGA300 consists of a programmable gain, an instrumentation amplifier stage (P Gain), and a 16-bit, delta-sigma ADC (P ADC).

7.3.7.1 P Gain Stage

The P Gain stage is designed with precision, low-drift, low-flicker-noise, chopper-stabilized amplifiers. P Gain is implemented as an instrumentation amplifier as shown in Figure 4. The gain of this stage is adjustable using the P_GAIN[4:0] bits in the P_GAIN_SELECT register to accommodate sense elements with a wide range of signal spans.

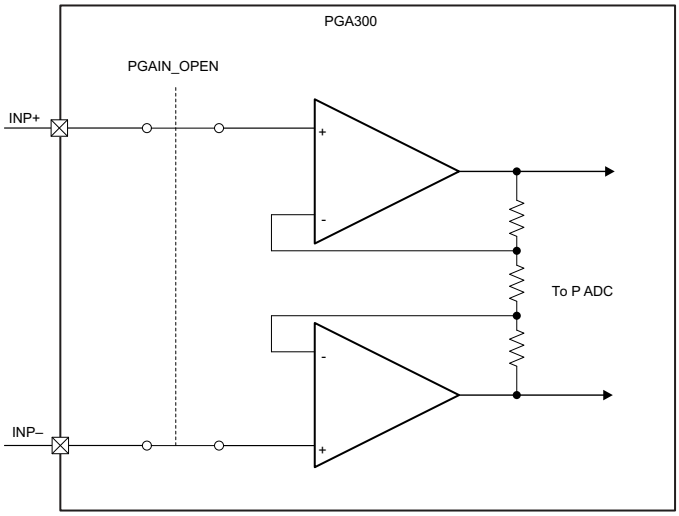


Figure 4. P Gain Stage Diagram

The P Gain value should be set based on the maximum bridge output voltage. The maximum bridge voltage is the maximum sum of bridge offset and bridge span across the entire operating temperature range.

7.3.7.2 P Analog-to-Digital Converter

The P analog-to-digital converter digitizes the voltage output of the P Gain amplifier. The digitized value is available in the PADC_DATA_MSB and PADC_DATA_LSB registers.

7.3.7.2.1 P Sigma-Delta Modulator for P ADC

The sigma-delta modulator used in the P ADC is a 1-MHz, second-order, 3-bit quantizing sigma-delta modulator.

7.3.7.2.2 P Decimation Filter for P ADC

The pressure signal path output conversion time is 128 µs, which equals an output rate of 7.8125 ksamples per second. The output of the decimation filter in the pressure signal path is a 16-bit *signed* value. Some example decimation output codes for given differential voltages at the input of the sigma-delta modulator are shown in Table 1.

Table 1. Input Voltage to Output Counts for the P ADC

SIGMA-DELTA MODULATOR DIFFERENTIAL INPUT VOLTAGE	16-BIT NOISE-FREE DECIMATOR OUTPUT
–2.5 V	–32 768 (0x8000)
–1.25 V	–16 384 (0xC000)
0 V	0 (0x0000)
1.25 V	16 383 (0x3FFF)
2.5 V	32 767 (0x7FFF)

7.3.8 Temperature Measurement Signal Chain

The temperature measurement signal chain of the PGA300 consists of a programmable gain amplifier stage (T Gain) and a 16-bit, delta-sigma ADC (T ADC).

7.3.8.1 T Gain Stage

The device has the ability to perform temperature compensation via an internal or external temperature sensor. The user can select the source of the temperature measurement with the TEMP_MUX_CTRL[3:0] bits in the TEMP_CTRL register. The device connects to an external temperature sensor via the INT+ and INT– pins.

The T Gain block is constructed with a low-flicker-noise, low-offset, chopper-stabilized amplifier. The gain is configured using the T_GAIN[1:0] bits in the T_GAIN_SELECT register. Figure 5 shows the T Gain amplifier topology.

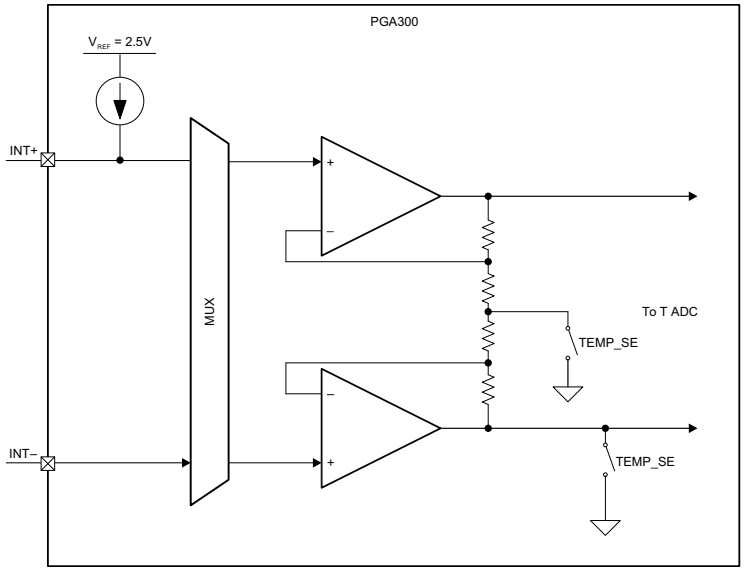


Figure 5. T Gain Stage Diagram

The T Gain amplifier can be configured for single-ended or differential operation using the TEMP_SE bit in the TEMP_SE register. When the T Gain amplifier is configured for single-ended operation, the differential voltage converted by the T ADC is with respect to ground. The T Gain amplifier must be set up for either single-ended or differential configuration, depending on the source of signal to the T Gain stage. Table 2 shows the configuration that the user must select for the different temperature sources.

Table 2. T Gain Configuration

TEMPERATURE SOURCE	T GAIN CONFIGURATION
Internal temperature sensor	Single-ended
External temperature sensor with one terminal of the sensor connected to ground	Single-ended
External temperature sensor with neither terminal of the sensor connected to ground	Differential

The T Gain value must be set based on the temperature sense element used:

- For the internal temperature sensor, set T Gain = 5 V/V
- For an external temperature sensor such as a PTC thermistor, set T Gain = 20 V/V

7.3.8.2 T Analog-to-Digital Converter

The T analog-to-digital converter digitizes the T Gain amplifier output. The digitized value is available in the TADC_DATA_MSB and TADC_DATA_LSB registers.

7.3.8.2.1 T Sigma-Delta Modulator for T ADC

The sigma-delta modulator used in the T ADC is a 1-MHz, second-order, 3-bit quantizing sigma-delta modulator.

7.3.8.2.2 T Decimation Filters for T ADC

The temperature signal path contains a decimation filter with an internal output rate of 128 µs.

The output of the decimation filter in the temperature signal path is a 16-bit *signed* value. Some example decimation output codes for given differential voltages at the input of the sigma-delta modulator are shown in Table 3.

Table 3. Input Voltage to Output Codes Relationship for T ADC

SIGMA-DELTA MODULATOR DIFFERENTIAL INPUT VOLTAGE	16-BIT NOISE-FREE DECIMATOR OUTPUT
–2.5 V	–32 768 (0x8000)
–1.25 V	–16 384 (0xC000)
0 V	0 (0x0000)
1.25 V	16 383 (0x3FFF)
2.5 V	32 767 (0x7FFF)

The nominal relationship between the internal temperature sensor and the 16-bit T ADC code for T Gain = 5 V/V is shown in Equation 1.

$$\text{T ADC Code} = 25.9\ \text{Codes/°C} \times \text{TEMP} + 6680\ \text{Codes} \quad (1)$$

where

- TEMP is temperature in °C

7.3.9 DAC Output

The device includes a 14-bit digital-to-analog converter that produces an absolute output voltage with respect to the accurate reference voltage or a ratiometric output voltage with respect to the PWR supply.

When the device undergoes a reset, the DAC registers are driven to the 0x0000 code.

The PGA300 integrates a 40-kΩ filter resistor at the output of the DAC, as shown in Figure 6. Together with an external capacitor connected to the DACCAP pin, an RC low-pass filter can be implemented between the DAC output and the DAC gain amplifier. The external capacitor can be disconnected by opening switch S_1. The DACCAP_EN bit in the OP_STAGE_CTRL register controls the state of the S_1 switch.

7.3.9.1 Ratiometric vs Absolute Output Mode

The DAC output can be configured to be either in ratiometric-to-PWR mode or independent-of-PWR (or absolute) mode using the DAC_RATIOMETRIC bit in the DAC_CONFIG register.

NOTE

In ratiometric mode, changes in the V_{PWR} voltage result in a proportional change in the DAC output voltage because the reference for the DAC is derived from V_{PWR}.

7.3.10 DAC Gain Stage

The DAC gain amplifier is a configurable buffer stage following the DAC output. The DAC gain amplifier can be configured to operate in voltage amplification mode for voltage output or current amplification mode for 4-mA to 20-mA applications. In voltage output mode, the DAC gain is set to one of four possible gain settings using the DAC_GAIN[2:0] bits in the OP_STAGE_CTRL register, as shown in Figure 6. In current output mode the gain of the DAC gain amplifier is fixed and cannot be changed.

The final stage of the DAC gain amplifier is connected to PWR and ground, thus providing the ability to drive the V_{OUT} voltage close to the V_{PWR} voltage.

The DAC gain amplifier also offers a COMP pin in order to allow implementing compensation when driving large capacitive loads. See the *PGA900 DAC Output Stability* application note and additional documentation in the *Related Documentation* section for details.

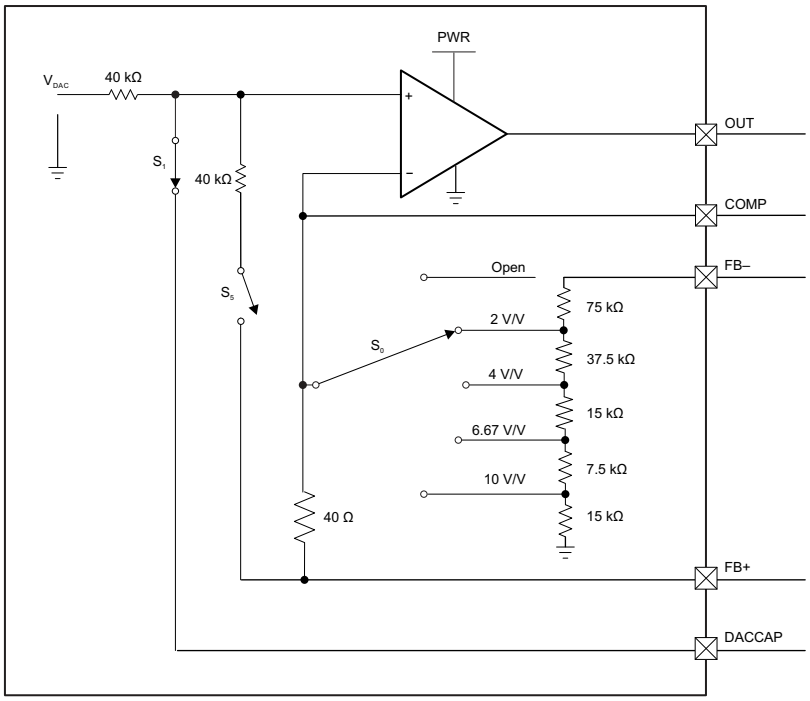


Figure 6. DAC Gain Stage Diagram

7.3.11 Digital Compensation and Filter

The PGA300 implements digital gain and offset compensation as well as a third-order temperature (TC) and nonlinearity (NL) correction of the pressure and temperature inputs. The corrected output is filtered using a second-order IIR filter and then written to the DAC as shown in Figure 7.

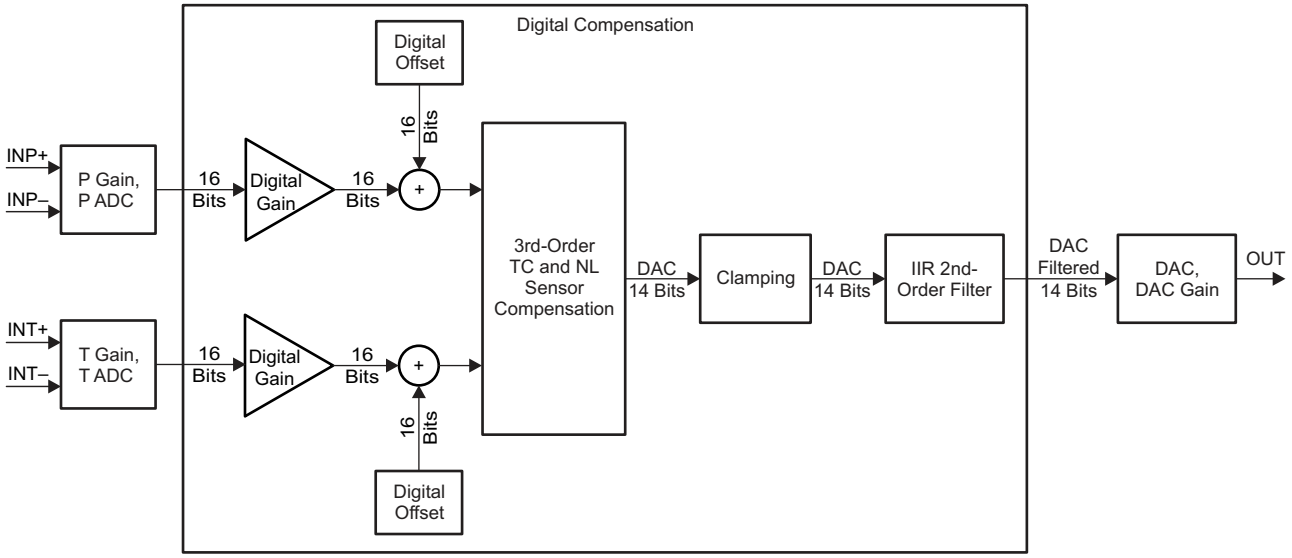


Figure 7. Digital Compensation and Filter Block Diagram

7.3.11.1 Digital Gain and Offset Compensation

The PGA300 implements digital gain and offset compensation for both pressure and temperature signal chains. Equation 2 and Equation 3 show the relationship between the outputs of the P ADC and T ADC, respectively and the gain and offset compensated pressure and temperature values:

$$P = a_P(P\ ADC + b_P) \quad (2)$$

$$T = a_T(T\ ADC + b_T) \quad (3)$$

where

- a_P and a_T are the digital gain coefficients programmed in the PADC_GAIN[15:0] and TADC_GAIN[15:0] bits respectively
- b_P and b_T are the digital offset coefficients programmed in the PADC_OFFSET[15:0] and TADC_OFFSET[15:0] bits respectively
- P is the gain and offset compensated pressure value
- T is the gain and offset compensated temperature value
- P ADC is the pressure digital output
- T ADC is the temperature digital output

For sensors with larger offset voltages or sensor bridges with low or high common-mode voltages, amplifying and offsetting the P ADC value in the digital domain can be useful. The digital gain and offset compensation allows the PGA300 to cancel the offset and amplify the signal further before being used by the temperature and nonlinearity compensation algorithm.

7.3.11.2 Temperature and Nonlinearity Compensation

The PGA300 implements a third-order TC and NL compensation of the bridge offset, bridge span, and bridge nonlinearity. Equation 4 shows the digital temperature and nonlinearity compensation algorithm implemented in the PGA300:

$$DAC = (h_0 + h_1T + h_2T^2 + h_3T^3) + (g_0 + g_1T + g_2T^2 + g_3T^3) \times P + (n_0 + n_1T + n_2T^2 + n_3T^3) \times P^2 + (m_0 + m_1T + m_2T^2 + m_3T^3) \times P^3 \quad (4)$$

where

- DAC = Digitally compensated value at the input of the DAC
- h_x, g_x, n_x and m_x are the TC and NL compensation coefficients programmed in EEPROM
- P is the offset and gain compensated pressure value
- T is the offset and gain compensated temperature value

Equation 4 has 16 coefficients, and therefore requires at least 16 different measurement points to compute a unique set of 16 coefficients.

The 16 different P ADC and T ADC measurements can be made, for example, at four temperatures and at four different pressures:

- The P Gain and T Gain values must be set to a fixed value for all measurements.
- At each measurement point, the P ADC value and the T ADC value must be recorded in order to compute the 16 coefficients.
- Measuring P ADC and T ADC at different temperatures and pressures may sometimes be expensive. In this case, there are three approaches:
  - Use a model of the bridge to estimate the P ADC and T ADC measurements instead of actually measuring them.
  - Use *batch modeling*, in which a family of sense elements is characterized across temperature, and the TC coefficients of the compensation equation are determined prior to calibration. On a production line, measurements are made at a limited number of temperature and pressure set points, and coefficients are adjusted accordingly. Discuss details with TI application engineers on the E2E community.
  - Reduce the number of coefficients by reducing the order of TC compensation. Discuss the procedure to use fewer coefficients with TI application engineers on the E2E community.

7.3.11.2.1 Operating Without TC and NL Compensation

The equation for P ADC-to-DAC conversion when operating without TC and NL compensation is shown in Equation 5.

$$DAC = OFFSET_{PA2D} + GAIN_{PA2D} \times P\ ADC \quad (5)$$

To use the PGA without TC and NL compensation set the h_x, g_x, n_x and m_x coefficients in EEPROM to the following values:

- $h_0 = OFFSET_{PA2D} / 4$
- h_1 to h_3 = 0x0000
- $g_0 = GAIN_{PA2D} \times 2^{14}$
- g_1 to g_3 = 0x0000
- n_0 to n_3 = 0x0000
- m_0 to m_3 = 0x0000

Consider an example of scaling the positive half of the 16-bit P ADC to a 14-bit DAC value. In this case, $OFFSET_{PA2D}$ = 0 and $GAIN_{PA2D}$ = 0.5. Therefore, h_0 = 0, and $g_0 = 2^{13}$.

7.3.11.2.2 Temperature Compensation Using the Internal Temperature Sensor

Temperature compensation can be performed using the internal temperature sensor with T Gain = 5 V/V. Typical internal temperature sensor ADC values at the different temperatures are shown in Table 4.

Table 4. T ADC Value for the Internal Temperature Sensor

TEMPERATURE	T ADC VALUE (Typ)
–40°C	0x160C
0°C	0x1A18
150°C	0x2945

For T ADC output codes at intermediate temperatures, use linear interpolation.

7.3.11.3 Clamping

The output of the digital compensation is clamped. The low and high clamp values are programmable using the LOW_CLAMP[15:0] and HIGH_CLAMP[15:0] bits in the EEPROM. In addition, a normal operating output can be configured using the NORMAL_LOW[15:0] and NORMAL_HIGH[15:0] bits in the EEPROM. Any output value from the digital compensation that exceeds the NORMAL_HIGH threshold gets driven to the HIGH_CLAMP value. Similarly, any output value below the NORMAL_LOW threshold gets driven to the LOW_CLAMP value. Figure 8 shows an example of the clamping feature for 0-V to 5-V voltage output mode. The output of the compensation can be configured in a similar way when the 4-mA to 20-mA current output mode is used. In such case, however, the LOW_CLAMP[15:0] value must be larger than the maximum supply current needed for normal operation of the device.

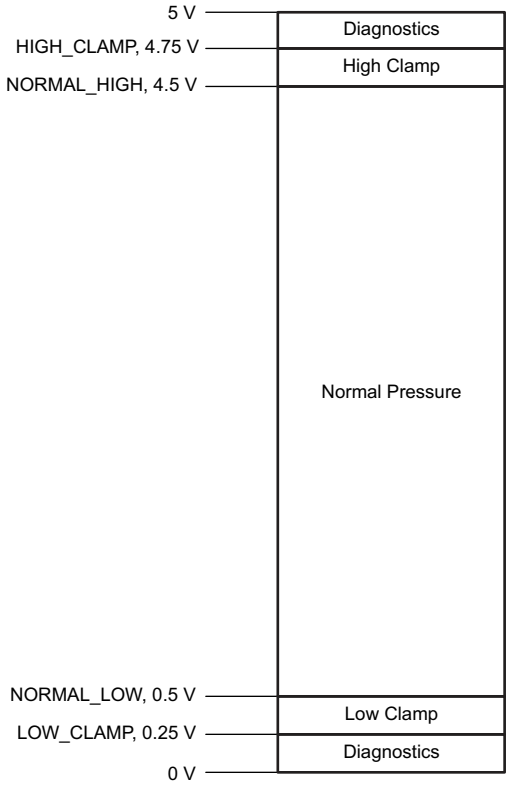


Figure 8. Example of Clamping the Digital Compensation Output

7.3.11.4 Digital IIR Filter

The IIR filter is implemented as follows:

$$w(n) = (a_0 \times DAC(n) + a_1 \times w(n-1) + a_2 \times w(n-2)) \quad (6)$$

$$DACF(n) = (b_0 \times w(n) + b_1 \times w(n-1) + b_2 \times w(n-2)) \quad (7)$$

where

- a_0, a_1, a_2, b_0, b_1, and b_2 are the IIR filter coefficients stored in EEPROM.
- DAC(n) is the DAC output prior to the IIR filter.
- DACF(n) is the output of the PGA300 after the second-order IIR filter.

7.3.11.4.1 Filter Coefficients

7.3.11.4.1.1 No Filtering

If filtering must be disabled, set a_0 = 0x0000.

7.3.11.4.1.2 Filter Coefficients for P ADC Sampling Rate = 128 µs

Table 5 shows the different filter coefficients that must be programmed to achieve a certain filter cutoff frequency.

Table 5. Filter Cutoff Frequency and Filter Coefficients

CUTOFF FREQUENCY (Hz)	a_0	a_1	a_2	b_0	b_1	b_2
600	0x4000	0xAAA1	0x2060	0x0B01	0x1602	0x0B01
700	0x4000	0xB169	0x1CEE	0x0E57	0x1CAF	0x0E57
800	0x4000	0xB818	0x19E0	0x11F8	0x23F0	0x11F8
900	0x4000	0xBEAE	0x172D	0x15DB	0x2BB7	0x15DB
1000	0x4000	0xC52D	0x14CE	0x19FB	0x33F6	0x19FB
1100	0x4000	0xCB95	0x12BC	0x1E52	0x3CA3	0x1E52
1200	0x4000	0xD1EA	0x10F2	0x22DC	0x45B8	0x22DC
1300	0x4000	0xD82D	0x0F6A	0x2798	0x4F2F	0x2798
1400	0x4000	0xDE61	0x0E21	0x2C82	0x5905	0x2C82
1500	0x4000	0xE487	0x0D14	0x319B	0x6336	0x319B
1600	0x4000	0xEAA3	0x0C3F	0x36E2	0x6DC4	0x36E2
1700	0x4000	0xF0B6	0x0BA1	0x3C56	0x78AD	0x3C56
1800	0x4000	0xF6C3	0x0B37	0x41FA	0x83F4	0x41FA
1900	0x4000	0xFCCC	0x0B02	0x47CE	0x8F9C	0x47CE
2000	0x4000	0x02D4	0x0B01	0x4DD4	0x9BA9	0x4DD4
2100	0x4000	0x08DD	0x0B33	0x540F	0xA81F	0x540F
2200	0x4000	0x0EE9	0x0B99	0x5A82	0xB504	0x5A82
2300	0x4000	0x14FC	0x0C33	0x612F	0xC25E	0x612F
2400	0x4000	0x1B17	0x0D05	0x681B	0xD037	0x681B
2500	0x4000	0x213C	0x0E0F	0x6F4B	0xDE96	0x6F4B

7.3.12 Diagnostics

The PGA300 implements the diagnostics described in Table 6.

Table 6. Diagnostics Overview

DIAGNOSTICS DESCRIPTION	ACTION
Execution-timing error	DAC is disabled and digital compensation logic set to a reset state
Checksum error of internal logic	DAC is disabled and digital compensation logic set to a reset state
EEPROM is corrupted or EEPROM CRC_GOOD = 0b0	DAC code is driven to 0 code
Power-supply and signal-chain errors	DAC output is driven to the value determined by the DAC_FAULT_LSB and DAC_FAULT_MSB registers

All the foregoing diagnostics are enabled by setting the DIAG_ENABLE bit in the DIAG_ENABLE register. To disable diagnostics, set the DIAG_ENABLE bit to 0b0.

7.3.12.1 Power-Supply Diagnostics

The PGA300 includes circuits to monitor the accurate reference and power supplies for faults. Specifically, the following signals are monitored for over- and undervoltages:

- AVDD supply voltage
- DVDD supply voltage
- Bridge supply voltage
- Internal oscillator supply voltage
- Accurate reference output voltage

The *Electrical Characteristics: Diagnostics* table lists the voltage thresholds for each of the power rails.

7.3.12.2 Signal Chain Diagnostics

The PGA300 includes circuits to monitor the P and T signal chains for faults. This section describes the faults monitored by the PGA300. Figure 9 and Figure 10 illustrate the implementation of the P Gain and T Gain diagnostics.

7.3.12.2.1 P Gain and T Gain Input Diagnostics

The PGA300 includes circuits to monitor for sensor connectivity faults. Specifically, the device monitors the bridge sensor pins for opens (including loss of connection from the sensor), short to ground, and short to sensor supply. The monitoring is accomplished by comparing the voltages at the INP+ and INP– pins with the overvoltage (INP_OV) and undervoltage (INP_UV) thresholds specified in the *Electrical Characteristics: Diagnostics* table.

Bridge-sensor connectivity faults are detected through the use of internal pulldown resistors. The value of the pulldown resistors and the threshold is configured through the PD[1:0] and THRS[2:0] bits in the AFEDIAG_CFG register.

The device also includes an overvoltage monitor at the INT+ and INT– pins through the use of 1-MΩ pullup resistors.

The pullup and pulldown resistors can be disconnected through the DIS_R_P and DIS_R_T bits in the AFEDIAG_CFG register.

7.3.12.2.2 P Gain and T Gain Output Diagnostics

The PGA300 includes monitors that verify that the output signal of each gain stage is within a certain range. The P Gain and T Gain monitors ensure that the gain stages in the signal chain are working correctly. Comparators at the individual P Gain and T Gain outputs compare the voltages with the overvoltage (PGAIN_OV, TGAIN_OV) and undervoltage (PGAIN_UV, TGAIN_UV) thresholds specified in the *Electrical Characteristics: Diagnostics* table.

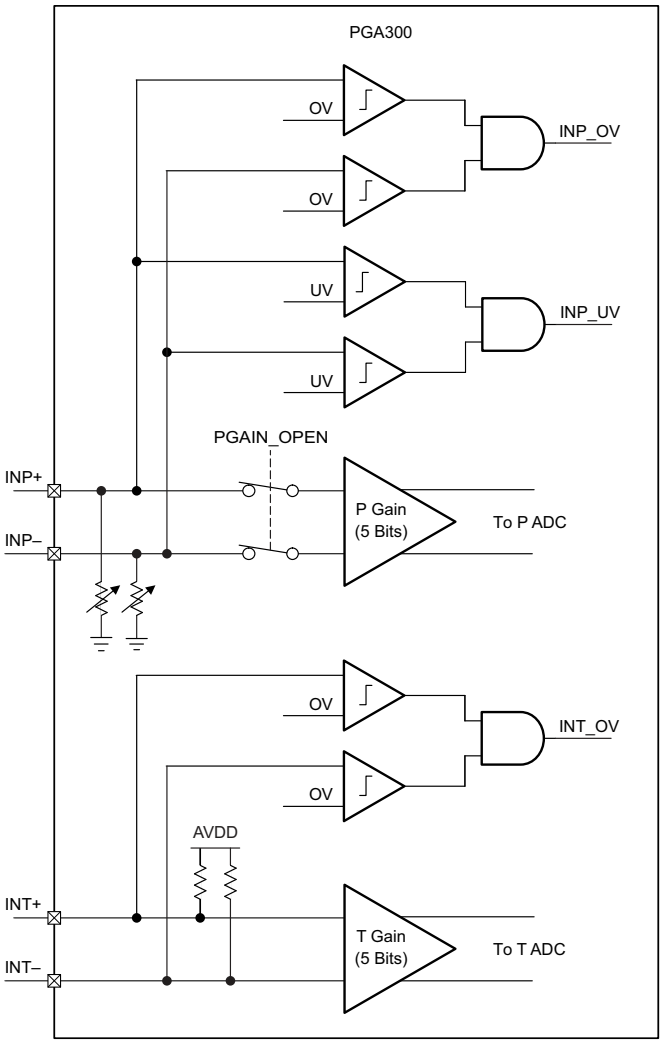


Figure 9. Block Diagram of P Gain and T Gain Input Diagnostics

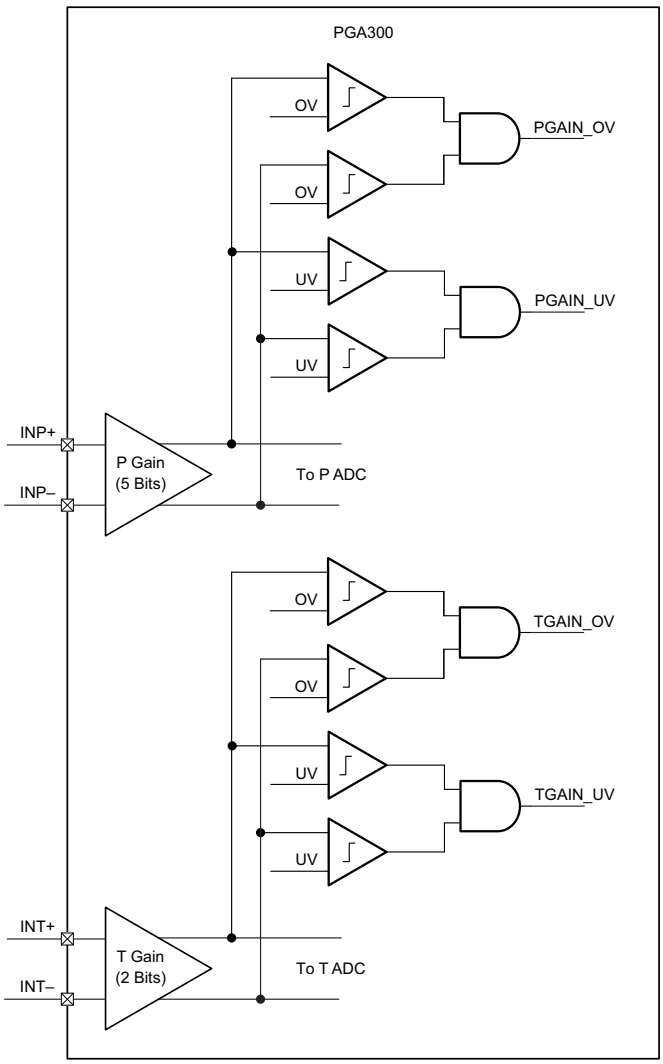


Figure 10. Block Diagram of P Gain and T Gain Output Diagnostics

7.3.12.2.3 Masking Signal Chain Diagnostics

The signal chain diagnostics can be selectively enabled and disabled using the bits in the AFEDIAG_MASK register. Table 7 describes the mask bits. Setting a bit to 0b1 enables detection of the corresponding fault and setting the bit to 0b0 disables the detection of the corresponding fault.

Table 7. Signal Chain Fault Masking Bits

BIT	DESCRIPTION
0	INP+ or INP– overvoltage
1	INP+ or INP– undervoltage
2	INT+ or INT– overvoltage
3	N/A
4	P Gain output overvoltage
5	P Gain output undervoltage
6	T Gain output overvoltage
7	T Gain output undervoltage

7.3.12.3 Fault Detection Timing

The PGA300 fault-monitoring circuits monitor faults either at power up or periodically. Table 8 describes the fault-detection timing.

Table 8. Fault Detection Timing

FAULT	POWER UP OR RUN TIME	MINIMUM TIME AFTER FAULT OCCURS	MAXIMUM TIME AFTER FAULT OCCURS
Execution-timing error	Run time	500 ms	—
Checksum error of internal logic	Run time	500 ms	—
EEPROM is corrupted or EEPROM CRC_GOOD = 0b0	Power up only (EEPROM is accessed only at power up)	N/A	N/A
Power supply and signal chain errors	Run time	8 ms	16 ms

7.4 Device Functional Modes

7.4.1 Operating Modes

The PGA300 has two operating modes: execution and configuration mode. The flow chart in Figure 11 shows how to transition between the two modes.

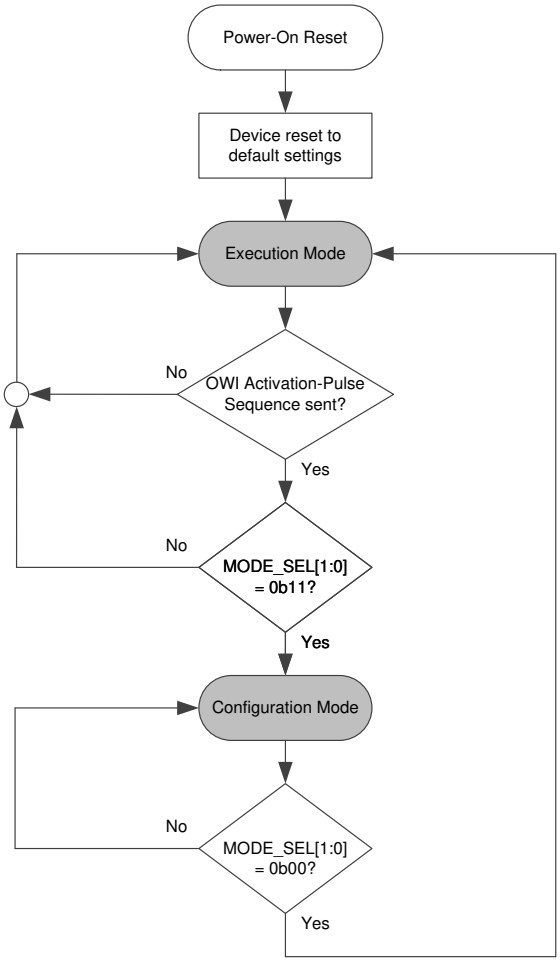


Figure 11. Operating Flow Chart

7.4.1.1 Execution Mode

In execution mode the T ADC and P ADC are converting, the DAC is enabled, and the DAC gain stage is driving the voltage or current on the OUT pin. The ADC conversion results are fed to the digital compensation and filter blocks and then output to the DAC. The device control and status registers and EEPROM cannot be programmed in execution mode.

7.4.1.2 Configuration Mode

Use the configuration mode to read or write the device control and status registers and EEPROM. The DAC is disabled by default in configuration mode and not connected to the output of the digital compensation and filter blocks. The following sequence must be followed to enter configuration mode:

1. Send the OWI activation-pulse sequence.
2. Set the MODE_SEL[1:0] bits in the MODE_CTRL register to 0b11.

To exit configuration mode and return to execution mode, set the MODE_SEL[1:0] bits in the MODE_CTRL register to 0b00.

Device Functional Modes (continued)

7.4.2 Output Modes

The PGA300 offers two output modes: voltage output and 4-mA to 20-mA current output mode. The external components and connections of the PGA300 depend on the selected output mode.

7.4.2.1 Voltage Output Mode

When configured for voltage output mode, the FB– pin must be connected to the OUT pin. If the OUT pin is driving a large capacitive load, a compensation capacitor can be connected to the COMP pin and an isolation resistor can be placed between the OUT and FB– pins. The FB+ pin is not used in voltage output mode.

To configure the PGA300 for voltage output mode set the following bits in the OP_STAGE_CTRL register:

1. 4_20MA_EN = 0b0 to disable current output mode.
2. DAC_GAIN[2:0] = 0b001, 0b010, 0b100, or 0b110 to select one of the four available gain settings and to enable voltage output mode.

In addition set the DAC_RATIOMETRIC bit in the DAC_CONFIG register to the desired output method, either absolute or ratiometric voltage output mode.

7.4.2.2 Current Output Mode

When configured in current output mode, the OUT pin is driving the base of a bipolar junction transistor (BJT); see Figure 74. The COMP pin is connected to the emitter of the BJT and the FB+ pin is connected to the return terminal of the supply. The FB– pin is not used in current output mode.

To configure the PGA300 for current output mode set the following bits in the OP_STAGE_CTRL and DAC_CONFIG registers:

1. 4_20MA_EN = 0b1 to enable current output mode.
2. DAC_GAIN[2:0] = 0b000 to disable voltage output mode.
3. DAC_RATIOMETRIC = 0b0 to select absolute output mode.

7.5 Programming

7.5.1 One-Wire Interface (OWI)

The device includes a OWI digital communication interface. The function of the OWI is to enable writes to and reads from the control and status registers as well as the EEPROM while in configuration mode.

7.5.1.1 Overview of OWI

The OWI digital communication is a master-slave communication link in which the PGA300 operates as a slave device only. The master device controls when data transmission begins and ends. The slave device does not transmit data back to the master until commanded to do so by the master.

The PWR pin of the PGA300 is used as the OWI line, so that when the PGA300 is embedded inside a system module, only two pins are needed (PWR and GND) for communication. The OWI master communicates with the PGA300 by modulating the voltage on the PWR pin, whereas the PGA300 communicates with the master by modulating the current on the PWR pin. The OWI master activates OWI communication by generating an activation-pulse sequence on the PWR pin.

Figure 12 shows a functional equivalent circuit for the structure of the OWI circuitry.

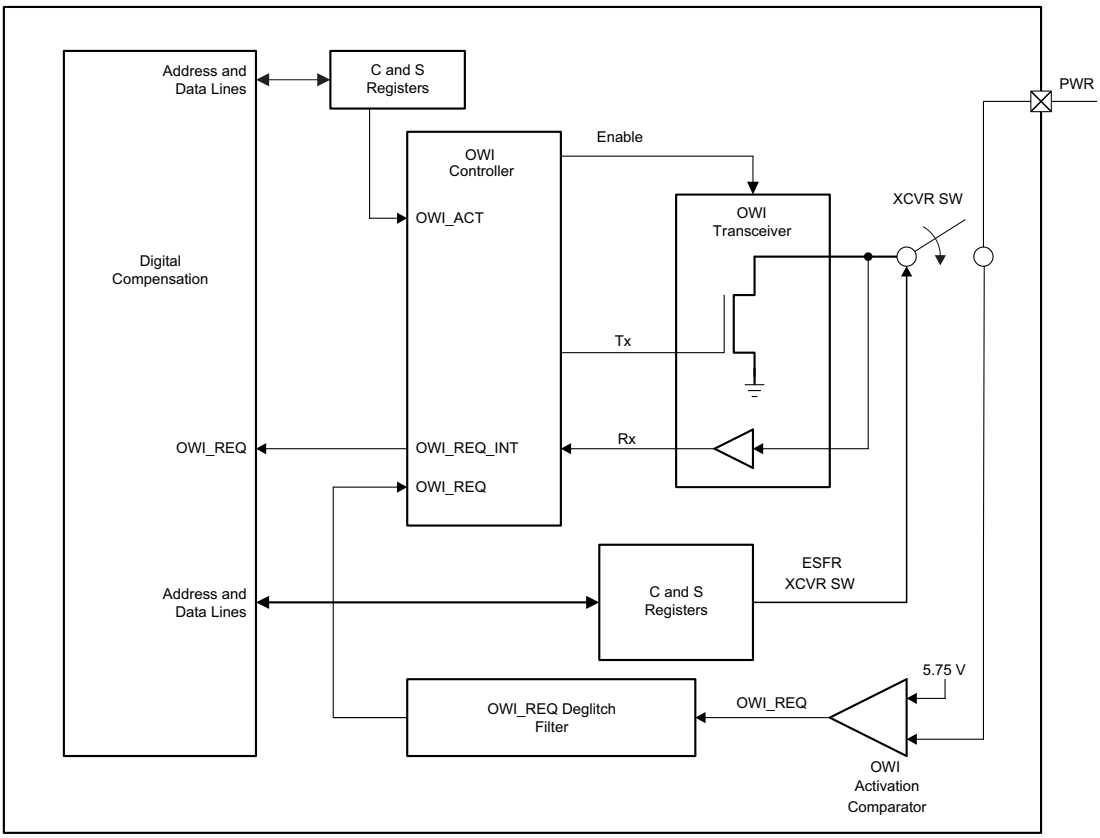


Figure 12. OWI System Components

Programming (continued)

7.5.1.2 Activating and Deactivating the OWI

7.5.1.2.1 Activating OWI Communication

The OWI master initiates OWI communication, as shown in Figure 13, by generating an OWI activation-pulse sequence on the PWR pin. When the PGA300 receives a valid OWI activation-pulse sequence, the device prepares itself for OWI communication.

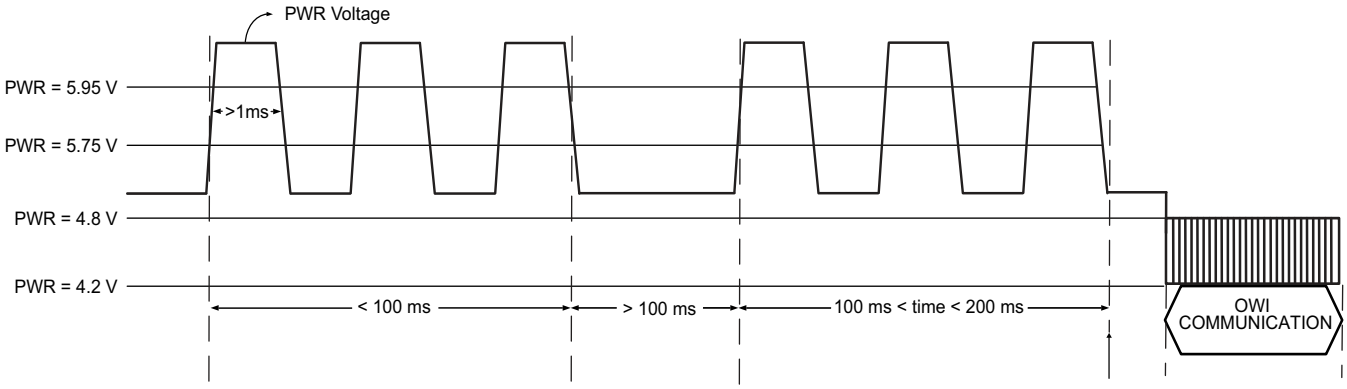


Figure 13. OWI Activation-Pulse Sequence Using Overvoltage Drive

7.5.1.2.2 Deactivating OWI Communication

In order to deactivate OWI communication and restart the execution mode of the PGA300, set the MODE_SEL[1:0] bits to 0b00 in the MODE_CTRL register.

7.5.1.3 OWI Protocol

7.5.1.3.1 OWI Frame Structure

7.5.1.3.1.1 Standard Field Structure

Data is transmitted on the one-wire interface in byte-sized packets. The first bit of the OWI field is the start bit. The next 8 bits of the field are data bits to be processed by the OWI control logic. The final bit in the OWI field is the stop bit. A group of fields make up a transmission frame. A transmission frame is composed of the fields necessary to complete one transmission operation on the one-wire interface. The standard field structure for an OWI field is shown in Figure 14.

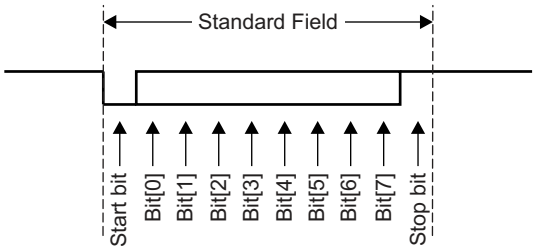


Figure 14. Standard OWI Field

Programming (continued)

7.5.1.3.1.2 Frame Structure

A complete one-wire data transmission operation is done in a frame with the structure as shown in Figure 15.

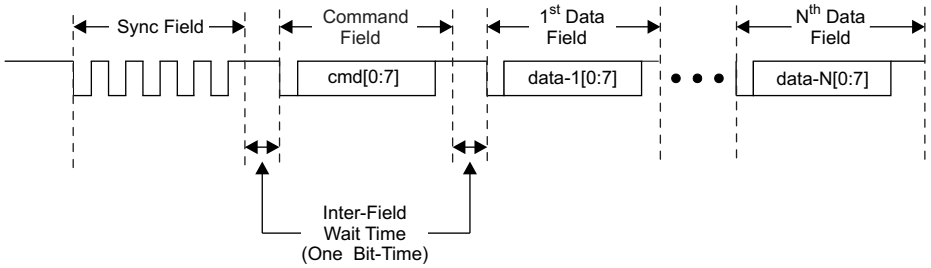


Figure 15. OWI Transmission Frame, N = 1 to 8

Each transmission frame must have a synchronization field and a command field followed by zero to a maximum of eight data fields. The sync field and command fields are always transmitted by the master device. The data fields may be transmitted either by the master or the slave, depending on the command given in the command field. The command field determines the direction of travel of the data fields (master-to-slave or slave-to-master). The number of data fields transmitted is also determined by the command in the command field. The inter-field wait time is optional and may be necessary for the slave or the master to process data that has been received.

NOTE

If the OWI remains idle in either the logic-0 or logic-1 state for more than 15 ms, then the PGA300 communication resets and requires a sync field as the next data transmission from the master.

7.5.1.3.1.3 Sync Field

The sync field is the first field in every frame that is transmitted by the master. The sync field is used by the slave device to compute the bit width transmitted by the master. This bit width is used to accurately receive all subsequent fields transmitted by the master. The format of the sync field is shown in Figure 16.

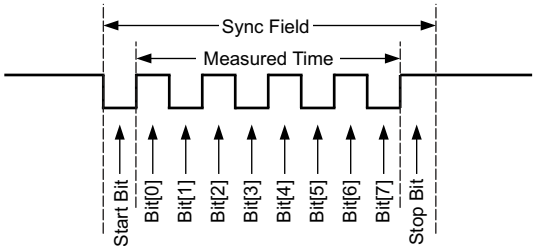


Figure 16. OWI Sync Field

NOTE

The width of consecutive sync-field bits is measured and compared to determine if a valid sync field was transmitted to the PGA300. If the difference in bit widths of any two consecutive sync-field bits is greater than ±25%, then the PGA300 ignores the rest of the OWI frame; that is, the PGA300 does not respond to the OWI message.

Programming (continued)

7.5.1.3.1.4 Command Field

The command field is the second field in every frame sent by the master. The command field contains instructions about what to do with and where to send the data that is transmitted to the slave. The command field can also instruct the slave to send data back to the master during a read operation. The number of data fields to be transmitted is also determined by the command in the command field. The format of the command field is shown in Figure 17.

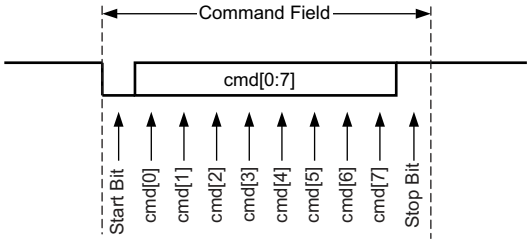


Figure 17. OWI Command Field

7.5.1.3.1.5 Data Fields

After the master has transmitted the command field in the transmission frame, zero or more data fields are transmitted to the slave (write operation) or to the master (read operation). The data fields can be raw EEPROM data or address locations in which to store data. The format of the data is determined by the command in the command field. The typical format of a data field is shown in Figure 18.

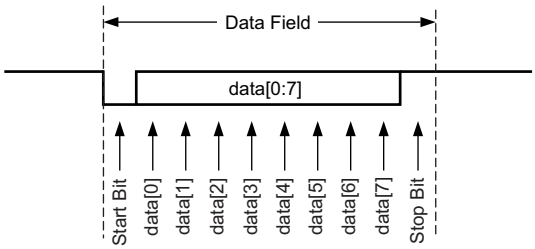


Figure 18. OWI Data Field

Programming (continued)

7.5.1.3.2 OWI Commands

The PGA300 supports the following five OWI commands:

1. OWI write
2. OWI read initialization
3. OWI read response
4. OWI burst write to EEPROM cache
5. OWI burst read from EEPROM cache

Table 9. OWI Control and Status Register Page Decode

P2	P1	P0	CONTROL AND STATUS REGISTER PAGE
0	0	0	Control and status register page 0
0	0	1	Reserved
0	1	0	Control and status register page 2
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Control and status register page 5
1	1	0	Reserved
1	1	1	Reserved

7.5.1.3.2.1 OWI Write Command

FIELD LOCATION	DESCRIPTION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Command field	Basic write command	0	P2	P1	P0	0	0	0	1
Data field 1	Destination address	A7	A6	A5	A4	A3	A2	A1	A0
Data field 2	Data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0

The P2, P1, and P0 bits in the command field determine the control and status register page that is being accessed by the OWI. The control and status register page decode is shown in Table 9.

7.5.1.3.2.2 OWI Read-Initialization Command

FIELD LOCATION	DESCRIPTION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Command field	Read-initialization command	0	P2	P1	P0	0	0	1	0
Data field 1	Fetch address	A7	A6	A5	A4	A3	A2	A1	A0

The P2, P1, and P0 bits in the command field determine the control and status register page that is being accessed by the OWI. The control and status register page decode is shown in Table 9.

7.5.1.3.2.3 OWI Read-Response Command

FIELD LOCATION	DESCRIPTION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Command field	Read-response command	0	1	1	1	0	0	1	1
Data field 1	Data retrieved (OWI drives data out)	D7	D6	D5	D4	D3	D2	D1	D0

7.5.1.3.2.4 OWI EEPROM Cache Burst-Write Command

FIELD LOCATION	DESCRIPTION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Command field	Burst-write command (8 bytes)	1	1	0	1	0	0	0	0
Data field 1	First data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0
Data field 2	Second data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0
Data field 3	Third data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0
Data field 4	Fourth data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0
Data field 5	Fifth data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0
Data field 6	Sixth data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0
Data field 7	Seventh data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0
Data field 8	Eighth data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0

7.5.1.3.2.5 OWI EEPROM Cache Burst-Read Command

FIELD LOCATION	DESCRIPTION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Command field	Burst-read command (8 bytes)	1	1	0	1	0	0	1	1
Data field 1	First data byte retrieved. EEPROM cache byte 0	D7	D6	D5	D4	D3	D2	D1	D0
Data field 2	Second data byte retrieved. EEPROM cache byte 1	D7	D6	D5	D4	D3	D2	D1	D0
Data field 3	Third data byte retrieved. EEPROM cache byte 2	D7	D6	D5	D4	D3	D2	D1	D0
Data field 4	Fourth data byte retrieved. EEPROM cache byte 3	D7	D6	D5	D4	D3	D2	D1	D0
Data field 5	Fifth data byte retrieved. EEPROM cache byte 4	D7	D6	D5	D4	D3	D2	D1	D0
Data field 6	Sixth data byte retrieved. EEPROM cache byte 5	D7	D6	D5	D4	D3	D2	D1	D0
Data field 7	Seventh data byte retrieved. EEPROM cache byte 6	D7	D6	D5	D4	D3	D2	D1	D0
Data field 8	Eighth data byte retrieved. EEPROM cache byte 7	D7	D6	D5	D4	D3	D2	D1	D0

7.5.1.3.3 OWI Operations

7.5.1.3.3.1 Write Operation

The write operation on the one-wire interface consists of a single OWI frame. The command field of the write operation specifies which control and status register page to write to. The first data field specifies which address within that control and status register page to write to. The second data field contains the data to write to the specified register in the slave (that is, the PGA300). Figure 19 shows the write operation. Sending data fields three to eight is optional. The slave ignores those additional data fields.

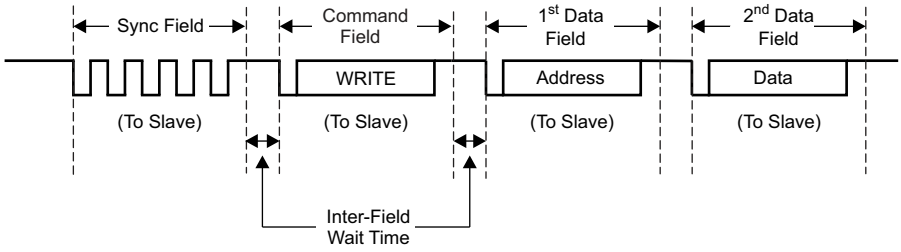


Figure 19. OWI Write Frame

7.5.1.3.3.2 Read Operation

The read operation requires two consecutive OWI frames to move data from the slave to the master. The first frame is the read-initialization frame. This frame tells the slave to retrieve data from a particular register location within the slave device and prepare to send the data over the OWI. The command field of the read-initialization frame specifies which control and status register page to read from. The first data field specifies which address within that control and status register page to read from. Sending data fields two to eight is optional. The slave ignores those additional data fields. The data are not sent until the master commands the data to be sent in the subsequent frame called the read-response frame. During the read-response frame, the data direction changes from master → slave to slave → master immediately after the read-response command field is sent. Enough time elapses between the command field and data field to allow the signal drivers to change direction. This wait time is 20 µs, and the timer for this wait time is located on the slave device. After this wait time is complete, the slave transmits the requested data. The master device is expected to have switched its signal drivers and to be ready to receive data. Figure 20 and Figure 21 show the two read frames that are required to complete a read operation.

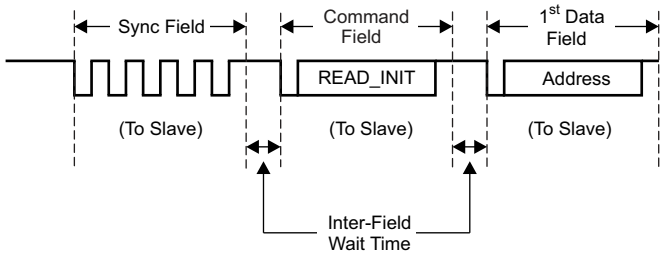


Figure 20. OWI Read-Initialization Frame

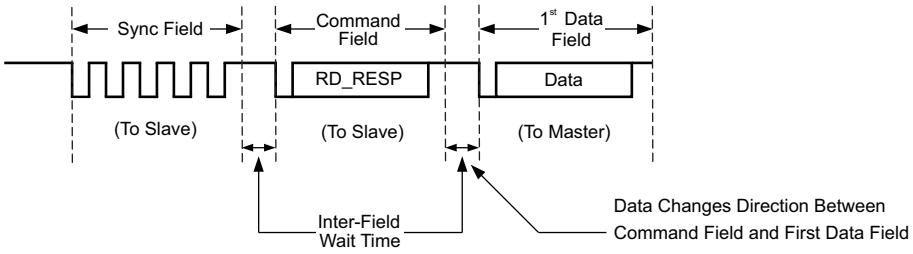


Figure 21. OWI Read-Response Frame

7.5.1.3.3.3 EEPROM Cache Burst Write

The EEPROM cache burst write is used to write 8 bytes of data to the EEPROM cache using one OWI frame to allow fast programming of the EEPROM. The respective EEPROM page must be selected before transferring the contents of the EEPROM cache to the EEPROM memory cells. See the *EEPROM Programming Procedure* section for more details.

7.5.1.3.3.4 EEPROM Cache Burst Read

The EEPROM cache burst read is used to read 8 bytes of data from the EEPROM cache using one OWI frame to allow for fast reading of the EEPROM cache contents. The read process is used to verify the writes to the EEPROM cache.

7.5.2 Memory

7.5.2.1 EEPROM Memory

Figure 22 shows the EEPROM structure of the PGA300. The contents to program into the EEPROM must be transferred to the EEPROM cache before writes; that is, the EEPROM can only be programmed 8 bytes (one page) at a time. EEPROM reads occur without the EEPROM cache. For reading purposes the complete EEPROM is mapped to the address space from 0x00 to 0x7F in the control and status register page 5. Address 0x00 maps to EEPROM page 0, byte 0 and address 0x7F maps to EEPROM page 15, byte 7.

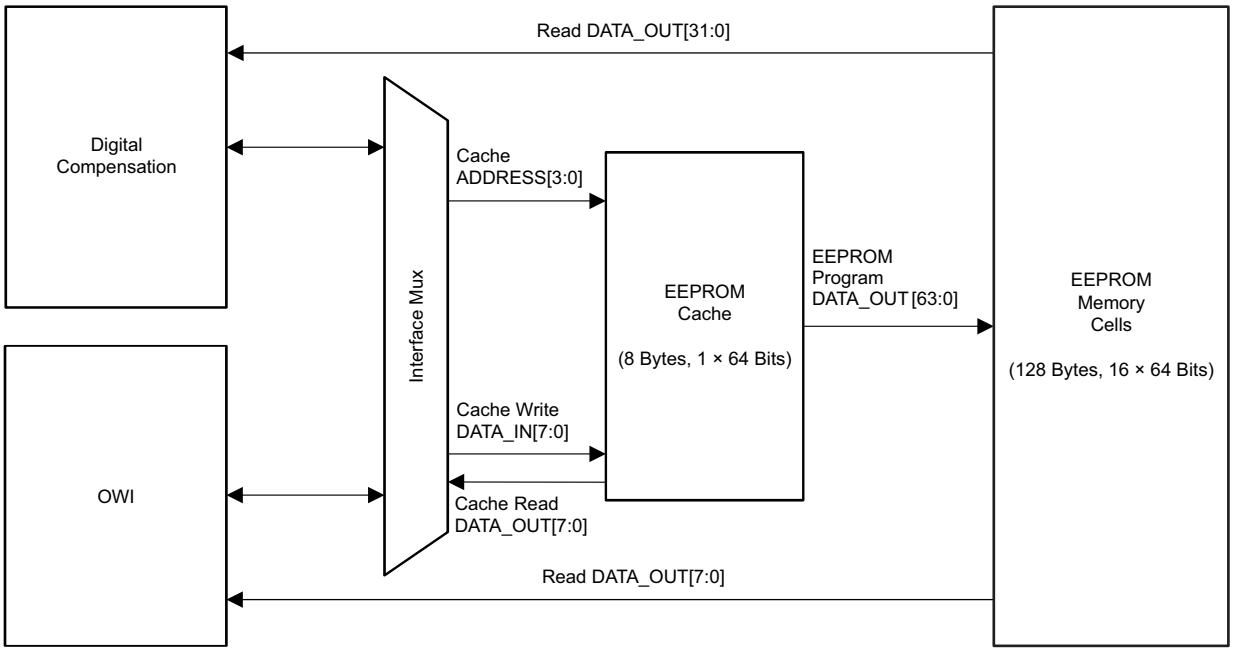


Figure 22. EEPROM Interface Structure

7.5.2.1.1 EEPROM Cache

The EEPROM cache serves as temporary storage of data being transferred to selected EEPROM locations during the programming process.

7.5.2.1.2 EEPROM Programming Procedure

The EEPROM is organized in 16 pages of eight bytes each. The EEPROM memory cells are programmed by writing to the 8-byte EEPROM cache. The contents of the cache is transferred to the EEPROM memory cells determined by the EEPROM memory page in the following way:

1. Write the 4-bit EEPROM page to the ADDR[3:0] bits in the EEPROM_PAGE_ADDRESS register to select the EEPROM page to write to.
2. Load the 8-byte EEPROM cache by writing to the EEPROM_CACHE register space using one of two methods:
   - The OWI EEPROM cache burst-write command to write the complete EEPROM cache in a single OWI frame.
   - Eight individual OWI write operations to addresses 0x80 to 0x87 in the control and status register page 5. All eight bytes must be loaded into the EEPROM_CACHE register.
3. Read back the EEPROM cache as an optional sanity check to verify that the EEPROM cache is written correctly by reading the EEPROM_CACHE register space using one of two methods:
   - The OWI EEPROM cache burst-read command to read the complete EEPROM cache in a single OWI frame.
   - Eight individual OWI read operations from addresses 0x80 to 0x87 in the control and status register page 5.
4. Set the ERASE_AND_PROGRAM bit in the EEPROM_CTRL register. Setting this bit automatically erases the selected EEPROM memory page and programs the page with the contents of the EEPROM_CACHE register. Alternatively, the contents of the EEPROM memory page can be erased by writing 1 to the ERASE bit in the EEPROM_CTRL register, followed by writing 1 to the PROGAM bit in the EEPROM_CTRL register when the erase operation is complete. The status of the erase and program operations can be monitored through the EEPROM_STATUS register.

7.5.2.1.3 EEPROM Programming Current

The EEPROM programming process results in an additional current of 6 mA on the PWR pin for the duration of programming.

7.5.2.1.4 EEPROM Memory Map CRC

The last byte of the EEPROM memory, which is the EEPROM_CRC_VALUE_USER register, is reserved for the memory map CRC. This CRC value covers all data in the EEPROM memory. Every time the EEPROM_CRC_VALUE_USER register is written, the PGA300 calculates the CRC value across the EEPROM memory, places the calculated CRC value in the EEPROM_CRC_VALUE_CALC register, and validates the value against the CRC value programmed in the EEPROM_CRC_VALUE_USER register. If the calculated CRC value in the EEPROM_CRC_VALUE_CALC register matches the value programmed in the EEPROM_CRC_VALUE_USER register, the CRC_GOOD bit is set in the EEPROM_CRC_STATUS register.

The CRC check can also be initiated at any time by setting the CALCULATE_CRC bit in the EEPROM_CRC register. The status of the CRC calculation is available in the CRC_CHECK_IN_PROG bit in the EEPROM_CRC_STATUS register, whereas the result of the CRC validation is available in the CRC_GOOD bit in the EEPROM_CRC_STATUS register.

The CRC calculation pseudo code is as follows:

```
currentCRC8 = 0xFF; // Current value of CRC8

for NextData

D = NextData;

C = currentCRC8;

  begin

      nextCRC8_BIT0 = D_BIT7 ^ D_BIT6 ^ D_BIT0 ^ C_BIT0 ^ C_BIT6 ^ C_BIT7;

      nextCRC8_BIT1 = D_BIT6 ^ D_BIT1 ^ D_BIT0 ^ C_BIT0 ^ C_BIT1 ^ C_BIT6;

      nextCRC8_BIT2 = D_BIT6 ^ D_BIT2 ^ D_BIT1 ^ D_BIT0 ^ C_BIT0 ^ C_BIT1 ^ C_BIT2 ^ C_BIT6;

      nextCRC8_BIT3 = D_BIT7 ^ D_BIT3 ^ D_BIT2 ^ D_BIT1 ^ C_BIT1 ^ C_BIT2 ^ C_BIT3 ^ C_BIT7;

      nextCRC8_BIT4 = D_BIT4 ^ D_BIT3 ^ D_BIT2 ^ C_BIT2 ^ C_BIT3 ^ C_BIT4;

      nextCRC8_BIT5 = D_BIT5 ^ D_BIT4 ^ D_BIT3 ^ C_BIT3 ^ C_BIT4 ^ C_BIT5;

      nextCRC8_BIT6 = D_BIT6 ^ D_BIT5 ^ D_BIT4 ^ C_BIT4 ^ C_BIT5 ^ C_BIT6;

      nextCRC8_BIT7 = D_BIT7 ^ D_BIT6 ^ D_BIT5 ^ C_BIT5 ^ C_BIT6 ^ C_BIT7;

   end

   currentCRC8 = nextCRC8_D8;

endfor
```

NOTE

The EEPROM CRC calculation is complete 340 µs after the digital core starts running at power up.

7.5.3 Control and Status Registers

The internal logic uses the control and status registers to interact with the analog blocks of the device. In configuration mode the settings of the control and status registers take priority over the settings of the EEPROM registers. In execution mode the settings of the EEPROM registers take effect.

7.6 Register Maps

7.6.1 Register Settings

Before the PGA300 can be used in any application, the device must be configured by setting various EEPROM registers to the desired values. Table 10 lists all the EEPROM registers that must be configured and their respective default configurations. The registers are configured by writing to the appropriate EEPROM addresses listed in the *EEPROM Registers* section.

Table 10. Default EEPROM Register Settings

REGISTER	VALUE	DESCRIPTION
DAC_CONFIG	0x00	DAC set for absolute voltage output.
OP_STAGE_CTRL	0x08	Output configured for 4-mA to 20-mA current output mode.
BRDG_CTRL	0x00	Bridge excitation set to 2.5 V.
P_GAIN_SELECT	0x00	P Gain set to 5 V/V.
T_GAIN_SELECT	0x00	T Gain set for 1.33 V/V.
TEMP_CTRL	0x40	I_{TEMP} drive disabled and T signal chain set for $V_{INT+} – V_{INT–}$.
TEMP_SE	0x00	T Gain set to single-ended configuration.
NORMAL_LOW_LSB	0x67	DAC normal low output set to 0x0667. Must be updated during calibration.
NORMAL_LOW_MSB	0x06	DAC normal low output set to 0x0667. Must be updated during calibration.
NORMAL_HIGH_LSB	0x9A	DAC normal high output set to 0x399A. Must be updated during calibration
NORMAL_HIGH_MSB	0x39	DAC normal high output set to 0x399A. Must be updated during calibration.
LOW_CLAMP_LSB	0x34	DAC clamp low output set to 0x0334. Must be updated during calibration.
LOW_CLAMP_MSB	0x03	DAC clamp low output set to 0x0334. Must be updated during calibration.
HIGH_CLAMP_LSB	0xCF	DAC clamp high output set to 0x3CCF. Must be updated during calibration.
HIGH_CLAMP_MSB	0x3C	DAC clamp high output set to 0x3CCF. Must be updated during calibration.
DIAG_ENABLE	0x00	Diagnostics disabled.
EEPROM_LOCK	0x00	EEPROM unlocked.
AFEDIAG_CFG	0x07	Diagnostics pulldown (1 MΩ) and pullup (1 MΩ) resistors enabled, INP_UV threshold = 10% and INP_OV threshold = 70%
AFEDIAG_MASK	0x33	INP_UV, INP_OV and PGAIN_UV, PGAIN_OV detection enabled.
SERIAL_NUMBER_BYTE0/1/2/3	0x00	Serial number specified by customer.
EEPROM_CRC_VALUE_USER	0xB8	Must be updated every time EEPROM is changed if diagnostics are enabled.

7.6.2 Control and Status Registers

Table 11. Control and Status Register Map

Register Name	Offset	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Control and Status Register Page 0										
MODE_CTRL	0x0C	R/W	RESERVED						MODE_SEL[1:0]	
Control and Status Register Page 2										
PADC_DATA_LSB	0x20	R	PADC_DATA[7:0]							
PADC_DATA_MSB	0x21	R	PADC_DATA[15:8]							
TADC_DATA_LSB	0x24	R	TADC_DATA[7:0]							
TADC_DATA_MSB	0x25	R	TADC_DATA[15:8]							
DAC_REG_LSB	0x30	R/W	DAC_REG[7:0]							
DAC_REG_MSB	0x31	R/W	RESERVED		DAC_REG[13:8]					
DAC_CONFIG(1)	0x39	R/W	RESERVED							DAC_ RATIOMETRIC
OP_STAGE_CTRL(1)	0x3B	R/W	RESERVED			DACCAP_EN	4_20MA_EN	DAC_GAIN[2:0]		
BRDG_CTRL(1)	0x46	R/W	RESERVED					VBRDG_ CTRL[1:0]		BRDG_EN
P_GAIN_ SELECT(1)	0x47	R/W	P_INV	RESERVED		P_GAIN[4:0]				
T_GAIN_ SELECT(1)	0x48	R/W	T_INV	RESERVED					T_GAIN[1:0]	
TEMP_CTRL(1)	0x4C	R/W	RESERVED	ITEMP_ CTRL[2:0]			TEMP_MUX_ CTRL[3:0]			
AFEDIAG	0x5A	R/W	TGAIN_UV	TGAIN_OV	PGAIN_UV	PGAIN_OV	RESERVED	INT_OV	INP_UV	INP_OV
TEST_CTRL	0x67	R/W	RESERVED				TEST_TEMP_ SE	RESERVED		TEST_DAC_ EN
Control and Status Register Page 5										
EEPROM ARRAY	0x00 - 0x7F	R								
EEPROM_CACHE	0x80 - 0x87	R/W								
EEPROM_PAGE_ ADDRESS	0x88	R/W	RESERVED				ADDR[3:0]			
EEPROM_CTRL	0x89	R/W	RESERVED				FIXED_ ERASE_ PROG_TIME	ERASE_AND _ PROGRAM	ERASE	PROGRAM
EEPROM_CRC	0x8A	R/W	RESERVED							CALCULATE _ CRC
EEPROM_STATUS	0x8B	R	RESERVED					PROGRAM_IN _ PROGRESS	ERASE_IN _ PROGRESS	READ_IN _ PROGRESS

(1) Register exists both in the control and status register map and the EEPROM register map. The settings of the control and status registers take effect when in configuration mode.

Table 11. Control and Status Register Map (continued)

Register Name	Offset	R/W	D7	D6	D5	D4	D3	D2	D1	D0
EEPROM_CRC _STATUS	0x8C	R	RESERVED						CRC_GOOD	CRC_CHECK _ IN_PROG
EEPROM_CRC_VALUE_ CALC	0x8D	R	EEPROM_ CRC_CALC[7:0]							

7.6.3 EEPROM Registers

Table 12. EEPROM Register Map

Register Name	Offset	R/W	D7	D6	D5	D4	D3	D2	D1	D0
EEPROM Page 0 (ADDR[3:0] = 0x0)										
H0_LSB	0x00	R/W	H0[7:0]							
H0_MSB	0x01	R/W	H0[15:8]							
G0_LSB	0x02	R/W	G0[7:0]							
G0_MSB	0x03	R/W	G0[15:8]							
N0_LSB	0x04	R/W	N0[7:0]							
N0_MSB	0x05	R/W	N0[15:8]							
H1_LSB	0x06	R/W	H1[7:0]							
H1_MSB	0x07	R/W	H1[15:8]							
EEPROM Page 1 (ADDR[3:0] = 0x1)										
G1_LSB	0x00	R/W	G1[7:0]							
G1_MSB	0x01	R/W	G1[15:8]							
N1_LSB	0x02	R/W	N1[7:0]							
N1_MSB	0x03	R/W	N1[15:8]							
H2_LSB	0x04	R/W	H2[7:0]							
H2_MSB	0x05	R/W	H2[15:8]							
G2_LSB	0x06	R/W	G2[7:0]							
G2_MSB	0x07	R/W	G2[15:8]							
EEPROM Page 2 (ADDR[3:0] = 0x2)										
N2_LSB	0x00	R/W	N2[7:0]							
N2_MSB	0x01	R/W	N2[15:8]							
A0_LSB	0x02	R/W	A0[7:0]							
A0_MSB	0x03	R/W	A0[15:8]							
A1_LSB	0x04	R/W	A1[7:0]							
A1_MSB	0x05	R/W	A1[15:8]							
A2_LSB	0x06	R/W	A2[7:0]							
A2_MSB	0x07	R/W	A2[15:8]							

Table 12. EEPROM Register Map (continued)

Register Name	Offset	R/W	D7	D6	D5	D4	D3	D2	D1	D0
EEPROM Page 3 (ADDR[3:0] = 0x3)										
B0_LSB	0x00	R/W	B0[7:0]							
B0_MSB	0x01	R/W	B0[15:8]							
B1_LSB	0x02	R/W	B1[7:0]							
B1_MSB	0x03	R/W	B1[15:8]							
B2_LSB	0x04	R/W	B2[7:0]							
B2_MSB	0x05	R/W	B2[15:8]							
RESERVED	0x06	R/W	RESERVED							
RESERVED	0x07	R/W	RESERVED							
EEPROM Page 4 (ADDR[3:0] = 0x4)										
DAC_CONFIG(1)	0x00	R/W	RESERVED							DAC_ RATIOMETRIC
OP_STAGE_CTRL(1)	0x01	R/W	RESERVED			DACCAP_EN	4_20MA_EN	DAC_GAIN[2:0]		
BRDG_CTRL(1)	0x02	R/W	RESERVED					VBRDG_ CTRL[1:0]		RESERVED
P_GAIN_ SELECT(1)	0x03	R/W	P_INV	RESERVED		P_GAIN[4:0]				
T_GAIN_ SELECT(1)	0x04	R/W	T_INV	RESERVED					T_GAIN[1:0]	
TEMP_CTRL(1)	0x05	R/W	RESERVED	ITEMP_ CTRL[2:0]			TEMP_MUX_ CTRL[3:0]			
RESERVED	0x06	R/W	RESERVED							
RESERVED	0x07	R/W	RESERVED							
EEPROM Page 5 (ADDR[3:0] = 0x5)										
TEMP_SE	0x00	R/W	RESERVED							TEMP_SE
RESERVED	0x01	R/W	RESERVED							
NORMAL_LOW_LSB	0x02	R/W	NORMAL_LOW[7:0]							
NORMAL_LOW_MSB	0x03	R/W	RESERVED		NORMAL_LOW[13:8]					
NORMAL_HIGH_LSB	0x04	R/W	NORMAL_HIGH[7:0]							
NORMAL_HIGH_MSB	0x05	R/W	RESERVED		NORMAL_HIGH[13:8]					
LOW_CLAMP_LSB	0x06	R/W	LOW_CLAMP[7:0]							
LOW_CLAMP_MSB	0x07	R/W	RESERVED		LOW_CLAMP[13:8]					

(1) Register exists both in the control and status register map and the EEPROM register map. The settings of the EEPROM registers take effect when in execution mode.

Table 12. EEPROM Register Map (continued)

Register Name	Offset	R/W	D7	D6	D5	D4	D3	D2	D1	D0
EEPROM Page 6 (ADDR[3:0] = 0x6)										
HIGH_CLAMP_LSB	0x00	R/W	HIGH_CLAMP[7:0]							
HIGH_CLAMP_MSB	0x01	R/W	RESERVED		HIGH_CLAMP[13:8]					
PADC_GAIN_LSB	0x02	R/W	PADC_GAIN[7:0]							
PADC_GAIN_MSB	0x03	R/W	PADC_GAIN[15:8]							
PADC_OFFSET_LSB	0x04	R/W	PADC_OFFSET[7:0]							
PADC_OFFSET_MSB	0x05	R/W	PADC_OFFSET[15:8]							
H3_LSB	0x06	R/W	H3[7:0]							
H3_MSB	0x07	R/W	H3[15:8]							
EEPROM Page 7 (ADDR[3:0] = 0x7)										
G3_LSB	0x00	R/W	G3[7:0]							
G3_MSB	0x01	R/W	G3[15:8]							
N3_LSB	0x02	R/W	N3[7:0]							
N3_MSB	0x03	R/W	N3[15:8]							
M0_LSB	0x04	R/W	M0[7:0]							
M0_MSB	0x05	R/W	M0[15:8]							
M1_MSB	0x06	R/W	M1[7:0]							
M1_LSB	0x07	R/W	M1[15:8]							
EEPROM Page 8 (ADDR[3:0] = 0x8)										
M2_LSB	0x00	R/W	M2[7:0]							
M2_MSB	0x01	R/W	M2[15:8]							
M3_LSB	0x02	R/W	M3[7:0]							
M3_MSB	0x03	R/W	M3[15:8]							
DIAG_ENABLE	0x04	R/W	RESERVED							DIAG_ ENABLE
EEPROM_LOCK	0x05	R/W	RESERVED							EEPROM_ LOCK
AFEDIAG_CFG	0x06	R/W	RESERVED	DIS_R_T	DIS_R_P	THRS[2:0]			PD[1:0]	
AFEDIAG_MASK	0x07	R/W	TGAIN_UV	TGAIN_OV	PGAIN_UV	PGAIN_OV	RESERVED	INT_OV	INP_UV	INP_OV

Table 12. EEPROM Register Map (continued)

Register Name	Offset	R/W	D7	D6	D5	D4	D3	D2	D1	D0
EEPROM Page 9 (ADDR[3:0] = 0x9)										
RESERVED	0x00	R/W	RESERVED							
RESERVED	0x01	R/W	RESERVED							
DAC_FAULT_LSB	0x02	R/W	DAC_FAULT[7:0]							
DAC_FAULT_MSB	0x03	R/W	RESERVED		DAC_FAULT[13:8]					
TADC_GAIN_LSB	0x04	R/W	TADC_GAIN[7:0]							
TADC_GAIN_MSB	0x05	R/W	TADC_GAIN[15:8]							
TADC_OFFSET_LSB	0x06	R/W	TADC_OFFSET[7:0]							
TADC_OFFSET_MSB	0x07	R/W	TADC_OFFSET[15:8]							
EEPROM Page 10 (ADDR[3:0] = 0xA)										
SERIAL_NUMBER_BYTE0	0x00	R/W	SERIAL_NUMBER_BYTE0[7:0]							
SERIAL_NUMBER_BYTE1	0x01	R/W	SERIAL_NUMBER_BYTE1[7:0]							
SERIAL_NUMBER_BYTE2	0x02	R/W	SERIAL_NUMBER_BYTE2[7:0]							
SERIAL_NUMBER_BYTE3	0x03	R/W	SERIAL_NUMBER_BYTE3[7:0]							
RESERVED	0x04	R/W	RESERVED							
RESERVED	0x05	R/W	RESERVED							
RESERVED	0x06	R/W	RESERVED							
RESERVED	0x07	R/W	RESERVED							
EEPROM Page 15 (ADDR[3:0] = 0xF)										
RESERVED	0x00	R/W	RESERVED							
RESERVED	0x01	R/W	RESERVED							
RESERVED	0x02	R/W	RESERVED							
RESERVED	0x03	R/W	RESERVED							
RESERVED	0x04	R/W	RESERVED							
RESERVED	0x05	R/W	RESERVED							
RESERVED	0x06	R/W	RESERVED							
EEPROM_CRC_VALUE_USER	0x07	R/W	EEPROM_ CRC_USER[7:0]							

Table 13 shows the factory programmed default values of the EEPROM. Do not change byte values marked in red font from their respective default values, otherwise the device does not operate as specified. Always write the default values as shown in Table 13 to the red marked bytes.

Table 13. EEPROM Default Values

EEPROM Page	BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
0x0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x1	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x2	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x3	0x00	0x00	0x00	0x00	0x00	0x00	0xFF	0xFF
0x4	0x00	0x08	0x00	0x00	0x00	0x40	0xFF	0x01
0x5	0x00	0xFF	0x67	0x06	0x9A	0x39	0x34	0x03
0x6	0xCF	0x3C	0x01	0x00	0x00	0x00	0x00	0x00
0x7	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x8	0x00	0x00	0x00	0x00	0x00	0x00	0x07	0x33
0x9	0xFF	0xFF	0xDD	0xCC	0x01	0x00	0x00	0x00
0xA	0x00	0x00	0x00	0x00	0xFF	0xFF	0xFF	0xFF
0xB	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
0xC	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
0xD	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
0xE	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
0xF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xB8

7.6.4 Register Descriptions

7.6.4.1 MODE_CTRL Register (CS Register Page: 0x0) (CS Offset: 0x0C) (EEPROM Page: N/A) (EEPROM Offset: N/A)

Figure 23. MODE_CTRL Register

7	6	5	4	3	2	1	0
RESERVED						MODE_SEL[1:0]	
R/W-0b000000						R/W-0b00	

Table 14. MODE_CTRL Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R/W	0b000000	Reserved Always write 0b000000.
1:0	MODE_SEL[1:0]	R/W	0b00	0b00: Execution mode 0b01: Do not use 0b10: Do not use 0b11: Configuration mode. Used to read and write the control and status and EEPROM registers through the OWI.

7.6.4.2 PADC_DATA_LSB and PADC_DATA_MSB Registers (CS Register Page: 0x2) (CS Offset: 0x20, 0x21) (EEPROM Page: N/A) (EEPROM Offset: N/A)

The PADC_DATA_LSB and PADC_DATA_MSB registers together make up the P ADC conversion result (PADC_DATA[15:0]) which can be read in configuration mode. The PADC_DATA[15:0] data is provided in binary two's-complement format.

Figure 24. PADC_DATA_LSB Register

7	6	5	4	3	2	1	0
PADC_DATA[7:0]							
R-0bxxxxxxxx							

Figure 25. PADC_DATA_MSB Register

7	6	5	4	3	2	1	0
PADC_DATA[15:8]							
R-0bxxxxxxxx							

7.6.4.3 TADC_DATA_LSB and TADC_DATA_MSB Registers (CS Register Page: 0x2) (CS Offset: 0x24, 0x25) (EEPROM Page: N/A) (EEPROM Offset: N/A)

The TADC_DATA_LSB and TADC_DATA_MSB registers together make up the T ADC conversion result (TADC_DATA[15:0]) which can be read in configuration mode. The TADC_DATA[15:0] data is provided in binary two's-complement format.

Figure 26. TADC_DATA_LSB Register

7	6	5	4	3	2	1	0
TADC_DATA[7:0]							
R-0bxxxxxxxx							

Figure 27. TADC_DATA_MSB Register

7	6	5	4	3	2	1	0
TADC_DATA[15:8]							
R-0bxxxxxxxx							

7.6.4.4 DAC_REG_LSB and DAC_REG_MSB Registers (CS Register Page: 0x2) (CS Offset: 0x30, 0x31) (EEPROM Page: N/A) (EEPROM Offset: N/A)

The DAC_REG_LSB and DAC_REG_MSB registers together make up the DAC output code (DAC_REG[13:0]) which can be read and written in configuration mode. The DAC_REG[13:0] data is provided in unipolar straight binary format.

Figure 28. DAC_REG_LSB Register

7	6	5	4	3	2	1	0
DAC_REG[7:0]							
R/W-0bxxxxxxxx							

Figure 29. DAC_REG_MSB Register

7	6	5	4	3	2	1	0
RESERVED		DAC_REG[13:8]					
R/W-0b00		R/W-0bxxxxxx					

7.6.4.5 TC and NL Compensation Coefficient (h_x, g_x, n_x, and m_x) Registers (CS Register Page: N/A) (CS Offset: N/A) (EEPROM Page: see Table 12) (EEPROM Offset: see Table 12)

The H0_LSB and H0_MSB registers together make up the h_0 TC and NL compensation coefficient (H0[15:0]). The H0[15:0] data is provided in binary two's-complement format. All other TC and NL compensation coefficients (h_x, g_x, n_x, and m_x) follow the same format.

Figure 30. H0_LSB Register

7	6	5	4	3	2	1	0
H0[7:0]							
R/W-0b00000000							

Figure 31. H0_MSB Register

7	6	5	4	3	2	1	0
H0[15:8]							
R/W-0b00000000							

7.6.4.6 Digital Filter Coefficient (a_x and b_x) Registers (CS Register Page: N/A) (CS Offset: N/A) (EEPROM Page: see Table 12) (EEPROM Offset: see Table 12)

The A0_LSB and A0_MSB registers together make up the a_0 digital filter coefficient (A0[15:0]). The A0[15:0] data is provided in binary two's-complement format. All other digital filter coefficients (a_x and b_x) follow the same format. Please see the *Filter Coefficients* section for digital filter coefficient settings.

Figure 32. A0_LSB Register

7	6	5	4	3	2	1	0
A0[7:0]							
R/W-0b00000000							

Figure 33. A0_MSB Register

7	6	5	4	3	2	1	0
A0[15:8]							
R/W-0b00000000							

7.6.4.7 NORMAL_LOW_LSB and NORMAL_LOW_MSB Registers (CS Register Page: N/A) (CS Offset: N/A) (EEPROM Page: 0x5) (EEPROM Offset: 0x02, 0x03)

The NORMAL_LOW_LSB and NORMAL_LOW_MSB registers together make up the NORMAL_LOW[13:0] DAC output threshold. Any DAC output below the NORMAL_LOW[13:0] threshold is driven to the LOW_CLAMP[13:0] DAC output code. The NORMAL_LOW[13:0] data is provided in unipolar straight binary format.

Figure 34. NORMAL_LOW_LSB Register

7	6	5	4	3	2	1	0
NORMAL_LOW[7:0]							
R/W-0b01100111							

Figure 35. NORMAL_LOW_MSB Register

7	6	5	4	3	2	1	0
RESERVED		NORMAL_LOW[13:8]					
R/W-0b00		R/W-0b000110					

7.6.4.8 NORMAL_HIGH_LSB and NORMAL_HIGH_MSB Registers (CS Register Page: N/A) (CS Offset: N/A) (EEPROM Page: 0x5) (EEPROM Offset: 0x04, 0x05)

The NORMAL_HIGH_LSB and NORMAL_HIGH_MSB registers together make up the NORMAL_HIGH[13:0] DAC output threshold. Any DAC output above the NORMAL_HIGH[13:0] threshold is driven to the HIGH_CLAMP[13:0] DAC output code. The NORMAL_HIGH[13:0] data is provided in unipolar straight binary format.

Figure 36. NORMAL_HIGH_LSB Register

7	6	5	4	3	2	1	0
NORMAL_HIGH[7:0]							
R/W-0b10011010							

Figure 37. NORMAL_HIGH_MSB Register

7	6	5	4	3	2	1	0
RESERVED		NORMAL_HIGH[13:8]					
R/W-0b00		R/W-0b111001					

7.6.4.9 LOW_CLAMP_LSB and LOW_CLAMP_MSB Registers (CS Register Page: N/A) (CS Offset: N/A) (EEPROM Page: 0x5) (EEPROM Offset: 0x06, 0x07)

The LOW_CLAMP_LSB and LOW_CLAMP_MSB registers together make up the LOW_CLAMP[13:0] DAC output value. Any DAC output below the NORMAL_LOW[13:0] threshold is driven to the LOW_CLAMP[13:0] DAC output code. The LOW_CLAMP[13:0] data is provided in unipolar straight binary format.

Figure 38. LOW_CLAMP_LSB Register

7	6	5	4	3	2	1	0
LOW_CLAMP[7:0]							
R/W-0b00110100							

Figure 39. LOW_CLAMP_MSB Register

7	6	5	4	3	2	1	0
RESERVED		LOW_CLAMP[13:8]					
R/W-0b00		R/W-0b000011					

7.6.4.10 HIGH_CLAMP_LSB and HIGH_CLAMP_MSB Registers (CS Register Page: N/A) (CS Offset: N/A) (EEPROM Page: 0x6) (EEPROM Offset: 0x00, 0x01)

The HIGH_CLAMP_LSB and HIGH_CLAMP_MSB registers together make up the HIGH_CLAMP[13:0] DAC output value. Any DAC output above the NORMAL_HIGH[13:0] threshold is driven to the HIGH_CLAMP[13:0] DAC output code. The HIGH_CLAMP[13:0] data is provided in unipolar straight binary format.

Figure 40. HIGH_CLAMP_LSB Register

7	6	5	4	3	2	1	0
HIGH_CLAMP[7:0]							
R/W-0b11001111							

Figure 41. HIGH_CLAMP_MSB Register

7	6	5	4	3	2	1	0
RESERVED		HIGH_CLAMP[13:8]					
R/W-0b00		R/W-0b111100					

7.6.4.11 PADC_GAIN_LSB and PADC_GAIN_MSB Registers (CS Register Page: N/A) (CS Offset: N/A) (EEPROM Page: 0x6) (EEPROM Offset: 0x02, 0x03)

The PADC_GAIN_LSB and PADC_GAIN_MSB registers together make up the P ADC digital gain coefficient (PADC_GAIN[15:0]). The PADC_GAIN[15:0] data is provided in binary two's-complement format. No fractional gain coefficients are possible. Means a value of 0x0001 represents a gain coefficient of 1x, while a value of 0x0010 represents a gain coefficient of 2x.

Figure 42. PADC_GAIN_LSB Register

7	6	5	4	3	2	1	0
PADC_GAIN[7:0]							
R/W-0b00000001							

Figure 43. PADC_GAIN_MSB Register

7	6	5	4	3	2	1	0
PADC_GAIN[15:8]							
R/W-0b00000000							

7.6.4.12 PADC_OFFSET_LSB and PADC_OFFSET_MSB Registers (CS Register Page: N/A) (CS Offset: N/A) (EEPROM Page: 0x6) (EEPROM Offset: 0x04, 0x05)

The PADC_OFFSET_LSB and PADC_OFFSET_MSB registers together make up the P ADC digital offset coefficient (PADC_OFFSET[15:0]). The PADC_OFFSET[15:0] data is provided in binary two's-complement format.

Figure 44. PADC_OFFSET_LSB Register

7	6	5	4	3	2	1	0
PADC_OFFSET[7:0]							
R/W-0b00000000							

Figure 45. PADC_OFFSET_MSB Register

7	6	5	4	3	2	1	0
PADC_OFFSET[15:8]							
R/W-0b00000000							

7.6.4.13 DAC_FAULT_LSB and DAC_FAULT_MSB Registers (CS Register Page: N/A) (CS Offset: N/A) (EEPROM Page: 0x9) (EEPROM Offset: 0x02, 0x03)

The DAC_FAULT_LSB and DAC_FAULT_MSB registers together make up the DAC_FAULT[13:0] DAC output value. When the diagnostics are enabled, the DAC ouput is driven to the DAC_FAULT[13:0] value in case a power-supply or signal-chain error occurs. The DAC_FAULT[13:0] data is provided in unipolar straight binary format.

The power-supply or signal-chain error indication takes priority over the clamping condition. That means if the DAC output is clamped to either the LOW_CLAMP[13:0] or HIGH_CLAMP[13:0] value and a power-supply or signal-chain error occurs, then the DAC output is driven to the DAC_FAULT[13:0] value.

Figure 46. DAC_FAULT_LSB Register

7	6	5	4	3	2	1	0
DAC_FAULT[7:0]							
R/W-0b11011101							

Figure 47. DAC_FAULT_MSB Register

7	6	5	4	3	2	1	0
RESERVED		DAC_FAULT[13:8]					
R/W-0b11		R/W-0b001100					

7.6.4.14 TADC_GAIN_LSB and TADC_GAIN_MSB Registers (CS Register Page: N/A) (CS Offset: N/A) (EEPROM Page: 0x9) (EEPROM Offset: 0x04, 0x05)

The TADC_GAIN_LSB and TADC_GAIN_MSB registers together make up the T ADC digital gain coefficient (TADC_GAIN[15:0]). The TADC_GAIN[15:0] data is provided in binary two's-complement format. No fractional gain coefficients are possible. Means a value of 0x0001 represents a gain coefficient of 1x, while a value of 0x0010 represents a gain coefficient of 2x.

Figure 48. TADC_GAIN_LSB Register

7	6	5	4	3	2	1	0
TADC_GAIN[7:0]							
R/W-0b00000001							

Figure 49. TADC_GAIN_MSB Register

7	6	5	4	3	2	1	0
TADC_GAIN[15:8]							
R/W-0b00000000							

7.6.4.15 TADC_OFFSET_LSB and TADC_OFFSET_MSB Registers (CS Register Page: N/A) (CS Offset: N/A) (EEPROM Page: 0x9) (EEPROM Offset: 0x06, 0x07)

The TADC_OFFSET_LSB and TADC_OFFSET_MSB registers together make up the T ADC digital offset coefficient (TADC_OFFSET[15:0]). The TADC_OFFSET[15:0] data is provided in binary two's-complement format.

Figure 50. TADC_OFFSET_LSB Register

7	6	5	4	3	2	1	0
TADC_OFFSET[7:0]							
R/W-0b00000000							

Figure 51. TADC_OFFSET_MSB Register

7	6	5	4	3	2	1	0
TADC_OFFSET[15:8]							
R/W-0b00000000							

7.6.4.16 SERIAL_NUMBER_BYTE0/1/2/3 Registers (CS Register Page: N/A) (CS Offset: N/A) (EEPROM Page: 0xA) (EEPROM Offset: 0x00, 0x01, 0x02, 0x03)

The SERIAL_NUMBER_BYTEx registers are used to program a user-defined serial number into the device.

Figure 52. SERIAL_NUMBER_BYTEx Register

7	6	5	4	3	2	1	0
SERIAL_NUMBER_BYTEx[7:0]							
R/W-0b00000000							

7.6.4.17 DAC_CONFIG Register (CS Register Page: 0x2) (CS Offset: 0x39) (EEPROM Page: 0x4) (EEPROM Offset: 0x00)

Figure 53. DAC_CONFIG Register

7	6	5	4	3	2	1	0
RESERVED							DAC_ RATIOMETRIC
R/W-0b0000000							R/W-0b0

Table 15. DAC_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R/W	0b0000000	Reserved Always write 0b0000000.
0	DAC_RATIOMETRIC	R/W	0b0	Set to 0b0 when in current output mode. 0b0: DAC is in absolute output mode 0b1: DAC is in ratiometric output mode

7.6.4.18 OP_STAGE_CTRL Register (CS Register Page: 0x2) (CS Offset: 0x3B) (EEPROM Page: 0x4) (EEPROM Offset: 0x01)

Figure 54. OP_STAGE_CTRL Register

7	6	5	4	3	2	1	0
RESERVED			DACCAP_EN	4_20MA_EN	DAC_GAIN[2:0]		
R/W-0b000			R/W-0b0	R/W-0b1	R/W-0b000		

Table 16. OP_STAGE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0b000	Reserved Always write 0b000.
4	DACCAP_EN	R/W	0b0	0b0: DACCAP capacitor disabled 0b1: DACCAP capacitor enabled
3	4_20MA_EN	R/W	0b1	Set to 0b0 when in voltage output mode. 0b0: 4-mA to 20-mA current output disabled 0b1: 4-mA to 20-mA current output enabled
2:0	DAC_GAIN[2:0]	R/W	0b000	Set to 0b000 when in current output mode. 0b000: Voltage mode disabled 0b001: Gain = 10 V/V 0b010: Gain = 4 V/V 0b011: Reserved 0b100: Gain = 2 V/V 0b101: Reserved 0b110: Gain = 6.67 V/V 0b111: Reserved

7.6.4.19 TEST_CTRL Register (CS Register Page: 0x02) (CS Offset: 0x67) (EEPROM Page: N/A) (EEPROM Offset: N/A)

Figure 55. TEST_CTRL Register

7	6	5	4	3	2	1	0
RESERVED				TEST_TEMP_SE	RESERVED		TEST_DAC_EN
R/W-0b0000				R/W-0b0	R/W-0b00		R/W-0b0

Table 17. TEST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b0000	Reserved Always write 0b0000.
3	TEST_TEMP_SE	R/W	0b0	0b0: T Gain amplifier configured for single-ended operation in configuration mode 0b1: T Gain amplifier configured for differential operation in configuration mode
2:1	RESERVED	R/W	0b00	Reserved Always write 0b00.
0	TEST_DAC_EN	R/W	0b0	0b0: DAC output disabled in configuration mode 0b1: DAC output enabled and connected to DAC gain stage in configuration mode

7.6.4.20 BRDG_CTRL Register (CS Register Page: 0x2) (CS Offset: 0x46) (EEPROM Page: 0x4) (EEPROM Offset: 0x02)

Figure 56. BRDG_CTRL Register

7	6	5	4	3	2	1	0
RESERVED					VBRDG_ CTRL[1:0]		BRDG_EN
R/W-0b00000					R/W-0b00		R/W-0b0

Table 18. BRDG_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R/W	0b00000	Reserved Always write 0b00000.
2:1	VBRDG_CTRL[1:0]	R/W	0b00	0b00: Bridge supply voltage = 2.5 V 0b01: Bridge supply voltage = 2.0 V 0b10: Bridge supply voltage = 1.25 V 0b11: Bridge supply voltage = 1.25 V
0	BRDG_EN	R/W	0b0	BRDG_EN configurable only in configuration mode. BRDG_EN is always enabled in execution mode irrespective of the BRDG_EN setting. 0b0: Bridge voltage disabled in configuration mode 0b1: Bridge voltage enabled in configuration mode

7.6.4.21 P_GAIN_SELECT Register (CS Register Page: 0x2) (CS Offset: 0x47) (EEPROM Page: 0x4) (EEPROM Offset: 0x03)

Figure 57. P_GAIN_SELECT Register

7	6	5	4	3	2	1	0
P_INV	RESERVED		P_GAIN[4:0]				
R/W-0b0	R/W-0b00		R/W-0b00000				

Table 19. P_GAIN_SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	P_INV	R/W	0b0	0b0: No inversion 0b1: Inverts the output of the P Gain output
6:5	RESERVED	R/W	0b00	Reserved Always write 0b00.
4:0	P_GAIN[4:0]	R/W	0b00000	0b00000: P Gain = 5 V/V 0b00001: P Gain = 5.48 V/V 0b00010: P Gain = 5.97 V/V 0b00011: P Gain = 6.56 V/V 0b00100: P Gain = 7.02 V/V 0b00101: P Gain = 8 V/V 0b00110: P Gain = 9.09 V/V 0b00111: P Gain = 10 V/V 0b01000: P Gain = 10.53 V/V 0b01001: P Gain = 11.11 V/V 0b01010: P Gain = 12.5 V/V 0b01011: P Gain = 13.33 V/V 0b01100: P Gain = 14.29 V/V 0b01101: P Gain = 16 V/V 0b01110: P Gain = 17.39 V/V 0b01111: P Gain = 18.18 V/V 0b10000: P Gain = 19.05 V/V 0b10001: P Gain = 20 V/V 0b10010: P Gain = 22.22 V/V 0b10011: P Gain = 25 V/V 0b10100: P Gain = 30.77 V/V 0b10101: P Gain = 36.36 V/V 0b10110: P Gain = 40 V/V 0b10111: P Gain = 44.44 V/V 0b11000: P Gain = 50 V/V 0b11001: P Gain = 57.14 V/V 0b11010: P Gain = 66.67 V/V 0b11011: P Gain = 80 V/V 0b11100: P Gain = 100 V/V 0b11101: P Gain = 133.33 V/V 0b11110: P Gain = 200 V/V 0b11111: P Gain = 400 V/V

7.6.4.22 T_GAIN_SELECT Register (CS Register Page: 0x2) (CS Offset: 0x48) (EEPROM Page: 0x4) (EEPROM Offset: 0x04)

Figure 58. T_GAIN_SELECT Register

7	6	5	4	3	2	1	0
T_INV	RESERVED					T_GAIN[1:0]	
R/W-0b0	R/W-0b00000					R/W-0b00	

Table 20. T_GAIN_SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	T_INV	R/W	0b0	0b0: No inversion 0b1: Inverts the output of the T Gain output
6:2	RESERVED	R/W	0b00000	Reserved Always write 0b00000.
1:0	T_GAIN[1:0]	R/W	0b00	0b00: T Gain = 1.33 V/V 0b01: T Gain = 2 V/V 0b10: T Gain = 5 V/V 0b11: T Gain = 20 V/V

7.6.4.23 TEMP_CTRL Register (CS Register Page: 0x2) (CS Offset: 0x4C) (EEPROM Page: 0x4) (EEPROM Offset: 0x05)

Figure 59. TEMP_CTRL Register

7	6	5	4	3	2	1	0
RESERVED	ITEMP_ CTRL[2:0]			TEMP_MUX_ CTRL[3:0]			
R/W-0b0	R/W-0b100			R/W-0b0000			

Table 21. TEMP_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b0	Reserved Always write 0b0.
6:4	ITEMP_ CTRL[2:0]	R/W	0b100	0b000: 25 µA 0b001: 50 µA 0b010: 100 µA 0b011: 500 µA 0b1xx: Off
3:0	TEMP_MUX_ CTRL[3:0]	R/W	0b0000	0b0000: INT+ and INT– 0b0011: VTEMP_INT-GND (Internal Temperature Sensor)

7.6.4.24 TEMP_SE Register (CS Register Page: N/A) (CS Offset: N/A) (EEPROM Page: 0x5) (EEPROM Offset: 0x00)

Figure 60. TEMP_SE Register

7	6	5	4	3	2	1	0
RESERVED							TEMP_SE
R/W-0b0000000							R/W-0b0

Table 22. TEMP_SE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R/W	0b0000000	Reserved Always write 0b0000000.
0	TEMP_SE	R/W	0b0	0b0: T Gain amplifier configured for single-ended operation 0b1: T Gain amplifier configured for differential operation

7.6.4.25 DIAG_ENABLE Register (CS Register Page: N/A) (CS Offset: N/A) (EEPROM Page: 0x8) (EEPROM Offset: 0x04)

Figure 61. DIAG_ENABLE Register

7	6	5	4	3	2	1	0
RESERVED							DIAG_ENABLE
R/W-0b0000000							R/W-0b0

Table 23. DIAG_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R/W	0b0000000	Reserved Always write 0b0000000.
0	DIAG_ENABLE	R/W	0b0	0b0: Diagnostics disabled 0b1: Diagnostics enabled

7.6.4.26 AFEDIAG_MASK Register (CS Register Page: N/A) (CS Offset: N/A) (EEPROM Page: 0x8) (EEPROM Offset: 0x07)

Figure 62. AFEDIAG_MASK Register

7	6	5	4	3	2	1	0
TGAIN_UV	TGAIN_OV	PGAIN_UV	PGAIN_OV	RESERVED	INT_OV	INP_UV	INP_OV
R/W-0b0	R/W-0b0	R/W-0b1	R/W-0b1	R/W-0b0	R/W-0b0	R/W-0b1	R/W-0b1

Table 24. AFEDIAG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TGAIN_UV	R/W	0b0	0b0: Undervoltage detection at output pins of T Gain disabled 0b1: Undervoltage detection at output pins of T Gain enabled
6	TGAIN_OV	R/W	0b0	0b0: Overvoltage detection at output pins of T Gain disabled 0b1: Overvoltage detection at output pins of T Gain enabled
5	PGAIN_UV	R/W	0b1	0b0: Undervoltage detection at output pins of P Gain disabled 0b1: Undervoltage detection at output pins of P Gain enabled
4	PGAIN_OV	R/W	0b1	0b0: Overvoltage detection at output pins of P Gain disabled 0b1: Overvoltage detection at output pins of P Gain enabled
3	RESERVED	R/W	0b0	Reserved Always write 0b0.
2	INT_OV	R/W	0b0	0b0: Overvoltage detection at input pins of T Gain disabled 0b1: Overvoltage detection at input pins of T Gain enabled
1	INP_UV	R/W	0b1	0b0: Undervoltage detection at input pins of P Gain disabled 0b1: Undervoltage detection at input pins of P Gain enabled
0	INP_OV	R/W	0b1	0b0: Overvoltage detection at input pins of P Gain disabled 0b1: Overvoltage detection at input pins of P Gain enabled

7.6.4.27 AFEDIAG_CFG Register (CS Register Page: N/A) (CS Offset: N/A) (EEPROM Page: 0x8) (EEPROM Offset: 0x06)

Figure 63. AFEDIAG_CFG Register

7	6	5	4	3	2	1	0
RESERVED	DIS_R_T	DIS_R_P	THRS[2:0]			PD[1:0]	
R/W-0b0	R/W-0b0	R/W-0b0	R/W-0b001			R/W-0b11	

Table 25. AFEDIAG_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b0	Reserved Always write 0b0
6	DIS_R_T	R/W	0b0	0b0: Pullup resistors used for open/short diagnostics on INT+ and INT– pins enabled 0b1: Pullup resistors used for open/short diagnostics on INT+ and INT– pins disabled
5	DIS_R_P	R/W	0b0	0b0: Pulldown resistors used for open/short diagnostics on the INP+ and INP– pins enabled 0b1: Pulldown resistors used for open/short diagnostics on the INP+ and INP– pins disabled
4:2	THRS[2:0]	R/W	0b001	V_{BRG} = 2.5 V: 0b000: INP_UV Threshold = 7.5% of programmed V_{BRG}, INP_OV Threshold = 72.5% of programmed V_{BRG} 0b001: INP_UV Threshold = 10% of programmed V_{BRG}, INP_OV Threshold = 70% of programmed V_{BRG} 0b010: INP_UV Threshold = 15% of programmed V_{BRG}, INP_OV Threshold = 65% of programmed V_{BRG} V_{BRG} = 2 V: 0b011: INP_UV Threshold = 10% of programmed V_{BRG}, INP_OV Threshold = 90% of programmed V_{BRG} 0b100: INP_UV Threshold = 12.5% of programmed V_{BRG}, INP_OV Threshold = 87.5% of programmed V_{BRG} 0b101: INP_UV Threshold = 17.5% of programmed V_{BRG}, INP_OV Threshold = 82.5% of programmed V_{BRG} V_{BRG} = 1.25 V: 0b110: INP_UV Threshold = 17.5% of programmed V_{BRG}, INP_OV Threshold = 100% of programmed V_{BRG} 0b111: INP_UV Threshold = 22.5% of programmed V_{BRG}, INP_OV Threshold = 95% of programmed V_{BRG}
1:0	PD[1:0]	R/W	0b11	0b00: Pulldown resistor value = 4 MΩ 0b01: Pulldown resistor value = 2 MΩ 0b10: Pulldown resistor value = 3 MΩ 0b11: Pulldown resistor value = 1 MΩ

7.6.4.28 AFEDIAG
(CS Register Page: 0x2) (CS Offset: 0x5A) (EEPROM Page: N/A) (EEPROM Offset: N/A)

Figure 64. AFEDIAG Register

7	6	5	4	3	2	1	0
TGAIN_UV	TGAIN_OV	PGAIN_UV	PGAIN_OV	RESERVED	INT_OV	INP_UV	INP_OV
R/W-0b0	R/W-0b0	R/W-0b0	R/W-0b0	R-0b0	R/W-0b0	R/W-0b0	R/W-0b0

Table 26. AFEDIAG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TGAIN_UV	R/W	0b0	Write 0b1 to clear bit. Writing 0b0 has no effect. TGAIN_UV flag is always set if T Gain is configured for single-ended mode because one of the terminals is always at ground potential. 0b0: Indicates no undervoltage at output pins of T Gain 0b1: Indicates undervoltage at output pins of T Gain
6	TGAIN_OV	R/W	0b0	Write 0b1 to clear bit. Writing 0b0 has no effect. 0b0: Indicates no overvoltage at output pins of T Gain 0b1: Indicates overvoltage at output pins of T Gain
5	PGAIN_UV	R/W	0b0	Write 0b1 to clear bit. Writing 0b0 has no effect. 0b0: Indicates no undervoltage at output pins of P Gain 0b1: Indicates undervoltage at output pins of P Gain
4	PGAIN_OV	R/W	0b0	Write 0b1 to clear bit. Writing 0b0 has no effect. 0b0: Indicates no overvoltage at output pins of P Gain 0b1: Indicates overvoltage at output pins of P Gain
3	RESERVED	R/W	0b0	Reserved Always write 0b0.
2	INT_OV	R/W	0b0	Write 0b1 to clear bit. Writing 0b0 has no effect. 0b0: Indicates no overvoltage at input pins of T Gain 0b1: Indicates overvoltage at input pins of T Gain
1	INP_UV	R/W	0b0	Write 0b1 to clear bit. Writing 0b0 has no effect. 0b0: Indicates no undervoltage at input pins of P Gain 0b1: Indicates undervoltage at input pins of P Gain
0	INP_OV	R/W	0b0	Write 0b1 to clear bit. Writing 0b0 has no effect. 0b0: Indicates no overvoltage at input pins of P Gain 0b1: Indicates overvoltage at input pins of P Gain

7.6.4.29 EEPROM_LOCK Register (CS Register Page: N/A) (CS Offset: N/A) (EEPROM Page: 0x8) (EEPROM Offset: 0x05)

Figure 65. EEPROM_LOCK Register

7	6	5	4	3	2	1	0
RESERVED							EEPROM_LOCK
R/W-0b0000000							R/W-0b0

Table 27. EEPROM_LOCK Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R/W	0b0000000	Reserved Always write 0b0000000.
0	EEPROM_LOCK	R/W	0b0	0b0: EEPROM is unlocked - EEPROM is accessible 0b1: EEPROM is locked - EEPROM is not accessible

7.6.4.30 EEPROM_PAGE_ADDRESS Register (CS Register Page: 0x5) (CS Offset: 0x88) (EEPROM Page: N/A) (EEPROM Offset: N/A)

Figure 66. EEPROM_PAGE_ADDRESS Register

7	6	5	4	3	2	1	0
RESERVED				ADDR[3:0]			
R/W-0b0000				R/W-0b0000			

Table 28. EEPROM_PAGE_ADDRESS Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b0000	Reserved Always write 0b0000.
3:0	ADDR[3:0]	R/W	0b0000	EEPROM page address used in the EEPROM programming procedure

7.6.4.31 EEPROM_CTRL Register (CS Register Page: 0x5) (CS Offset: 0x89) (EEPROM Page: N/A) (EEPROM Offset: N/A)

Figure 67. EEPROM_CTRL Register

7	6	5	4	3	2	1	0
RESERVED				FIXED_ ERASE_ PROG_TIME	ERASE_AND _PROGRAM	ERASE	PROGRAM
R/W-0b0000				R/W-0b0	R/W-0b0	R/W-0b0	R/W-0b0

Table 29. EEPROM_CTRL Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0b0000	Reserved Always write 0b0000.
3	FIXED_ERASE_PROG_TIME	R/W	0b0	0b0: Use variable time <8 ms as the Erase/Program time. The EEPROM programming logic will determine the duration to program the EEPROM memory. 0b1: Use fixed 8 ms as the Erase/Program time
2	ERASE_AND_PROGRAM	R/W	0b0	0b0: No action 0b1: Erase contents of EEPROM memory pointed to by EEPROM_PAGE_ADDRESS and program contents of EEPROM cache
1	ERASE	R/W	0b0	0b0: No action 0b1: Erase contents of EEPROM memory pointed to by EEPROM_PAGE_ADDRESS
0	PROGRAM	R/W	0b0	0b0: No action 0b1: Program contents of EEPROM cache into EEPROM memory pointed to by EEPROM_PAGE_ADDRESS

7.6.4.32 EEPROM_STATUS Register (CS Register Page: 0x5) (CS Offset: 0x8B) (EEPROM Page: N/A) (EEPROM Offset: N/A)

Figure 68. EEPROM_STATUS Register

7	6	5	4	3	2	1	0
RESERVED					PROGRAM_IN _PROGRESS	ERASE_IN _PROGRESS	READ_IN _PROGRESS
R-0b00000					R-0b0	R-0b0	R-0b0

Table 30. EEPROM_STATUS Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0b00000	Reserved Always write 0b00000.
2	PROGRAM_IN_PROGRESS	R	0b0	0b0: EEPROM Program not in progress 0b1: EEPROM Program in progress
1	ERASE_IN_PROGRESS	R	0b0	0b0: EEPROM Erase not in progress 0b1: EEPROM Erase in progress
0	READ_IN_PROGRESS	R	0b0	0b0: EEPROM Read not in progress 0b1: EEPROM Read in progress

7.6.4.33 EEPROM_CRC Register (CS Register Page: 0x5) (CS Offset: 0x8A) (EEPROM Page: N/A) (EEPROM Offset: N/A)

Figure 69. EEPROM_CRC Register

7	6	5	4	3	2	1	0
RESERVED							CALCULATE_CRC
R/W-0b0000000							R/W-0b0

Table 31. EEPROM_CRC Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R/W	0b0000000	Reserved Always write 0b0000000.
0	CALCULATE_CRC	R/W	0b0	0b0: No action 0b1: Calculate EEPROM CRC

7.6.4.34 EEPROM_CRC_STATUS Register (CS Register Page: 0x5) (CS Offset: 0x8C) (EEPROM Page: N/A) (EEPROM Offset: N/A)

Figure 70. EEPROM_CRC_STATUS Register

7	6	5	4	3	2	1	0
RESERVED						CRC_GOOD	CRC_CHECK_IN_PROG
R-0b000000						R-0b0	R-0b0

Table 32. EEPROM_CRC_STATUS Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0b000000	Reserved Always write 0b000000.
1	CRC_GOOD	R	0b0	0b0: Programmed EEPROM_CRC_VALUE_USER does not match calculated EEPROM_CRC_VALUE_CALC 0b1: Programmed EEPROM_CRC_VALUE_USER matches calculated EEPROM_CRC_VALUE_CALC
0	CRC_CHECK_IN_PROG	R	0b0	0b0: EEPROM CRC check not in progress 0b1: EEPROM CRC check in progress

7.6.4.35 EEPROM_CRC_VALUE_CALC Register (CS Register Page: 0x5) (CS Offset: 0x8D) (EEPROM Page: N/A) (EEPROM Offset: N/A)

Figure 71. EEPROM_CRC_VALUE_CALC Register

7	6	5	4	3	2	1	0
EEPROM_CRC_CALC[7:0]							
R-0bxxxxxxxx							

Table 33. EEPROM_CRC_VALUE_CALC Field Descriptions

Bit	Field	Type	Reset	Description
7:0	EEPROM_CRC_CALC[7:0]	R	0bxxxxxxxx	CRC value as calculated by the digital logic.

7.6.4.36 EEPROM_CRC_VALUE_USER Register (CS Register Page: N/A) (CS Offset: N/A) (EEPROM Page: 0xF) (EEPROM Offset: 0x07)

Figure 72. EEPROM_CRC_VALUE_USER Register

7	6	5	4	3	2	1	0
EEPROM_CRC_USER[7:0]							
R/W-0b10111000							

Table 34. EEPROM_CRC_VALUE_USER Field Descriptions

Bit	Field	Type	Reset	Description
7:0	EEPROM_CRC_USER[7:0]	R/W	0b10111000	CRC value written by the user.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The PGA300 can be used in a variety of applications to measure pressure and temperature. Depending on the application, the device can be configured in different output modes as illustrated in the *Typical Applications* section.

8.1.1 Harness Open-Wire Diagnostics

The device allows for open-wire diagnostics to be performed by the controller that interfaces with the PGA300. Specifically, the controller can detect an open PWR or open GND wire by installing a pullup or pulldown resistor on the OUT line.

Figure 73 shows the possible harness open-wire faults on the PWR and GND pins.

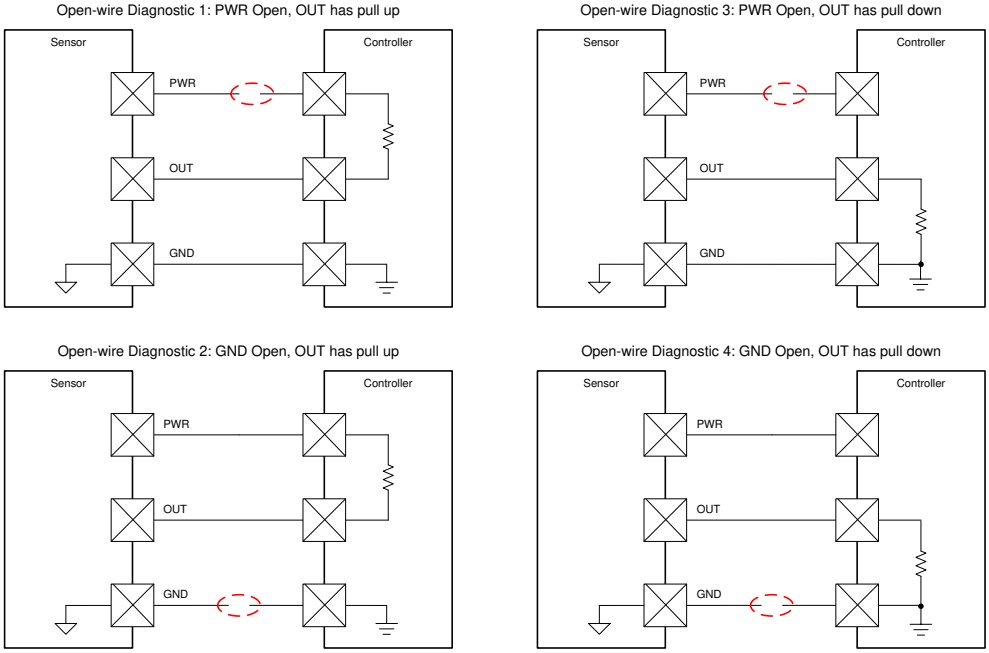


Figure 73. Harness Open-Wire Diagnostics

8.2 Typical Applications

8.2.1 4-mA to 20-mA Current Output

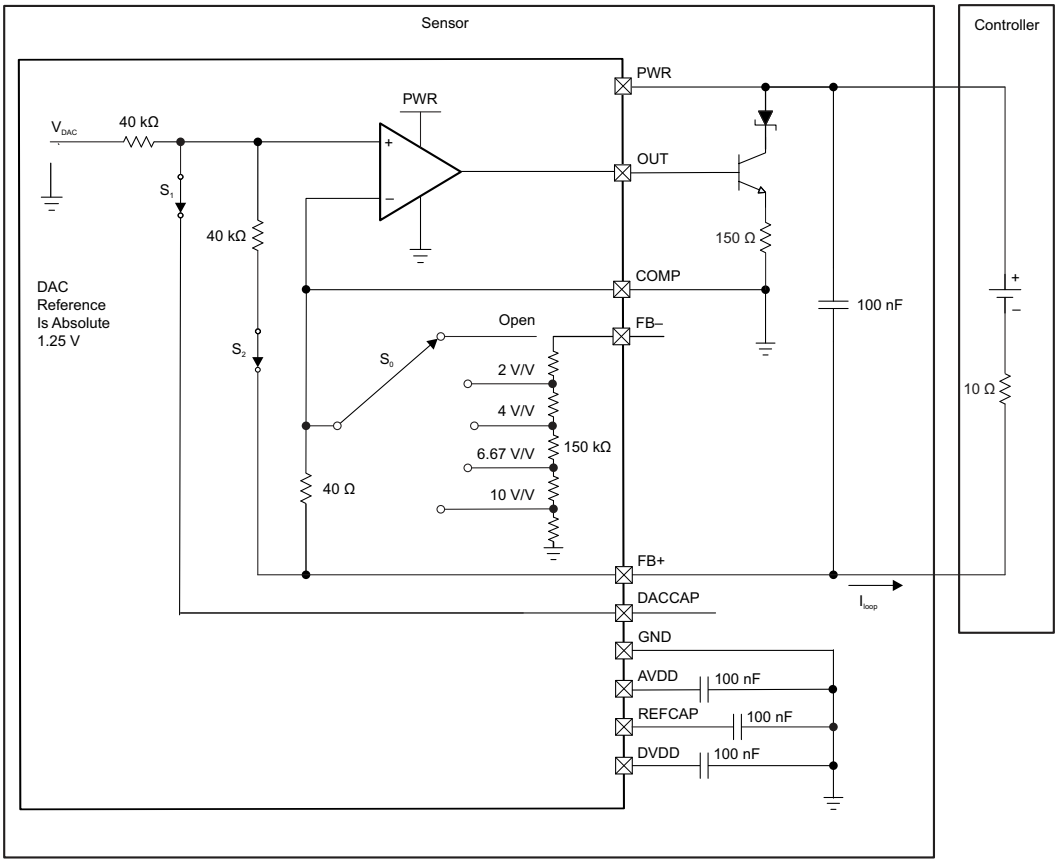


Figure 74. 4-mA to 20-mA Current Output Diagram

8.2.1.1 Design Requirements

Configure and program the PGA300 for a 4-mA to 20-mA current output using the internal current sense resistor.

Typical Applications (continued)

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 External Components

The following external components are required in order to configure the PGA300 for a 4-mA to 20-mA current output:

- Place a 100-nF capacitor from the PWR pin to ground, as close as possible to the PWR pin. Do not exceed the maximum slew rate of 0.5 V/µs at the PWR pin.
- Place a 100-nF capacitor from the AVDD pin to ground, as close as possible to the AVDD pin.
- Place a 100-nF capacitor from the DVDD pin to ground, as close as possible to the DVDD pin.
- Place a capacitor between 10 nF and 1000 nF from the REFCAP pin to ground, as close as possible to the REFCAP pin.
- Place a 150-Ω resistor between the COMP pin and the emitter of the BJT for current-loop stability purposes.
- Place a 10-Ω resistor between the FB+ pin and the negative terminal of the controller for current measurement.

8.2.1.2.2 Programming and EEPROM Settings

The following sequence must be followed to program and configure the PGA300 for current output mode:

1. Send the OWI activation-pulse sequence.
2. Set the MODE_SEL[1:0] bits in the MODE_CTRL register to 0b11 to switch into configuration mode.
3. Program 4_20MA_EN = 0b1 and DAC_GAIN[2:0] = 0b000 in the OP_STAGE_CTRL register to select current output mode.
4. Program the DAC_RATIOMETRIC bit in the DAC_CONFIG register to 0b0 to select absolute output mode.
5. Set the MODE_SEL[1:0] bits in the MODE_CTRL register to 0b00 to switch back to execution mode.

By default the PGA300 is configured to operate in current output mode.

8.2.1.3 Application Curve

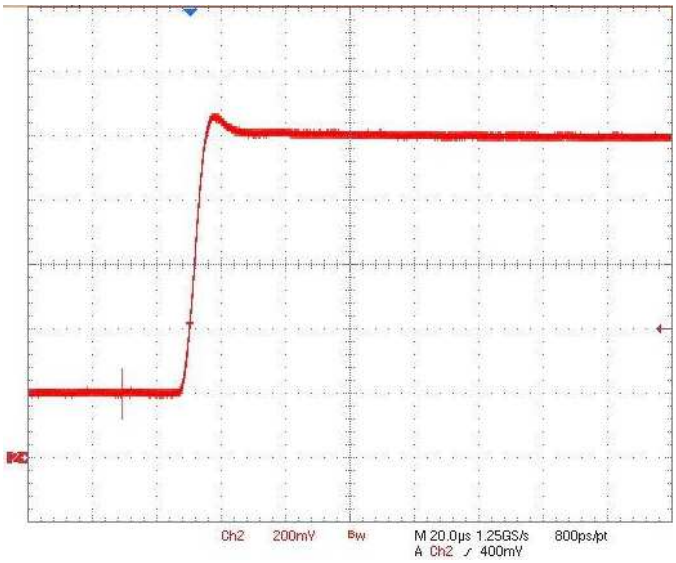


Figure 75. Loop Current Step From 4 mA to 20 mA

Voltage measured between the GND pin of the PGA300 and the negative terminal of the controller. This measurement includes the internal 40-Ω resistor and an external 10-Ω resistor, V_{PWR} = 15 V. The DAC codes used were 0x880 and 0x2760 for 4 mA and 20 mA, respectively.

Typical Applications (continued)

8.2.2 0-V to 10-V Absolute Voltage Output

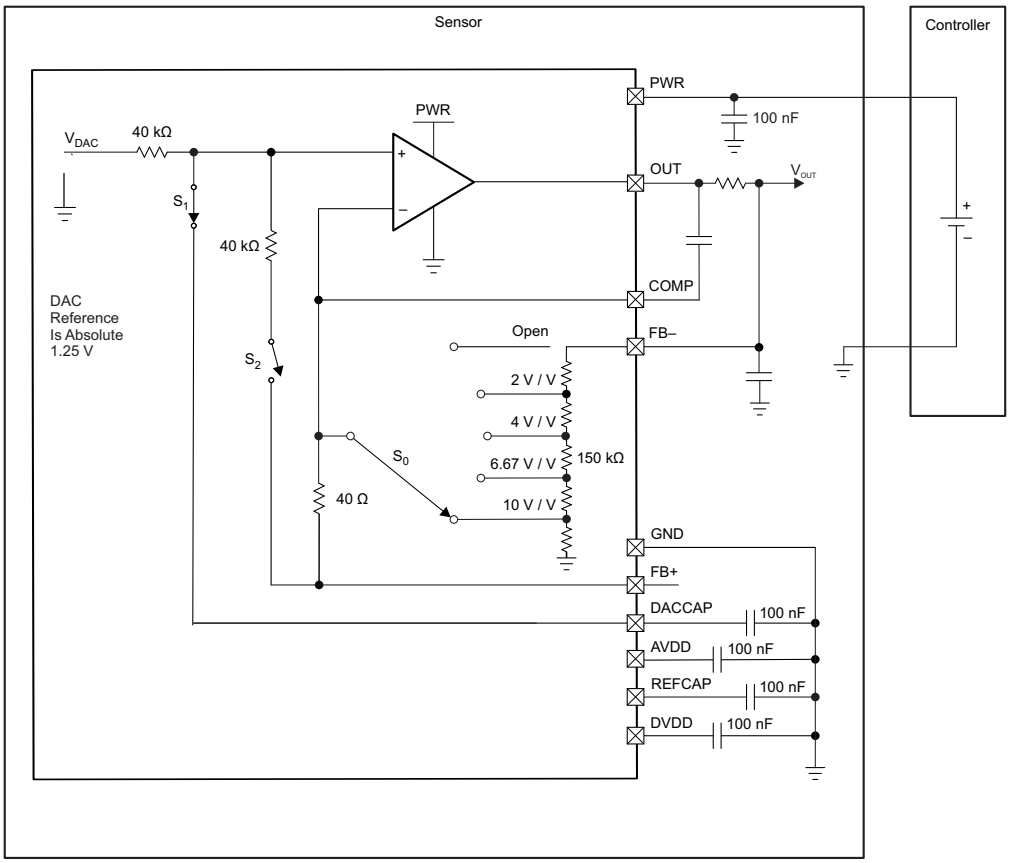


Figure 76. 0-V to 10-V Absolute Voltage Output Diagram

8.2.2.1 Design Requirements

Configure and program the PGA300 for a 0-V to 10-V absolute voltage output.

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 External Components

The following external components are required in order to configure the PGA300 for a 0-V to 10-V absolute voltage output:

- Place a 100-nF capacitor from the PWR pin to ground, as close as possible to the PWR pin. Do not exceed the maximum slew rate of 0.5 V/µs at the PWR pin.
- Place a 100-nF capacitor from the AVDD pin to ground, as close as possible to the AVDD pin.
- Place a 100-nF capacitor from the DVDD pin to ground, as close as possible to the DVDD pin.
- Place a capacitor between 10 nF and 1000 nF from the REFCAP pin to ground, as close as possible to the REFCAP pin.
- Implement compensation, using the COMP pin and an isolation resistor, when driving large capacitive loads with the OUT pin.

Typical Applications (continued)

8.2.2.2.1.1 Programming and EEPROM Settings

The following sequence must be followed to program and configure the PGA300 for absolute voltage output mode:

1. Send the OWI activation-pulse sequence.
2. Set the MODE_SEL[1:0] bits in the MODE_CTRL register to 0b11 to switch into configuration mode.
3. Program the 4_20MA_EN bit in the OP_STAGE_CTRL register to 0b0 to select voltage output mode.
4. Program the DAC_GAIN[2:0] bits in the OP_STAGE_CTRL register to 0b001 to select a DAC gain of 10 V/V.
5. Program the DACCAP_EN bit in the OP_STAGE_CTRL register to connect or disconnect the external capacitor at the DAC output.
6. Program the DAC_RATIOMETRIC bit in the DAC_CONFIG register to 0b0 to select absolute output mode.
7. Set the MODE_SEL[1:0] bits in the MODE_CTRL register to 0b00 to switch back to execution mode.

8.2.3 0-V to 5-V Ratiometric Voltage Output

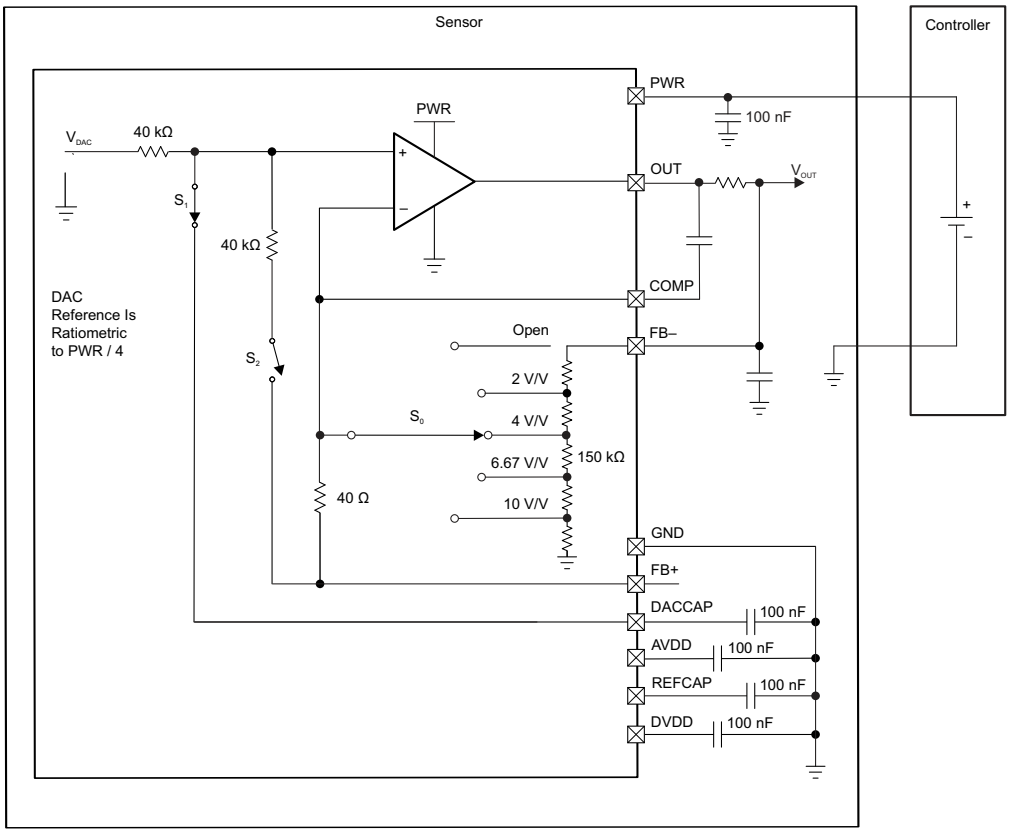


Figure 77. 0-V to 5-V Ratiometric Voltage Output Diagram

8.2.3.1 Design Requirements

Configure and program PGA300 for 0-V to 5-V ratiometric voltage output.

Typical Applications (continued)

8.2.3.2 Detailed Design Procedure

8.2.3.2.1 External Components

The following external components are required in order to configure the PGA300 for 0-V to 5-V ratiometric voltage output:

- Place a 100-nF capacitor from the PWR pin to ground, as close as possible to the PWR pin. Do not exceed the maximum slew rate of 0.5 V/µs at the PWR pin.
- Place a 100-nF capacitor from the AVDD pin to ground, as close as possible to the AVDD pin.
- Place a 100-nF capacitor from the DVDD pin to ground, as close as possible to the DVDD pin.
- Place a capacitor between 10 nF and 1000 nF from the REFCAP pin to ground, as close as possible to the REFCAP pin.
- Implement compensation, using the COMP pin and an isolation resistor, when driving large capacitive loads with the OUT pin.

8.2.3.2.2 Programming and EEPROM Settings

The following sequence must be followed to program and configure the PGA300 for absolute voltage output mode:

1. Send the OWI activation-pulse sequence.
2. Set the MODE_SEL[1:0] bits in the MODE_CTRL register to 0b11 to switch into configuration mode.
3. Program the 4_20MA_EN bit in the OP_STAGE_CTRL register to 0b0 to select voltage output mode.
4. Program the DAC_GAIN[2:0] bits in the OP_STAGE_CTRL register to 0b010 to select a DAC gain of 4 V/V.
5. Program the DACCAP_EN bit in the OP_STAGE_CTRL register to connect or disconnect the external capacitor at the DAC output.
6. Program the DAC_RATIOMETRIC bit in the DAC_CONFIG register to 0b1 to select ratiometric output mode.
7. Set the MODE_SEL[1:0] bits in the MODE_CTRL register to 0b00 to switch back to execution mode.

9 Power Supply Recommendations

The PGA300 has a single power-supply input pin (PWR). The maximum slew rate for the PWR pin is 0.5 V/µs, as specified in the *Recommended Operating Conditions* table. Faster slew rates might generate a POR. Place a 100-nF power-supply decoupling capacitor as close as possible to the PWR pin.

10 Layout

10.1 Layout Guidelines

Standard layout practices should be used when designing a board to test the PGA300. Depending on the number of layers in the board, one or more GND planes should be inserted as internal layers. However, given the limited number of external components needed for an application using the PGA300 and the number of NU pins in the device, a simple two-layer board can easily be designed. In addition, the PWR decoupling capacitor should be placed as close as possible to the PWR pin. In a similar way, the 100-nF recommended capacitors for the AVDD and DVDD regulators as well as the 10- to 1000-nF recommended capacitor for REFCAP should be placed as close as possible to their respective pins.

Depending on the application, the signal traces for FB–, FB+, COMP, and OUT should be routed such that they do not cross one another in order to minimize coupling.

When using the internal temperature sensor, thermal effects must be taken into account in the board design. Place the PGA300 as close as possible to the pressure-sensing element. This placement ensures that the internal temperature sensor has adequate thermal coupling to the sensing element. Additionally, if the device is used in 4-mA to 20-mA output mode with the internal temperature sensor, place the BJT as far away as possible from the PGA300 and the pressure-sensing element to reduce additional heating at high current outputs.

10.2 Layout Example

Figure 78 depicts the main guidelines previously discussed being implemented in a six-layer, socketed evaluation board (EVM) of the PGA300. Two main GND planes (layer 2 and 5) were used to provide a nearby GND plane to each of the signal layers and the power plane (layer 3) in the EVM. The EVM supports voltage and current output modes for the device, and as a result, GND separation is needed, depending on the application. As a result, layer 2 is a solid GND plane for the majority of the circuitry in the EVM (IRETURN). Because most of the circuitry is referred to this GND plane, layers 3 and 4 also contain copper pours connected to IRETURN. This GND plane is the return path for the supply used in the 4-mA to 20-mA loop. Layer 5 is a split plane for the ground references for the digital communication signals used for the EVM (USBGND) and the ground pins in the device (GND, AVSS and DVSS), referred to as ASICGND. The EVM provides jumpers to connect, or disconnect, these three planes one from another, depending on the desired configuration.

Figure 78 illustrates the recommended capacitors for proper operation of the PGA300. These capacitors are placed as close as possible to their respective pins of the socket used on the EVM. The signal traces for FB–, FB+, COMP, and OUT can also be observed to be routed all in the same layer to avoid crossing each other and minimize coupling.

Layout Example (continued)

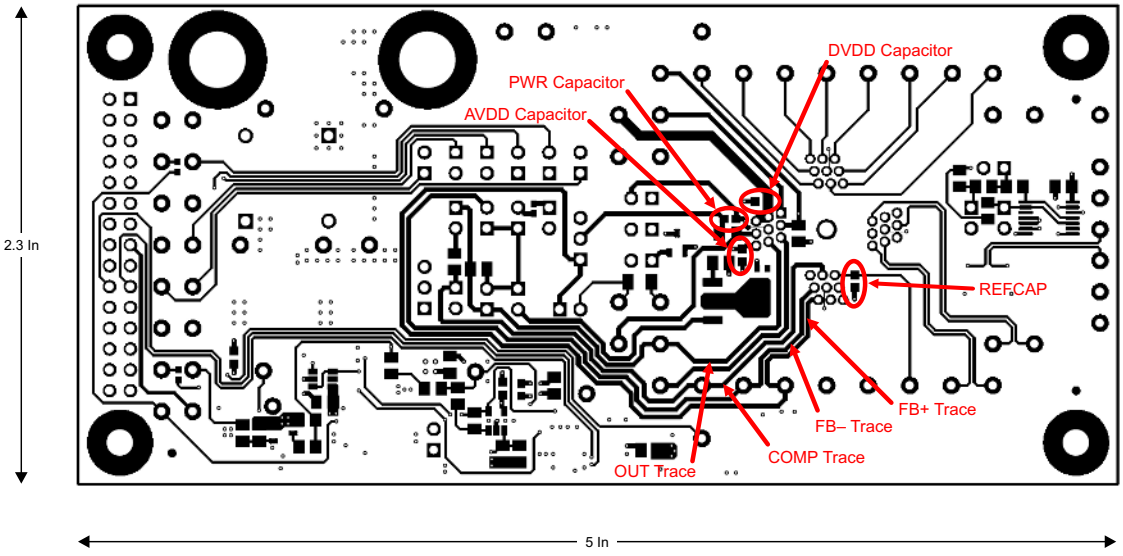


Figure 78. Layout Diagram

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *PGA900 DAC Output Stability* application note
- Texas Instruments, *PGA900 as a 4- to 20-mA Current Loop Transmitter* application note
- Texas Instruments, *Understanding Open Loop Gain of the PGA900 DAC Gain Amplifier* application note
- Texas Instruments, *Understanding Open Loop Output Impedance of the PGA900 DAC Gain Amplifier* application note

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 Trademarks

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PGA300ARHHR	ACTIVE	VQFN	RHH	36	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	PGA300A RHH	Samples
PGA300ARHHT	ACTIVE	VQFN	RHH	36	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	PGA300A RHH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

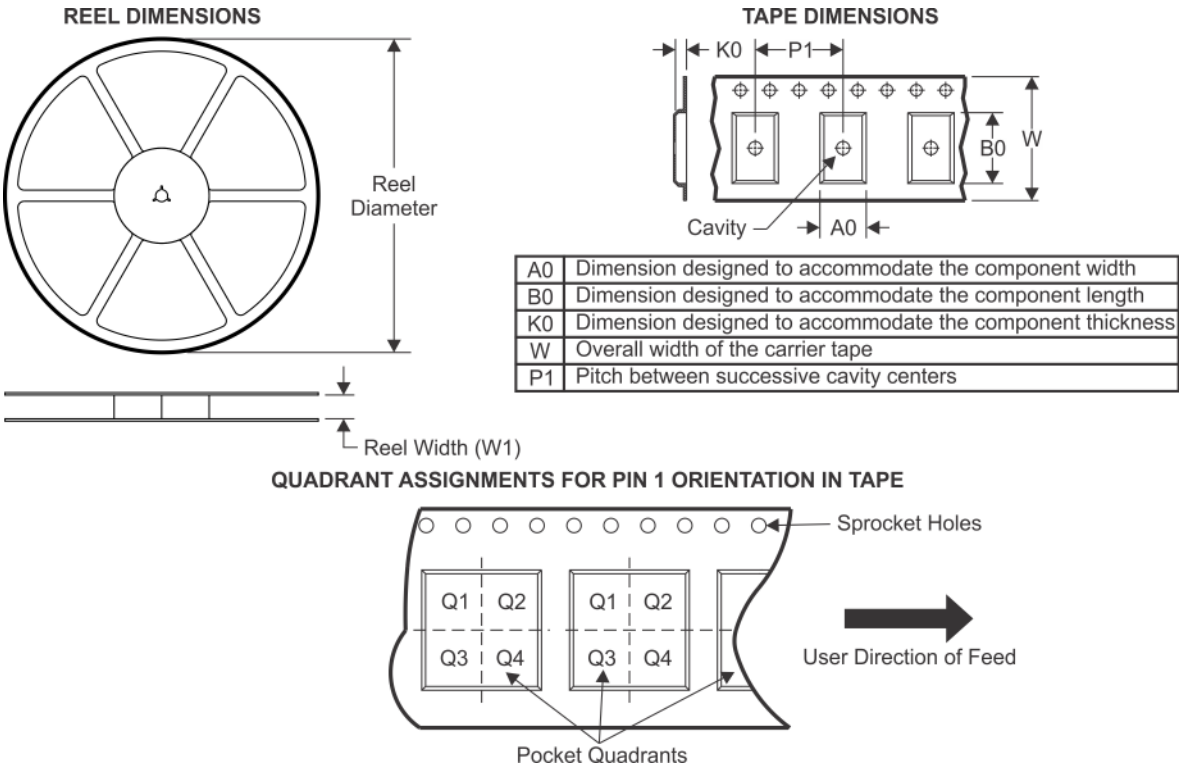
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

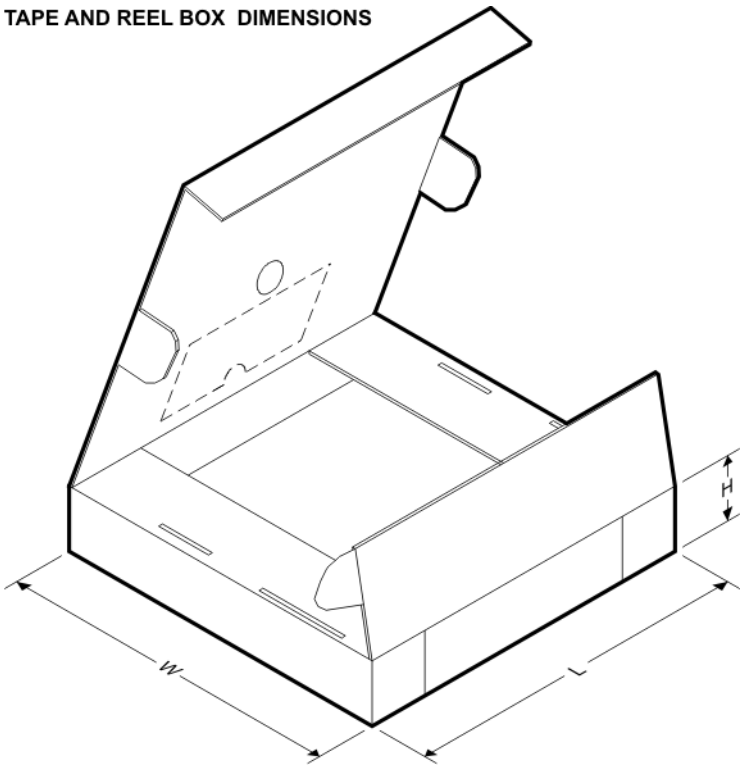


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PGA300ARHHR	VQFN	RHH	36	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
PGA300ARHHT	VQFN	RHH	36	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PGA300ARHHR	VQFN	RHH	36	2500	367.0	367.0	38.0
PGA300ARHHT	VQFN	RHH	36	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

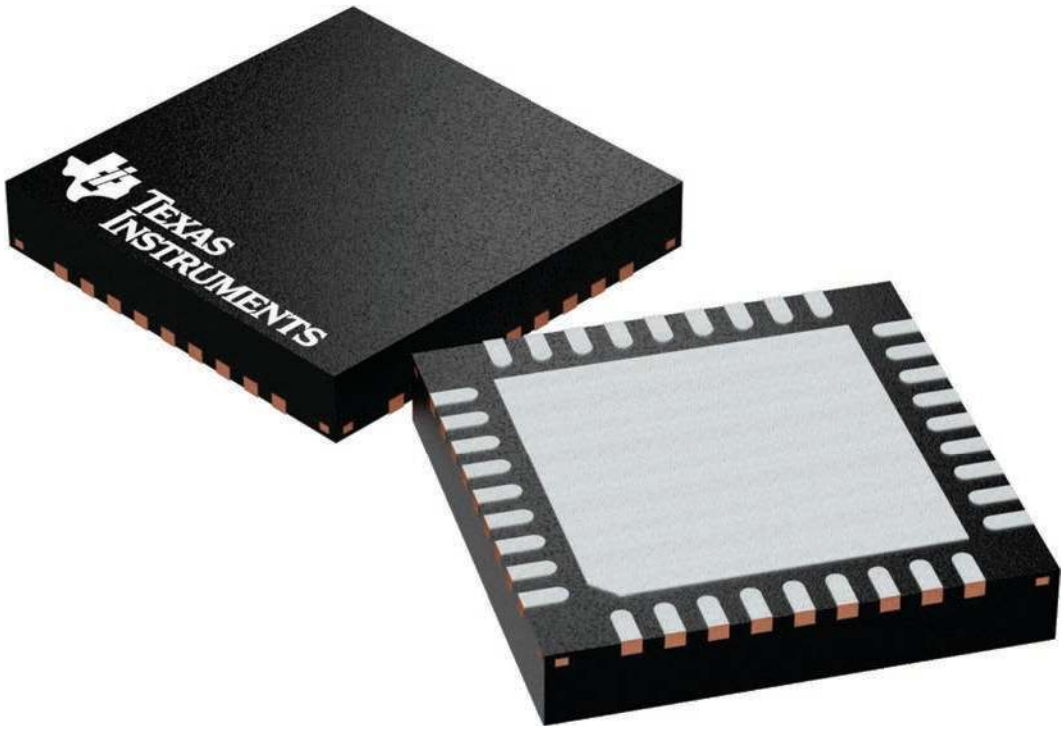
RHH 36

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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