

# NP75P04YLG

R07DS0183EJ0200

Rev.2.00

Mar 16, 2011

## MOS FIELD EFFECT TRANSISTOR

### Description

The NP75P04YLG is P-channel MOS Field Effect Transistor designed for high current switching applications.

### Features

- Low on-state resistance
  - $R_{DS(on)} = 9.7 \text{ m}\Omega \text{ MAX.}$  ( $V_{GS} = -10 \text{ V}$ ,  $I_D = -37.5 \text{ A}$ )
  - $R_{DS(on)} = 14 \text{ m}\Omega \text{ MAX.}$  ( $V_{GS} = -5 \text{ V}$ ,  $I_D = -37.5 \text{ A}$ )
- Logic level drive type
- Gate to Source ESD protection diode built in
- Designed for automotive application and AEC-Q101 qualified

### Ordering Information

Part No.	LEAD PLATING	PACKING	Package
NP75P04YLG -E1-AY <sup>*1</sup>	Pure Sn (Tin)	Tape 2500 p/reel	8-pin HSON, Taping (E1 type)
NP75P04YLG -E2-AY <sup>*1</sup>			8-pin HSON, Taping (E2 type)

Note: <sup>\*1</sup>. Pb-free (This product does not contain Pb in the external electrode.)

### Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ )

Item	Symbol	Ratings	Unit
Drain to Source Voltage ( $V_{GS} = 0 \text{ V}$ )	$V_{DSS}$	-40	V
Gate to Source Voltage ( $V_{DS} = 0 \text{ V}$ )	$V_{GSS}$	$\mp 20$	V
Drain Current (DC) ( $T_C = 25^\circ\text{C}$ )	$I_{D(DC)}$	$\mp 75$	A
Drain Current (pulse) <sup>*1</sup>	$I_{D(pulse)}$	$\mp 225$	A
Total Power Dissipation ( $T_C = 25^\circ\text{C}$ )	$P_{T1}$	138	W
Total Power Dissipation ( $T_A = 25^\circ\text{C}$ ) <sup>*2</sup>	$P_{T2}$	1.0	W
Channel Temperature	$T_{ch}$	175	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +175	$^\circ\text{C}$
Single Avalanche Current <sup>*3</sup>	$I_{AS}$	35	A
Single Avalanche Energy <sup>*3</sup>	$E_{AS}$	123	mJ

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### Thermal Resistance

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	1.09	$^\circ\text{C/W}$
Channel to Ambient Thermal Resistance <sup>*2</sup>	$R_{th(ch-A)}$	150	$^\circ\text{C/W}$

Notes: <sup>\*1</sup>.  $T_C = 25^\circ\text{C}$ ,  $PW \leq 10 \mu\text{s}$ , Duty Cycle  $\leq 1\%$

<sup>\*2</sup>. Mounted on glass epoxy substrate of 40 mm x 40 mm x 0.8 mm

<sup>\*3</sup>. Starting  $T_{ch} = 25^\circ\text{C}$ ,  $V_{DD} = -20 \text{ V}$ ,  $R_G = 25 \Omega$ ,  $L = 100 \mu\text{H}$ ,  $V_{GS} = -20 \rightarrow 0 \text{ V}$

The mark <R> shows major revised points.

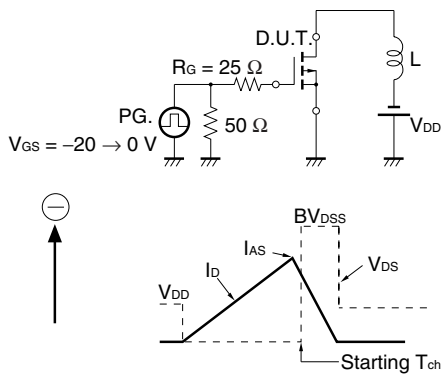
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

**Electrical Characteristics (T<sub>A</sub> = 25°C)**

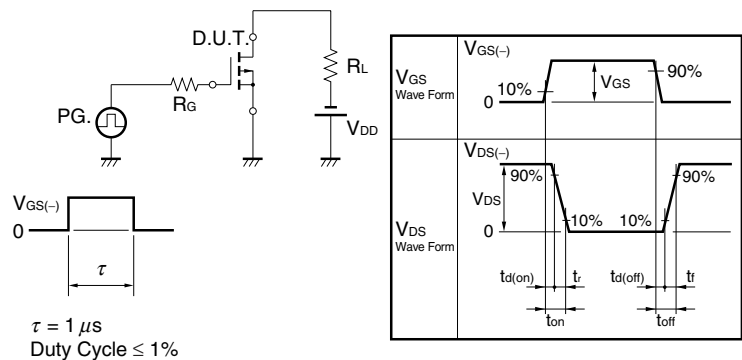
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I <sub>DSS</sub>			-1	μA	V <sub>DS</sub> = -40 V, V <sub>GS</sub> = 0 V
Gate Leakage Current	I <sub>GSS</sub>			±10	μA	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V
Gate to Source Threshold Voltage	V <sub>GS(th)</sub>	-1.0	-1.7	-2.5	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>b</sub> = -250 μA
Forward Transfer Admittance *1	y <sub>fs</sub>	31	63		S	V <sub>DS</sub> = -5 V, I <sub>D</sub> = -37.5 A
Drain to Source On-state Resistance *1	R <sub>DS(on)1</sub>		7.7	9.7	mΩ	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -37.5 A
	R <sub>DS(on)2</sub>		9.3	14	mΩ	V <sub>GS</sub> = -5 V, I <sub>D</sub> = -37.5 A
Input Capacitance	C <sub>iss</sub>		3200	4800	pF	V <sub>DS</sub> = -25 V, V <sub>GS</sub> = 0 V, f = 1 MHz
Output Capacitance	C <sub>oss</sub>		460	600	pF	
Reverse Transfer Capacitance	C <sub>rss</sub>		250	450	pF	
Turn-on Delay Time	t <sub>d(on)</sub>		12	24	ns	V <sub>DD</sub> = -20 V, I <sub>D</sub> = -37.5 A, V <sub>GS</sub> = -10 V, R <sub>G</sub> = 0 Ω
Rise Time	t <sub>r</sub>		11	27	ns	
Turn-off Delay Time	t <sub>d(off)</sub>		320	640	ns	
Fall Time	t <sub>f</sub>		180	440	ns	
Total Gate Charge	Q <sub>G</sub>		91	140	nC	V <sub>DD</sub> = -32 V, V <sub>GS</sub> = -10 V, I <sub>D</sub> = -75 A
Gate to Source Charge	Q <sub>GS</sub>		14		nC	
Gate to Drain Charge	Q <sub>GD</sub>		26		nC	
Body Diode Forward Voltage *1	V <sub>F(S-D)</sub>		1.02	1.5	V	I <sub>F</sub> = -75 A, V <sub>GS</sub> = 0 V
Reverse Recovery Time	t <sub>rr</sub>		43		ns	I <sub>F</sub> = -75 A, V <sub>GS</sub> = 0 V,
Reverse Recovery Charge	Q <sub>rr</sub>		57		nC	di/dt = -100 A/μs

Note: \*1. Pulsed

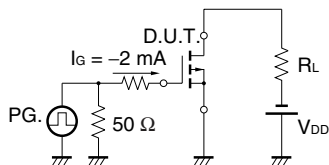
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



**TEST CIRCUIT 2 SWITCHING TIME**

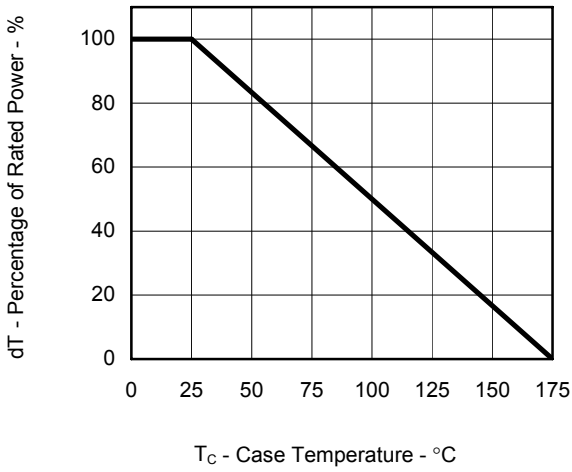


**TEST CIRCUIT 3 GATE CHARGE**

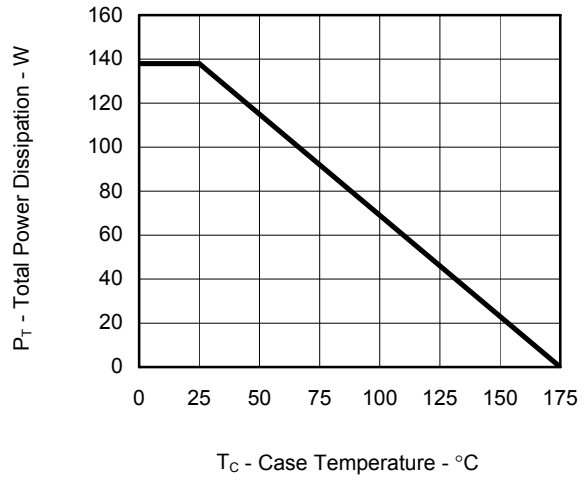


Typical Characteristics (T<sub>A</sub> = 25°C)

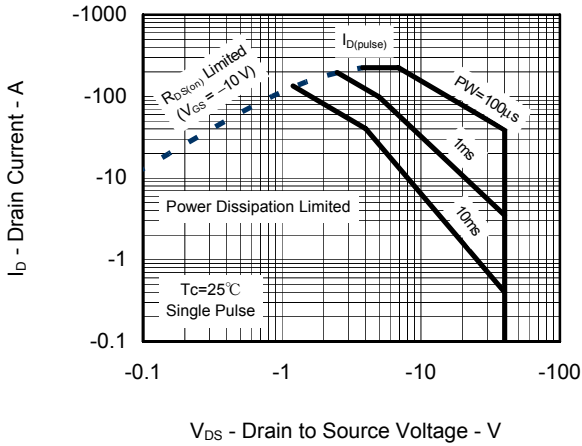
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



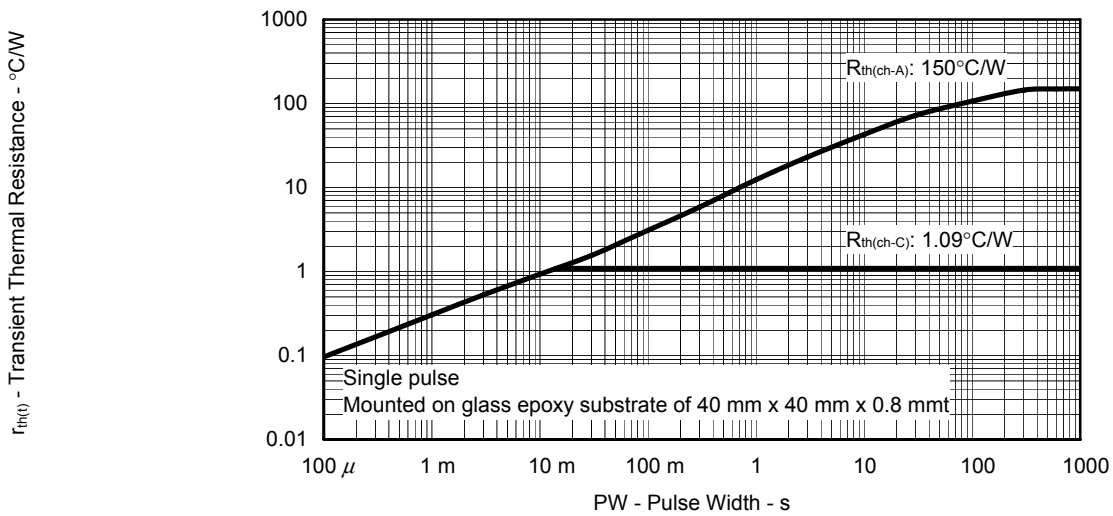
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



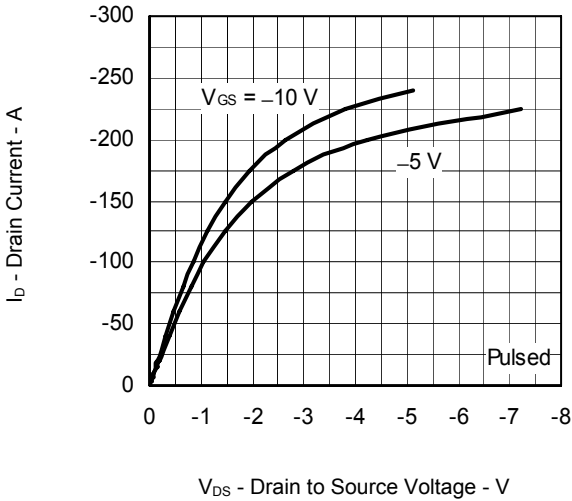
FORWARD BIAS SAFE OPERATING AREA



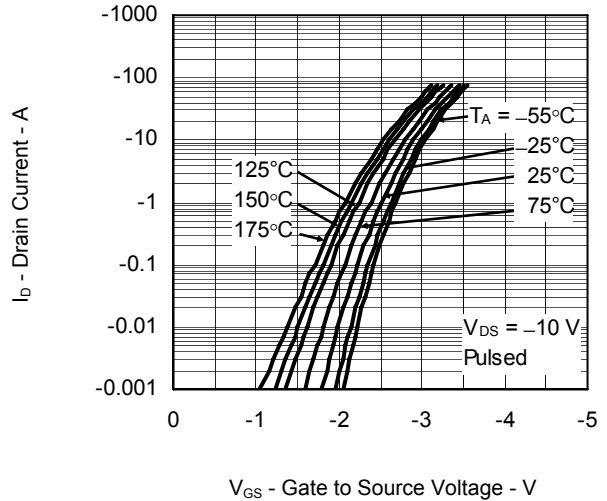
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



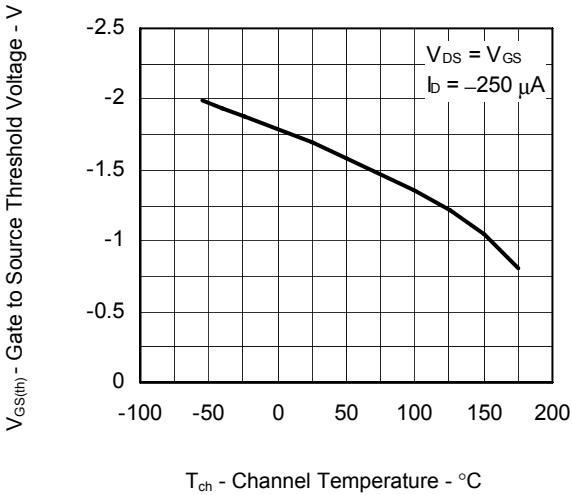
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



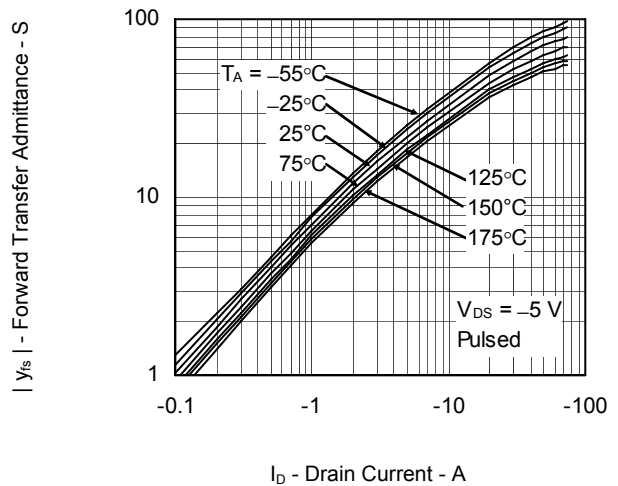
FORWARD TRANSFER CHARACTERISTICS



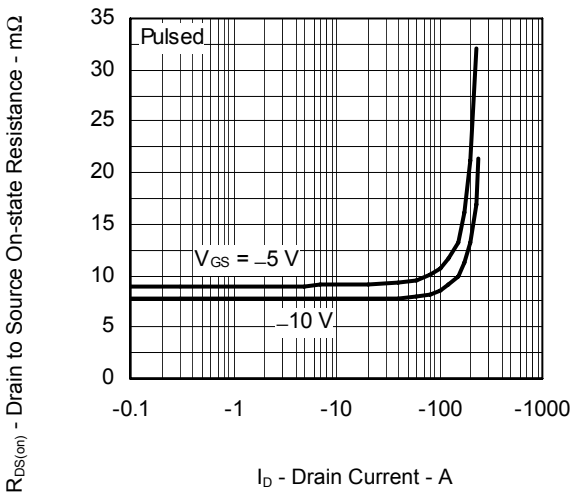
GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



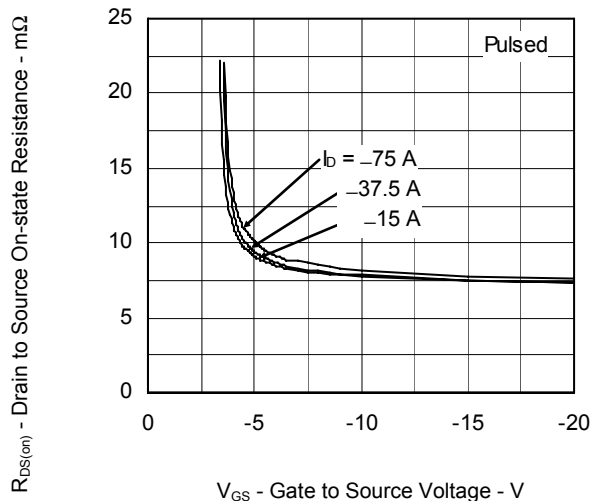
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



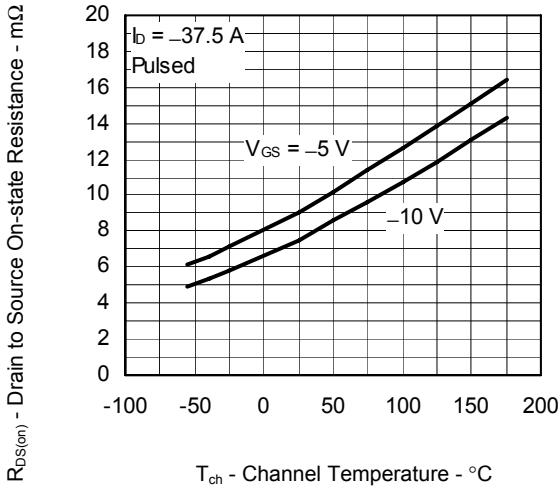
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



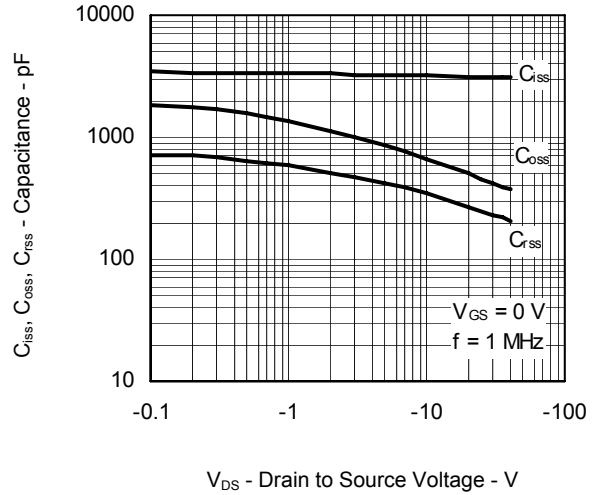
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



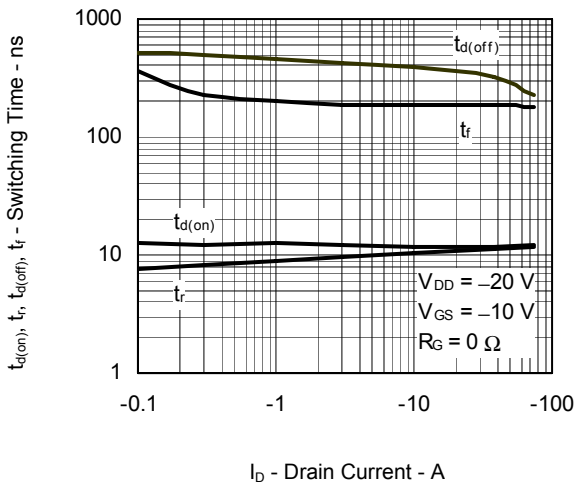
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



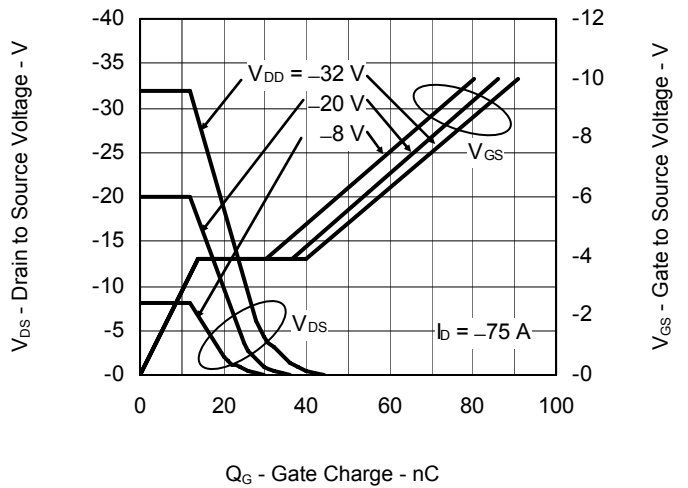
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



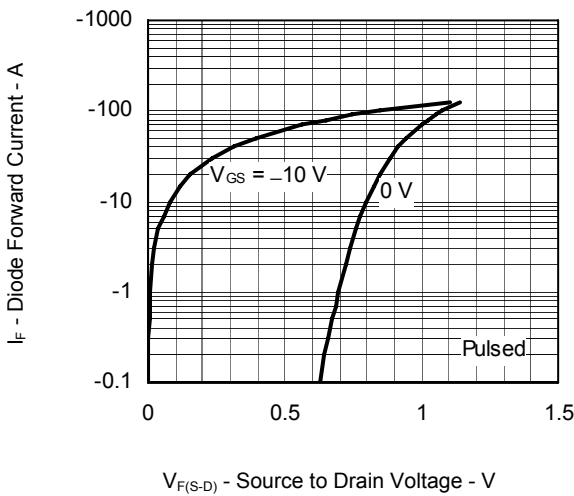
SWITCHING CHARACTERISTICS



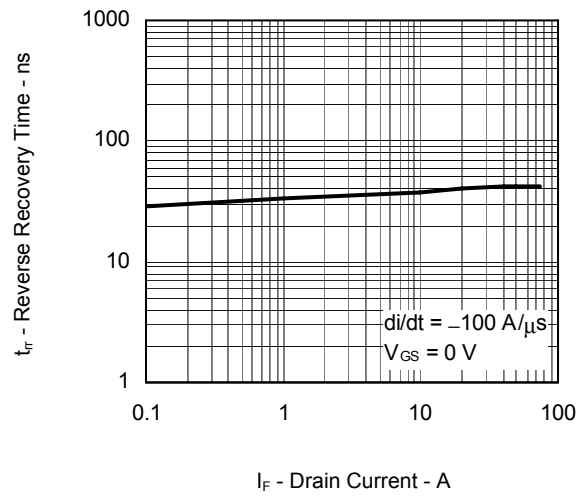
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

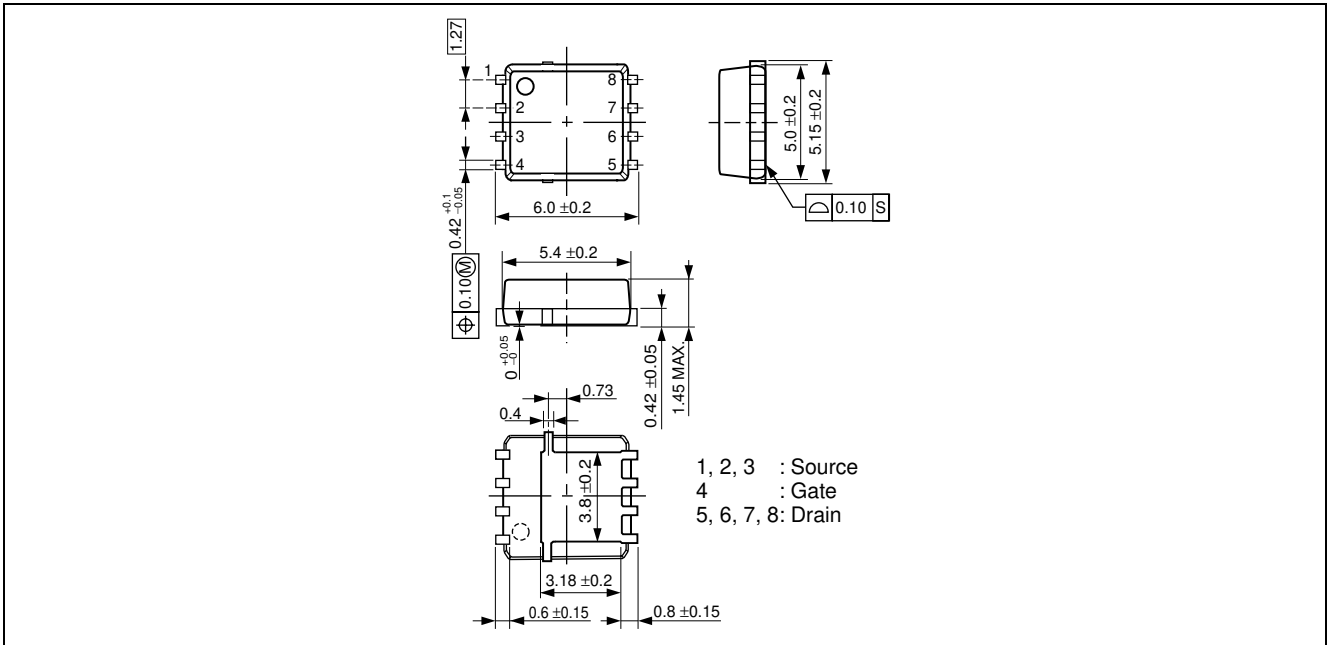


REVERSE RECOVERY TIME vs. DRAIN CURRENT

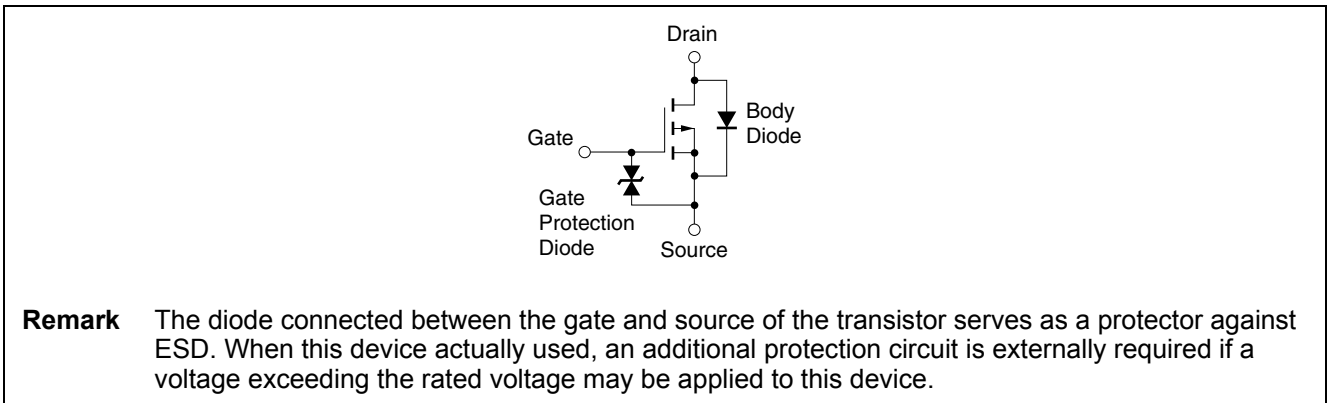


Package Drawings (Unit: mm)

8-pin HSON (Mass: 0.13 g TYP.)



Equivalent Circuit



<b>Revision History</b>	<b>NP75P04YLG Data Sheet</b>
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Rev.	Date	Description	
		Page	Summary
1.00	Oct 22, 2010	-	First Edition Issued
2.00	Mar 16, 2011	p.1	Repetitive Avalanche Current -> Single Avalanche Current Repetitive Avalanche Energy -> Single Avalanche Energy Modification of Note *3

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