TPS795 Ultralow-Noise, High-PSRR, Fast, RF, 500-mA, Low-Dropout Linear Regulators

1 Features

- 500-mA low-dropout regulator with enable
- Available in fixed and adjustable (1.2-V to 5.5-V) versions
- High PSRR (50 dB at 10 kHz)
- Ultralow noise (33 µV_{RMS}, TPS79530)
- Fast start-up time (50 µs)
- Stable with a 1-µF ceramic capacitor
- Excellent load and line transient response
- Low dropout voltage (110 mV at full load, TPS79530)
- 6-pin SOT-223 and 3-mm × 3-mm VSON packages

2 Applications

- RF: VCOs, receivers, ADCs
- Audio
- Bluetooth®, wireless LAN
- Cellular and cordless telephones
- Handheld organizers, PDAs

3 Description

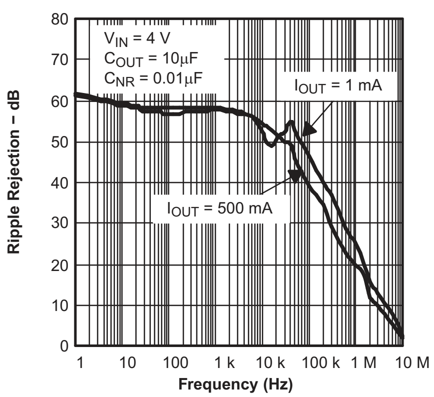
The TPS795 family of low-dropout (LDO), low-power linear voltage regulators features high power-supply rejection ratio (PSRR), ultralow noise, fast start-up, and excellent line and load transient responses in small outline, 6-pin SOT-223 and 3-mm × 3-mm VSON packages. Each device in the family is stable with a small 1-µF ceramic capacitor on the output. The family uses an advanced, proprietary BiCMOS fabrication process to yield extremely low dropout voltages (for example, 110 mV at 500 mA). Each device achieves fast start-up times (approximately 50 µs with a 0.001-µF bypass capacitor) while consuming very low quiescent current (265 µA, typical). Moreover, when the device is placed in standby mode, the supply current is reduced to less than 1 µA. The TPS79530 device exhibits approximately 33 µV_{RMS} of output voltage noise at 3-V output with a 0.1-µF bypass capacitor. Applications with analog components that are noise-sensitive, such as portable RF electronics, benefit from the high-PSRR and low-noise features, as well as from the fast response time.

Device Information(1)

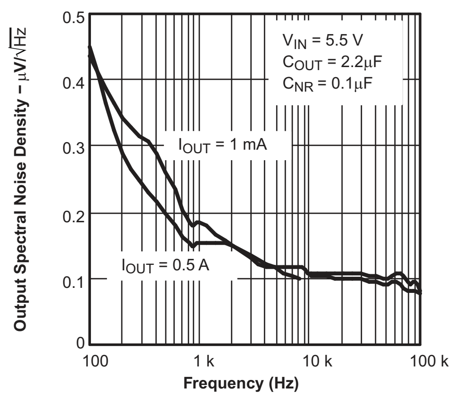
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS795	SOT-223 (6)	6.50 mm × 3.50 mm
	VSON (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

TPS79530 Ripple Rejection vs Frequency



TPS79530 vs Frequency



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

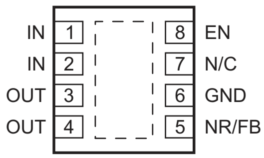
Changes from Revision I (May 2015) to Revision J	Page
• Changed DRB package name throughout data sheet from SON to VSON	1
• Changed *Pin Configuration* package names; switched designators to match correct package names (typo)	3
• Added note (1) to *Recommended Operating Conditions*; moved from *Electrical Characteristics*	4
• Changed thermal values in *Thermal Information* table	4
• Deleted *Input Voltage* from *Electrical Characteristics*; already shown in *Recommended Operating Conditions*	5
• Deleted *Junction Temperature* from *Electrical Characteristics*; already shown in *Recommended Operating Conditions*	5

Changes from Revision H (August 2010) to Revision I	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Changed front-page graphic	1
• Changed *Pin Configuration and Functions* section; updated table format and added pinout drawings	3
• Changed "free-air" to "junction" temperature in condition statement for *Absolute Maximum Ratings*	3
• Added Added *Operating junction temperature* specification to *Electrical Characteristics*	5
• Deleted Start-up time symbol	5
• Corrected min value for $I_{EN(HI)}$ parameter	5
• Added *Thermal shutdown temperature* specification to *Electrical Characteristics*	5
• Added condition statement to *Typical Characteristics* section	6
• Changed title for *Thermal Protection* section	16

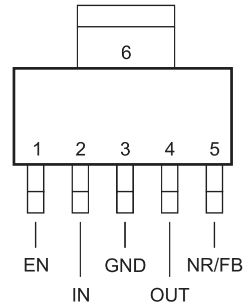
Changes from Revision G (July, 2006) to Revision H	Page
• Replaced the *Dissipation Ratings* table with the *Thermal Information* table	4
• Updated the *Thermal Protection* section	16

5 Pin Configuration and Functions

DRB Package
8-Pin VSON
Top View



DCQ Package
6-Pin SOT-223
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	VSON	SOT-223		
IN	1, 2	2	I	Unregulated input to the device
GND	6	3, 6	—	Regulator ground
EN	8	1	I	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. EN can be connected to IN if not used.
NR	5	5	—	Noise-reduction pin for fixed versions only. Connecting an external capacitor to this pin bypasses noise generated by the internal bandgap, which improves power-supply rejection and reduces output noise. ***(Not available on adjustable versions.)***
FB	5	5	I	Feedback input voltage for the adjustable device. ***(Not available on fixed voltage versions.)***
OUT	3, 4	4	O	Regulator output
N/C	7	–	—	No internal connection

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	IN	–0.3	6	V
	EN	–0.3	V_{IN} + 0.3	
	OUT		6	
Current	Peak output	Internally limited		A
Power dissipation	Continuous total	See *Thermal Information*		
Temperature	Junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage (1)	2.7		5.5	V
I_{OUT}	Output current	0		500	mA
T_J	Operating junction temperature	–40		125	°C

(1) Minimum V_{IN} is 2.7 V or V_{OUT} + V_{DO}, whichever is greater.

6.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC (1)(2)		TPS795 (3)		UNIT
		DRB (VSON)	DCQ (SOT-223)	
		6 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46.8	74.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.1	44.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18.4	8.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	3.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	18.4	8.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.3	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.
(3) Thermal data for the DRB and DCQ packages are derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:
(a) i. DRB: The exposed pad is connected to the PCB ground layer through a 2-mm x 2-mm thermal via array.
ii. DCQ: The exposed pad is connected to the PCB ground layer through a 3-mm x 2-mm thermal via array.
(b) i. DRB: The top and bottom copper layers are assumed to have a 20% thermal conductivity of copper representing a 20% copper coverage.
ii. DCQ: Each of top and bottom copper layers has a dedicated pattern for 20% copper coverage.
(c) These data were generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3in × 3in copper area. To understand the effects of the copper area on thermal performance, see *Thermal Considerations* and *Estimating Junction Temperature* of this data sheet.

6.5 Electrical Characteristics

over recommended operating temperature range (T_J = –40°C to 125°C), $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)}$ + 1 V[(1)], I_{OUT} = 1 mA, C_{OUT} = 10 µF, and C_{NR} = 0.01 µF (unless otherwise noted); typical values are at 25°C

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{FB}	Internal reference (TPS79501)				1.200	1.225	1.25	V
	Output voltage range	TPS79501			1.225		5.5 – V_{DO}	V
	Accuracy	TPS79501[(2)]	0 µA ≤ I_{OUT} ≤ 500 mA, $V_{OUT(nom)}$ + 1 V ≤ V_{IN} ≤ 5.5 V[(1)]		0.98$V_{OUT(nom)}$	$V_{OUT(nom)}$	1.02$V_{OUT(nom)}$	V
		Fixed V_{OUT} < 5 V	0 µA ≤ I_{OUT} ≤ 500 mA, $V_{OUT(nom)}$ + 1 V ≤ V_{IN} ≤ 5.5 V[(1)]		–2%		2%	
$\Delta V_{O(\Delta VI)}$	Line regulation[(1)]		V_{OUT} + 1 V ≤ V_{IN} ≤ 5.5 V			0.05	0.12	%/V
$\Delta V_{O(\Delta IO)}$	Load regulation		0 µA ≤ I_{OUT} ≤ 500 mA			3		mV
V_{DO}	Dropout voltage[(3)] ($V_{IN} = V_{OUT(nom)}$ – 0.1 V)	TPS79530	I_{OUT} = 500 mA			110	170	mV
		TPS79533	I_{OUT} = 500 mA			105	160	mV
I_{CL}	Output current limit		V_{OUT} = 0 V		2.4	2.8	4.2	A
I_{GND}	Ground pin current		0 µA ≤ I_{OUT} ≤ 500 mA			265	385	µA
I_{SHDN}	Shutdown current[(4)]		V_{EN} = 0 V, 2.7 V ≤ V_{IN} ≤ 5.5 V			0.07	1	µA
I_{FB}	Feedback pin current		V_{FB} = 1.225 V				1	µA
PSRR	Power-supply rejection ratio (TPS79530)		f = 100 Hz, I_{OUT} = 10 mA			59		dB
			f = 100 Hz, I_{OUT} = 500 mA			58		dB
			f = 10 kHz, I_{OUT} = 500 mA			50		dB
			f = 100 kHz, I_{OUT} = 500 mA			39		dB
V_n	Output noise voltage (TPS79530)		BW = 100 Hz to 100 kHz, I_{OUT} = 500 mA	C_{NR} = 0.001 µF		46		μV_{RMS}
				C_{NR} = 0.0047 µF		41		μV_{RMS}
				C_{NR} = 0.01 µF		35		μV_{RMS}
				C_{NR} = 0.1 µF		33		μV_{RMS}
	Start-up time (TPS79530)		R_L = 6 Ω, C_{OUT} = 1 µF	C_{NR} = 0.001 µF		50		µs
				C_{NR} = 0.0047 µF		75		µs
				C_{NR} = 0.01 µF		110		µs
$V_{EN(HI)}$	Enable high (enabled)		2.7 V ≤ V_{IN} ≤ 5.5 V		1.7		V_{IN}	V
$V_{EN(LO)}$	Enable low (shutdown)		2.7 V ≤ V_{IN} ≤ 5.5 V				0.7	V
$I_{EN(HI)}$	Enable pin current, enabled		V_{EN} = 0 V		–1		1	µA
UVLO	Undervoltage lockout		V_{CC} rising		2.25		2.65	V
	UVLO hysteresis					100		mV
T_{sd}	Thermal shutdown temperature		Shutdown, temperature increasing			165		°C
			Reset, temperature decreasing			140		°C

(1) Minimum V_{IN} is 2.7 V or V_{OUT} + V_{DO}, whichever is greater.
(2) Tolerance of external resistors not included in this specification.
(3) Dropout is not measured for the TPS79501 and TPS79525 because minimum V_{IN} = 2.7 V.
(4) For adjustable version, this applies only after V_{IN} is applied; then V_{EN} transitions high to low.

6.6 Typical Characteristics

at $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)} + 1$ V, $I_{OUT} = 1$ mA, $C_{OUT} = 10$ µF, $C_{NR} = 0.01$ µF, $C_{IN} = 2.2$ µF, and $T_J = 25°C$ (unless otherwise noted)

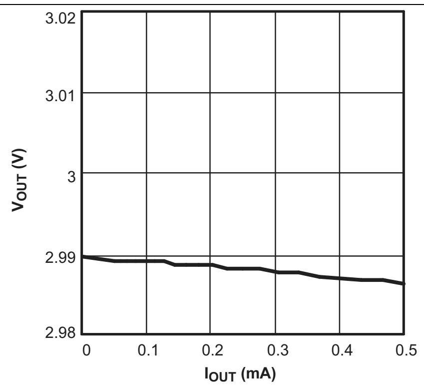


Figure 1. TPS79530 Output Voltage vs Output Current

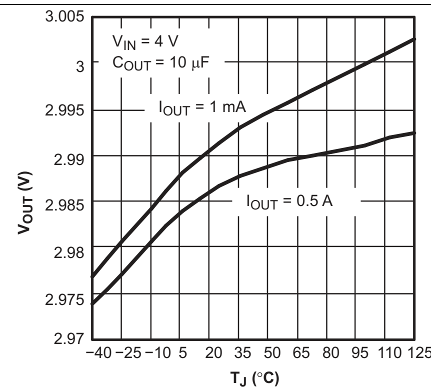


Figure 2. TPS79530 Output Voltage vs Junction Temperature

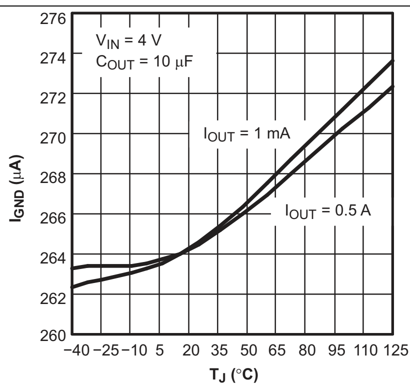


Figure 3. TPS79530 Ground Current vs Junction Temperature

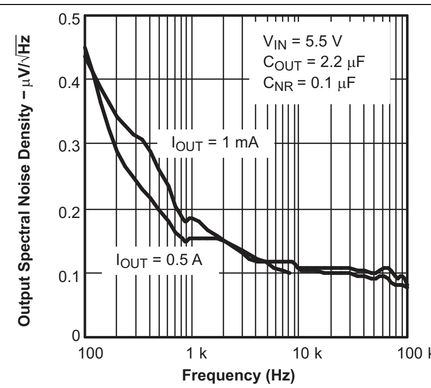


Figure 4. TPS79530 Output Spectral Noise Density vs Frequency

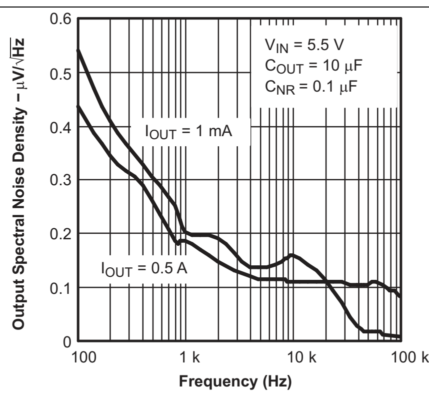


Figure 5. TPS79530 Output Spectral Noise Density vs Frequency

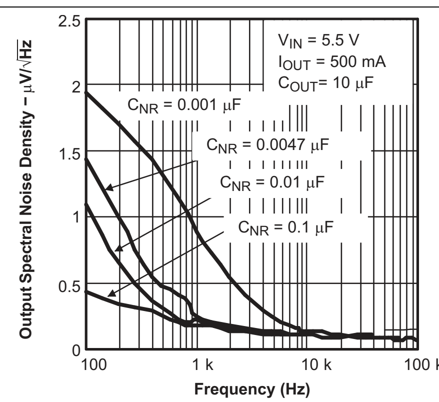


Figure 6. TPS79530 Output Spectral Noise Density vs Frequency

Typical Characteristics (continued)

at $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)} + 1$ V, $I_{OUT} = 1$ mA, $C_{OUT} = 10$ µF, $C_{NR} = 0.01$ µF, $C_{IN} = 2.2$ µF, and $T_J = 25°C$ (unless otherwise noted)

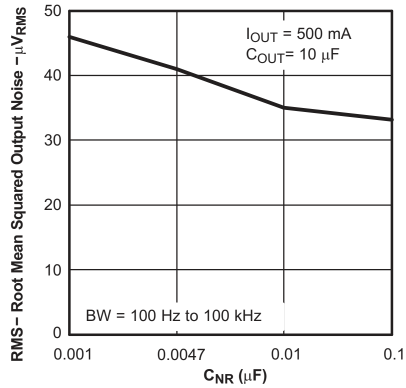


Figure 7. TPS79530 Root Mean Squared Output Noise vs C_{NR}

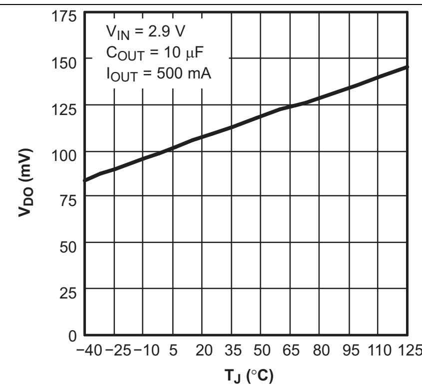


Figure 8. TPS79530 Dropout Voltage vs Junction Temperature

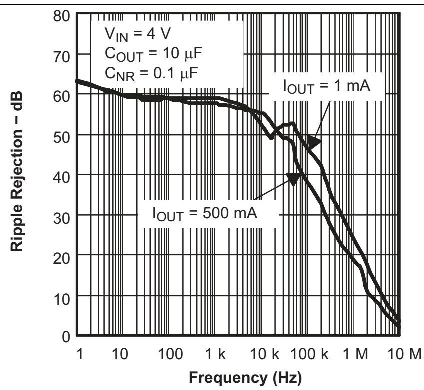


Figure 9. TPS79530 Ripple Rejection vs Frequency

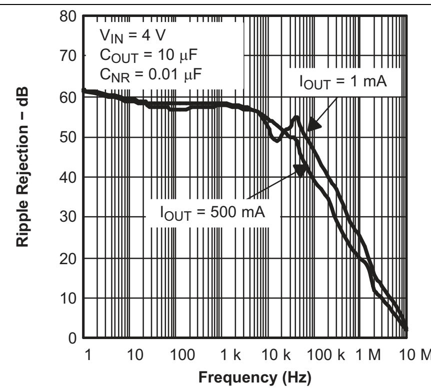


Figure 10. TPS79530 Ripple Rejection vs Frequency

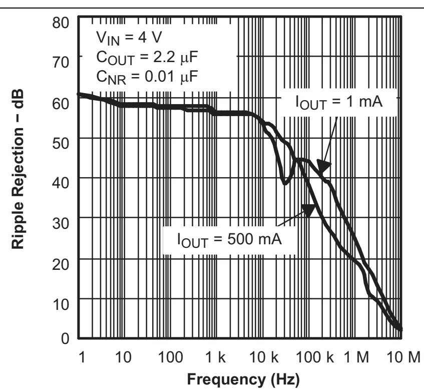


Figure 11. TPS79530 Ripple Rejection vs Frequency

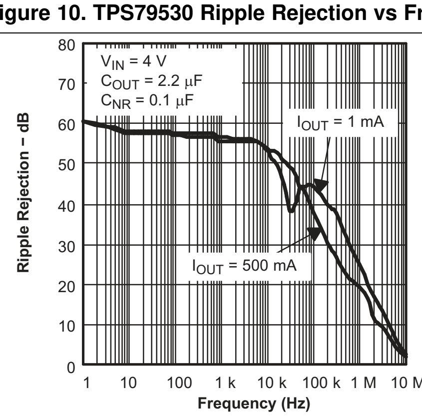


Figure 12. TPS79530 Ripple Rejection vs Frequency

Typical Characteristics (continued)

at $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)} + 1$ V, $I_{OUT} = 1$ mA, $C_{OUT} = 10$ µF, $C_{NR} = 0.01$ µF, $C_{IN} = 2.2$ µF, and $T_J = 25°C$ (unless otherwise noted)

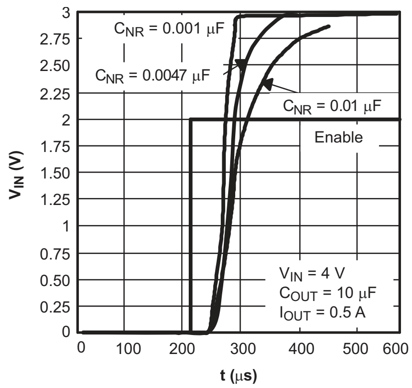


Figure 13. TPS79530 Start-Up Time

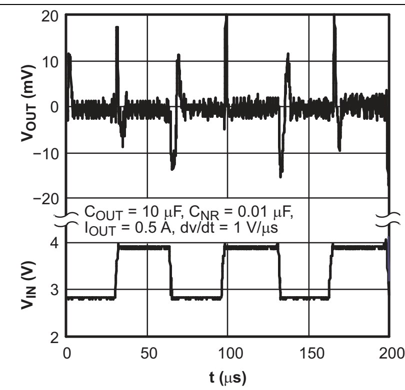


Figure 14. TPS79518 Line Transient Response

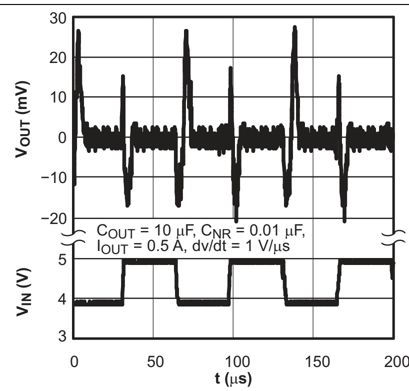


Figure 15. TPS79530 Line Transient Response

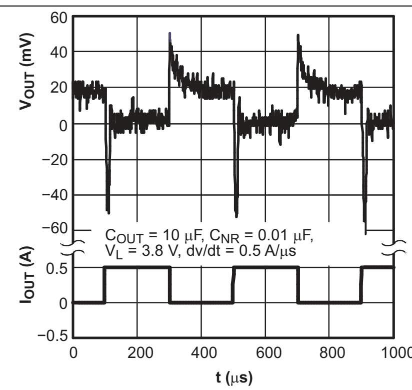


Figure 16. TPS79530 Load Transient Response

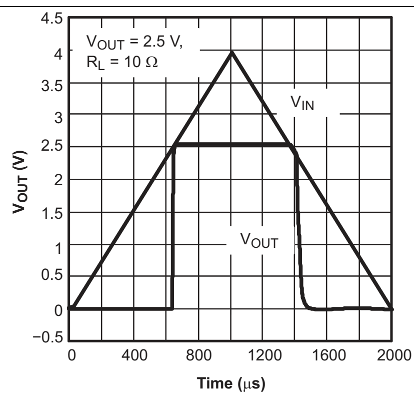


Figure 17. TPS79525 Power Up and Power Down

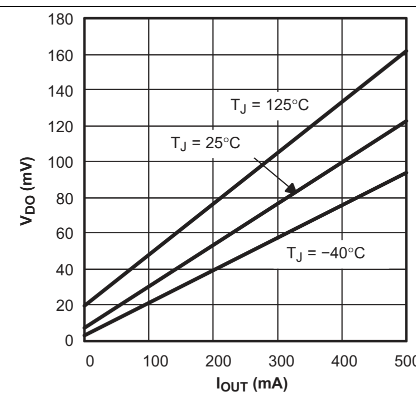


Figure 18. TPS79530 Dropout Voltage vs Output Current

Typical Characteristics (continued)

at $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)} + 1$ V, $I_{OUT} = 1$ mA, $C_{OUT} = 10$ µF, $C_{NR} = 0.01$ µF, $C_{IN} = 2.2$ µF, and $T_J = 25°C$ (unless otherwise noted)

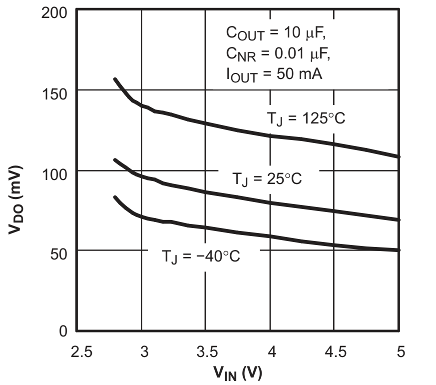


Figure 19. TPS79501 Dropout Voltage vs Input Voltage

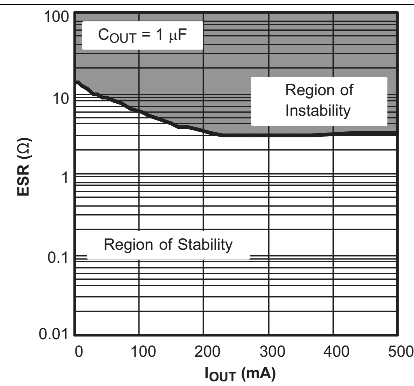


Figure 20. TPS79530 Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

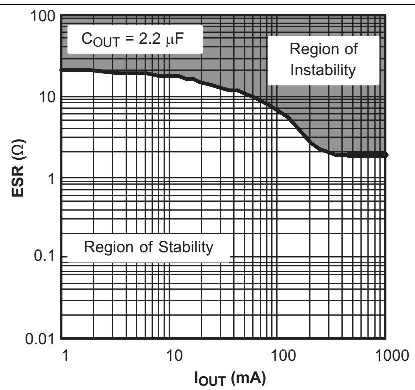


Figure 21. TPS79530 Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

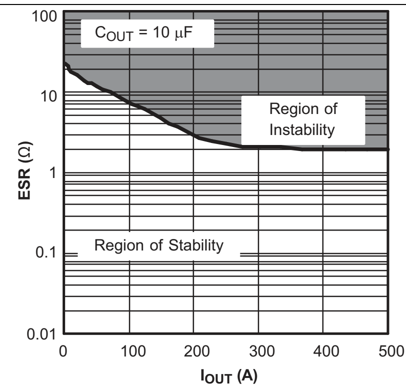


Figure 22. TPS79530 Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

7 Detailed Description

7.1 Overview

The TPS795 family of LDO regulators combines the high performance required of many RF and precision analog applications with low current consumption. High PSRR is provided by a high-gain, high-bandwidth error loop with good supply rejection at very low headroom (V_{IN} – V_{OUT}). A noise-reduction pin is provided to bypass noise generated by the band-gap reference and to improve PSRR, while a quick-start circuit quickly charges this capacitor at start-up. All versions have thermal and overcurrent protection, and are fully specified from –40°C to +125°C.

7.2 Functional Block Diagrams

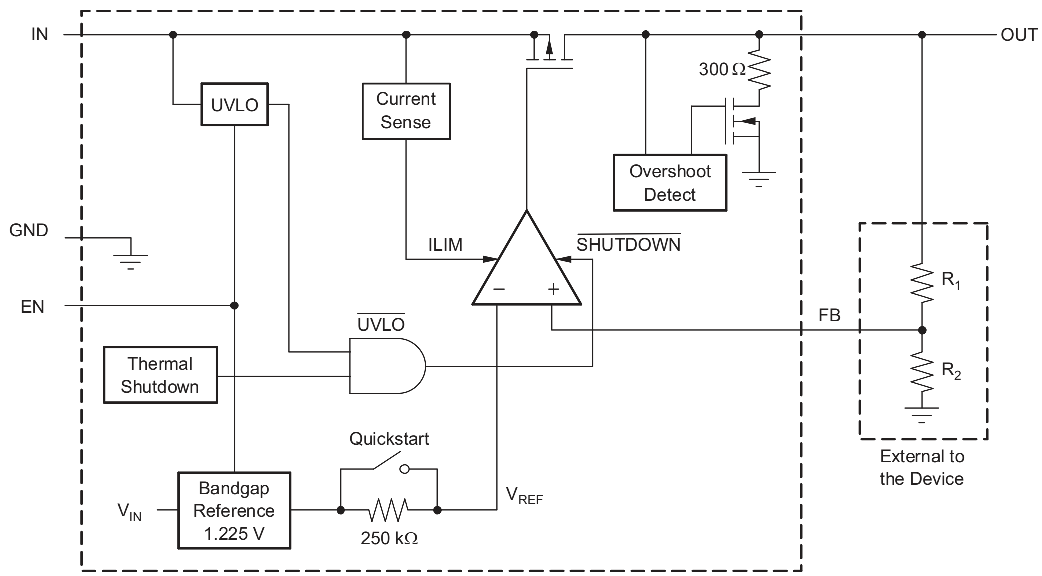


Figure 23. Functional Block Diagram—Adjustable Version

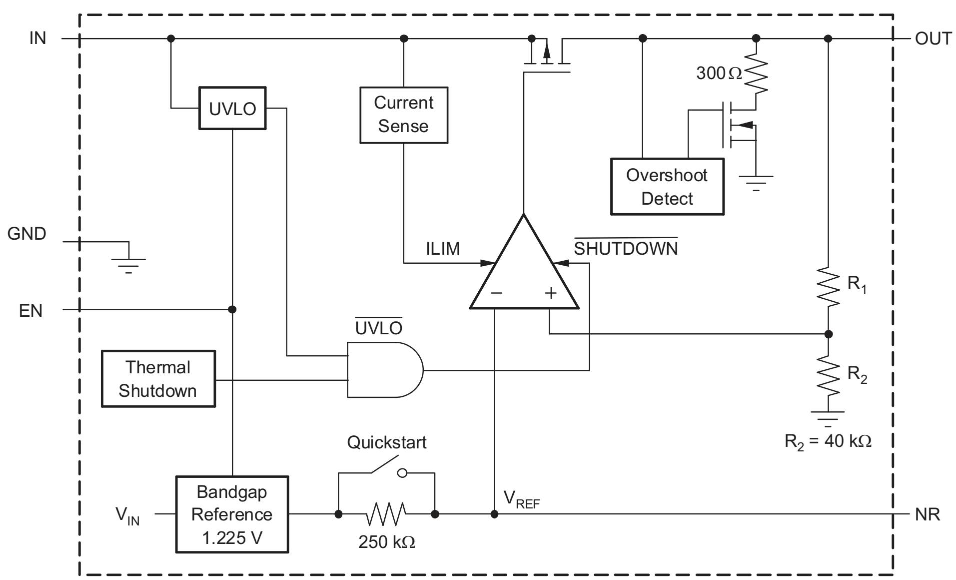


Figure 24. Functional Block Diagram—Fixed Versions

7.3 Feature Description

7.3.1 Shutdown

The enable pin (EN) is active high and is compatible with standard and low-voltage TTL-CMOS levels. When shutdown capability is not required, EN can be connected to IN.

7.3.2 Start-Up

The TPS795 uses a start-up circuit to quickly charge the noise reduction capacitor, C_{NR}, if present (see *Functional Block Diagrams*). This circuit allows for the combination of very low output noise and fast start-up times. The NR pin is high impedance so a low leakage C_{NR} capacitor must be used; most ceramic capacitors are appropriate for this configuration.

For the fastest start-up, apply V_{IN} first, and then drive the enable pin (EN) high. If EN is tied to IN, start-up is somewhat slower. To ensure that C_{NR} is fully charged during start-up, use a 0.1-µF or smaller capacitor.

7.3.3 Undervoltage Lockout (UVLO)

The TPS795 uses an undervoltage lockout circuit to keep the output shut off until internal circuitry is operating properly. The UVLO circuit has approximately 100 mV of hysteresis to help reject input voltage drops when the regulator first turns on.

7.3.4 Regulator Protection

The TPS795 PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS795 features internal current limiting and thermal protection. During normal operation, the TPS795 limits output current to approximately 2.8 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds approximately 165°C (T_{sd}), thermal-protection circuitry shuts it down. Once the device has cooled down to less than approximately 140°C, regulator operation resumes.

7.4 Device Functional Modes

Table 1 provides a quick comparison between the normal, dropout, and disabled modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	EN	I_{OUT}	T_J
Normal	$V_{IN} > V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{CL}$	$T_J < T_{sd}$
Dropout	$V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{CL}$	$T_J < T_{sd}$
Disabled	—	$V_{EN} < V_{EN(LO)}$	—	$T_J > T_{sd}$

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$).
- The enable voltage has previously exceeded the enable rising threshold voltage and not yet decreased below the enable falling threshold.
- The output current is less than the current limit ($I_{OUT} < I_{CL}$).
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{sd}$).

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass device is in the linear region and no longer controls the current through the LDO. Line or load transients in dropout can result in large output-voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature ($T_J > T_{sd}$).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS795 family of LDO regulators has been optimized for use in noise-sensitive equipment. The device features extremely low dropout voltages, high PSRR, ultralow output noise, low quiescent current (265 µA, typically), and an enable input to reduce supply currents to less than 1 µA when the regulator is turned off.

8.2 Typical Application

A typical application circuit is shown in Figure 25.

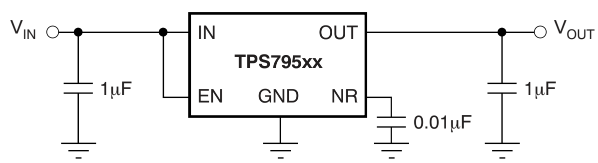


Figure 25. Typical Application Circuit

8.2.1 Design Requirements

Table 2 lists the design requirements.

Table 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	3.3 V
Output voltage	2.5 V
Maximum output current	500 mA

8.2.2 Detailed Design Procedure

Select the desired device based on the output voltage.

Provide an input supply with adequate headroom to account for dropout and output current to account for the GND terminal current, and power the load.

8.2.2.1 Input and Output Capacitor Requirements

Although not required, it is good analog design practice to place a 0.1-µF to 2.2-µF capacitor near the input of the regulator to counteract reactive input sources. A higher-value input capacitor may be necessary if large, fast-rise time load transients are anticipated and the device is located several inches from the power source.

Like most low dropout regulators, the TPS795 requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitor is 1 µF. Any 1-µF or larger ceramic capacitor is suitable.

8.2.2.2 Output Noise

The internal voltage reference is a key source of noise in an LDO regulator. The TPS795 has an NR pin which is connected to the voltage reference through a 250-kΩ internal resistor. The 250-kΩ internal resistor, in conjunction with an external bypass capacitor connected to the NR pin, creates a low-pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. For the regulator to operate properly, the current flow out of the NR pin must be at a minimum, because any leakage current creates an IR drop across the internal resistor, thus creating an output error. Therefore, the bypass capacitor must have minimal leakage current. The bypass capacitor should be no more than 0.1 µF to ensure that it is fully charged during the quickstart time provided by the internal switch shown in *Functional Block Diagrams*.

For example, the TPS79530 exhibits 40 μV_{RMS} of output voltage noise using a 0.1-µF ceramic bypass capacitor and a 10-µF ceramic output capacitor. The output starts up slower as the bypass capacitance increases due to the RC time constant at the bypass pin that is created by the internal 250-kΩ resistor and external capacitor.

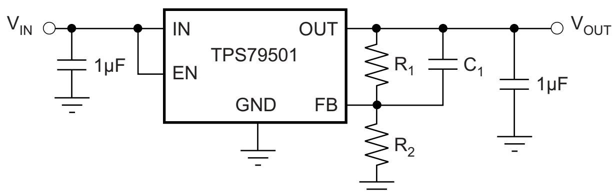
8.2.2.3 Dropout Voltage

The TPS795 uses a PMOS pass transistor to achieve a low dropout voltage. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in its linear region of operation and $r_{DS(on)}$ of the PMOS pass element is the input-to-output resistance. Because the PMOS device behaves like a resistor in dropout, V_{DO} approximately scales with the output current.

As with any linear regulator, PSRR degrades as (V_{IN} – V_{OUT}) approaches dropout. This effect is illustrated in Figure 9 through Figure 12.

8.2.2.4 Programming the TPS79501 Adjustable LDO Regulator

The output voltage of the TPS79501 adjustable regulator is programmed using an external resistor divider as shown in Figure 26.



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R_1	R_2	C_1
1.8 V	14.0 kΩ	30.1 kΩ	33 pF
3.6 V	57.9 kΩ	30.1 kΩ	15 pF

Figure 26. Typical Application, Adjustable Output

The output voltage is calculated using Equation 1.

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right)$$

where

- V_{REF} = 1.2246 V typical (the internal reference voltage) (1)

Resistors R_1 and R_2 should be chosen for approximately 40-µA divider current. Lower value resistors can be used for improved noise performance, but the device wastes more power. Higher values should be avoided, as leakage current at FB increases the output voltage error.

The recommended design procedure is to choose R_2 = 30.1 kΩ to set the divider current at 40 µA, C_1 = 15 pF for stability, and then calculate R_1 using Equation 2.

$$R_1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R_2 \quad (2)$$

To improve the stability of the adjustable version, TI suggests placing a small compensation capacitor between OUT and FB.

The approximate value of this capacitor can be calculated using Equation 3.

$$C_1 = \frac{\left(3 \times 10^{-7}\right) \times \left(R_1 + R_2\right)}{\left(R_1 \times R_2\right)} \quad (3)$$

The suggested value of this capacitor for several resistor ratios is shown in the table within Figure 26. If this capacitor is not used (such as in a unity-gain configuration), then the minimum recommended output capacitor is 2.2 µF instead of 1 µF.

8.2.3 Application Curves

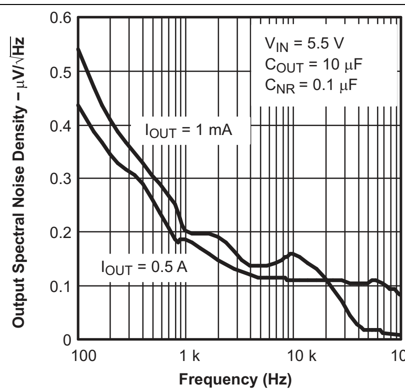


Figure 27. TPS79530 Output Spectral Noise Density vs Frequency

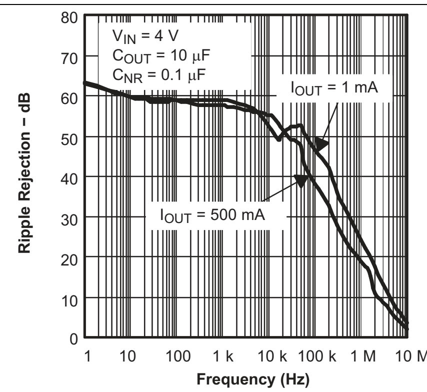


Figure 28. TPS79530 Ripple Rejection vs Frequency

8.3 What to Do and What Not to Do

Place at least one 1-µF ceramic capacitor as close as possible to the OUT pin of the regulator.

Do not place the output capacitor more than 10 mm away from the regulator.

Connect a 0.1-µF or larger, low equivalent series resistance (ESR) capacitor across the IN pin and GND input of the regulator.

Do not exceed the absolute maximum ratings.

9 Power Supply Recommendations

These devices are designed to operate from an input voltage supply range from 2.7 V to 5.5 V. The input voltage range provides adequate headroom for the device to have a regulated output. This input supply is well-regulated and stable. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

10.1.1 Board Layout Recommendation to Improve PSRR and Noise Performance

To improve ac measurements like PSRR, output noise, and transient response, TI recommends designing the board with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the ground pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the ground pin of the device.

10.1.2 Regulator Mounting

The tab of the 6-pin SOT-223 package is electrically connected to ground. For best thermal performance, solder the tab of the surface-mount version directly to a circuit-board copper area. Increasing the copper area improves heat dissipation.

Solder pad footprint recommendations for the devices are presented in application report SBFA015, *Solder Pad Recommendations for Surface-Mount Devices*, available from the TI website (www.ti.com).

10.1.3 Thermal Considerations

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the tab or pad is critical to avoiding thermal shutdown and ensuring reliable operation.

Power dissipation of the device depends on input voltage and load conditions and can be calculated using Equation 4:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{4}$$

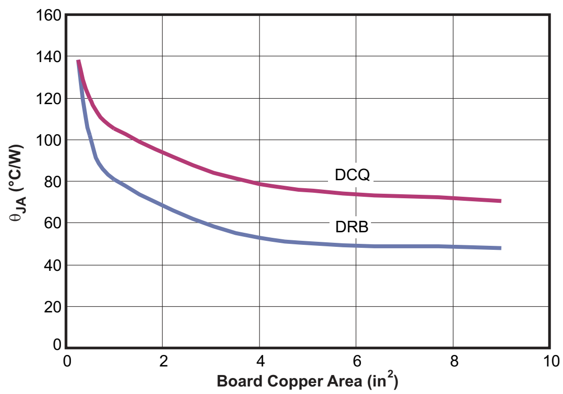
Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On the VSON (DRB) package, the primary conduction path for heat is through the exposed pad to the printed-circuit-board (PCB). The pad can be connected to ground or be left floating; however, it should be attached to an appropriate amount of copper PCB area to ensure the device does not overheat. On the SOT-223 (DCQ) package, the primary conduction path for heat is through the tab to the PCB. The tab should be connected to ground. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be calculated using Equation 5:

$$R_{\theta JA} = \frac{(+125°C - T_A)}{P_D} \tag{5}$$

Layout Guidelines (continued)

Knowing the maximum $R_{\theta JA}$, the minimum amount of PCB copper area needed for appropriate heatsinking can be estimated using Figure 29.



Note: θ_{JA} value at board size of 9 in.^{2} (that is, 3 in. × 3 in.) is a JEDEC standard.

Figure 29. Θ_{JA} vs Board Size

Figure 29 shows the variation of θ_{JA} as a function of ground plane copper area in the board. It is intended only as a guideline to demonstrate the effect of heat spreading in the ground plane and should not be used to estimate the thermal performance in real application environments.

NOTE

When the device is mounted on an application PCB, it is strongly recommended to use Ψ_{JT} and Ψ_{JB}, as explained in *Estimating Junction Temperature*.

10.1.4 Estimating Junction Temperature

Using the thermal metrics Ψ_{JT} and Ψ_{JB}, as shown in *Thermal Information*, the junction temperature can be estimated with corresponding formulas (given in Equation 6). For backwards compatibility, an older θ_{JC},*Top* parameter is also listed.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$

$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D$$

where

- P_D is the power dissipation shown by Equation 5
- T_T is the temperature at the center-top of the IC package
- T_B is the PCB temperature measured 1 mm away from the IC package *on the PCB surface* (see Figure 31) (6)

NOTE

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the application note SBVA025, *Using New Thermal Metrics*, available for download at www.ti.com.

Layout Guidelines (continued)

As shown in Figure 30, the new thermal metrics (Ψ_{JT} and Ψ_{JB}) have little dependency on board size. That is, using Ψ_{JT} or Ψ_{JB} with Equation 6 is a good way to estimate T_J by simply measuring T_T or T_B, regardless of the application board size.

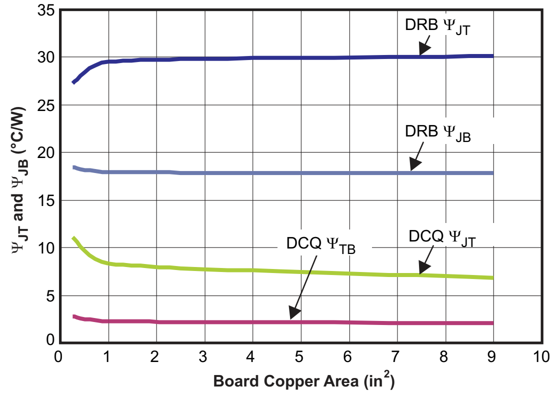


Figure 30. Ψ_{JT} and Ψ_{JB} vs Board Size

For a more detailed discussion of why TI does not recommend using $\theta_{JC(top)}$ to determine thermal characteristics, see the application report SBVA025, *Using New Thermal Metrics*, available at www.ti.com.

For further information, see the application report SPRA953, *IC Package Thermal Metrics*, also available on the TI website.

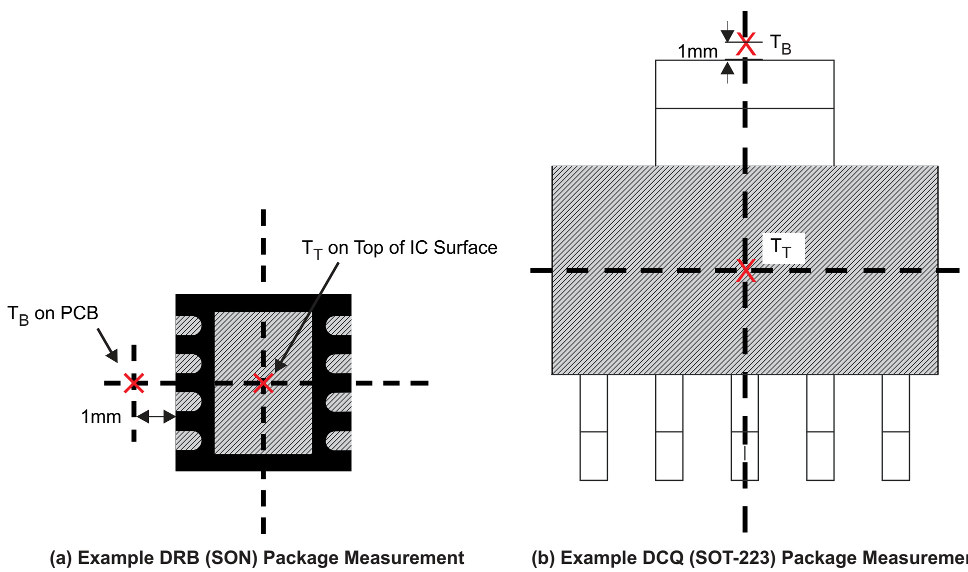


Figure 31. Measuring Point for T_T and T_B

10.2 Layout Examples

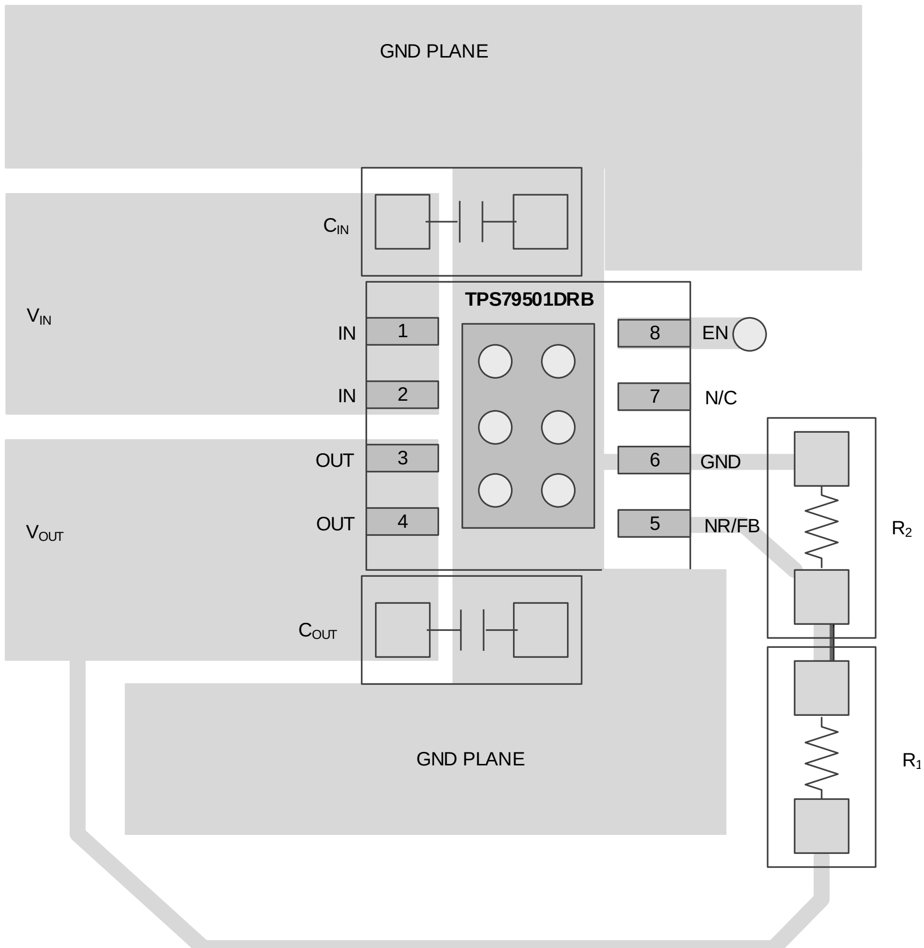


Figure 32. TPS79501 (Adjustable Voltage Version)—Layout Example

Layout Examples (continued)

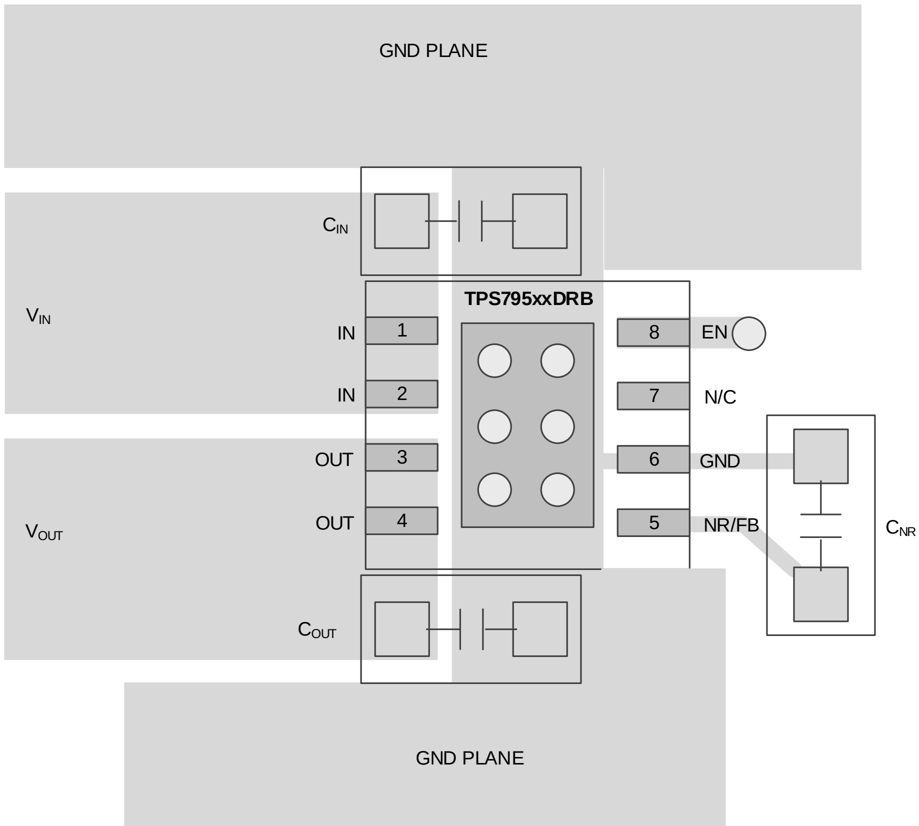


Figure 33. TPS795 (Fixed Voltage Versions)—Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS795. The TPS79501DRBEVM evaluation module related (and user's guide) can be requested at the TI website through the product folders or purchased directly from the TI eStore.

11.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS795 is available through the product folders under *Tools & Software*.

11.1.2 Device Nomenclature

Table 3. Device Nomenclature(1)

PRODUCT	V_{OUT}
TPS795**xx(x)** ***yyy z***	**xx(x)** is nominal output voltage (for example, 28 = 2.8 V, 285 = 2.85 V, 01 = adjustable). **yyy** is package designator. **z** is package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

11.2 Documentation Support

11.2.1 Related Documentation

- Texas Instruments, *Using New Thermal Metrics* application report
- Texas Instruments, *IC Package Thermal Metrics* application report
- Texas Instruments, *TPS78601/TPS79501/TPS79601DRB Evaluation Module* user's guide
- Texas Instruments, *Using New Thermal Metrics* application report

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS79501DCQ	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	PS79501	Samples
TPS79501DCQG4	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79501	Samples
TPS79501DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	PS79501	Samples
TPS79501DRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BUH	Samples
TPS79501DRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BUH	Samples
TPS79501DRBTG4	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BUH	Samples
TPS79516DCQ	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79516	Samples
TPS79516DCQR	LIFEBUY	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79516	
TPS79518DCQ	LIFEBUY	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79518	
TPS79518DCQG4	LIFEBUY	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79518	
TPS79518DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79518	Samples
TPS79525DCQ	LIFEBUY	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79525	
TPS79525DCQG4	LIFEBUY	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79525	
TPS79525DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79525	Samples
TPS79525DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79525	Samples
TPS79530DCQ	LIFEBUY	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79530	
TPS79530DCQR	LIFEBUY	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79530	
TPS79533DCQ	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	PS79533	Samples
TPS79533DCQG4	LIFEBUY	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79533	
TPS79533DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	PS79533	Samples
TPS79533DCQRG4	LIFEBUY	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79533	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

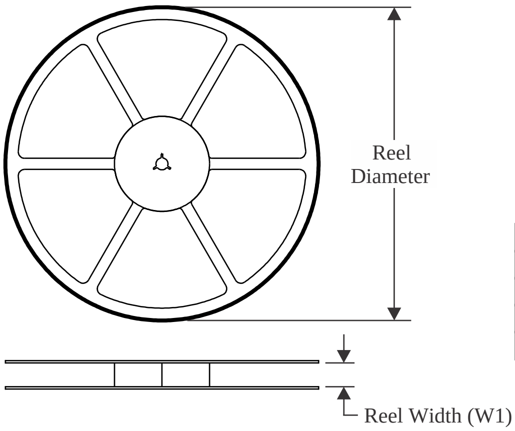
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

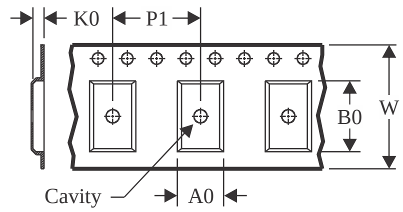
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

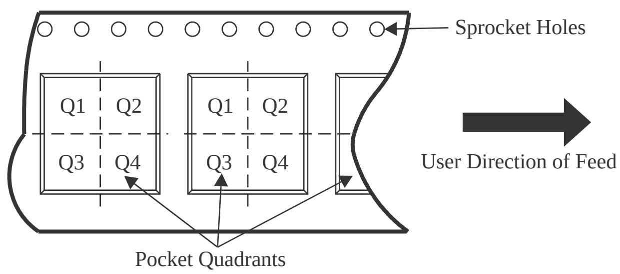


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

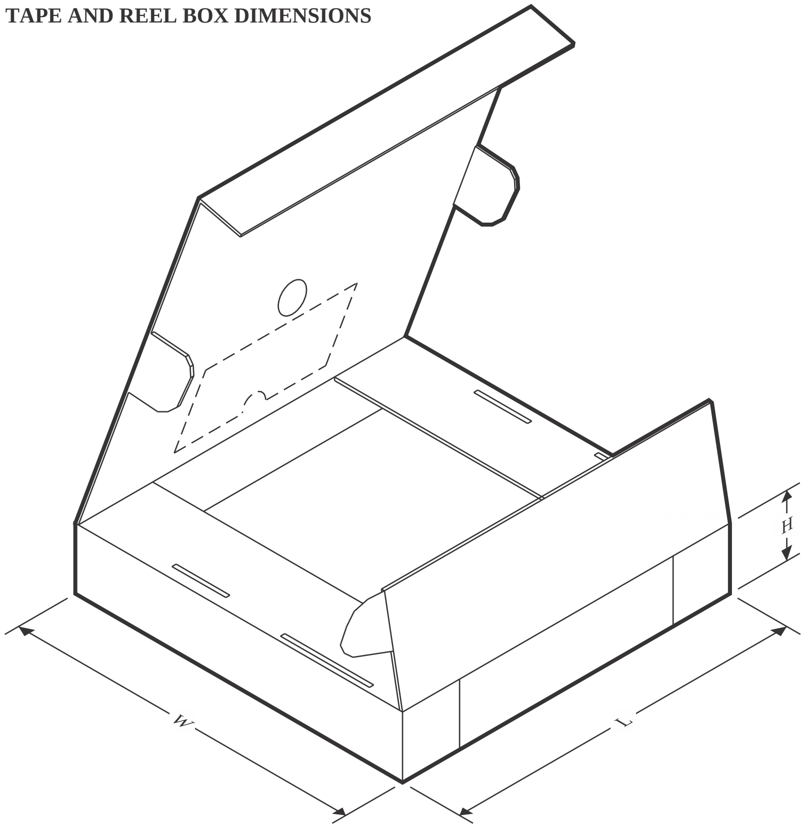
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79501DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.85	7.3	1.88	8.0	12.0	Q3
TPS79516DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS79530DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS79533DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.85	7.3	1.88	8.0	12.0	Q3
TPS79533DCQRG4	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3

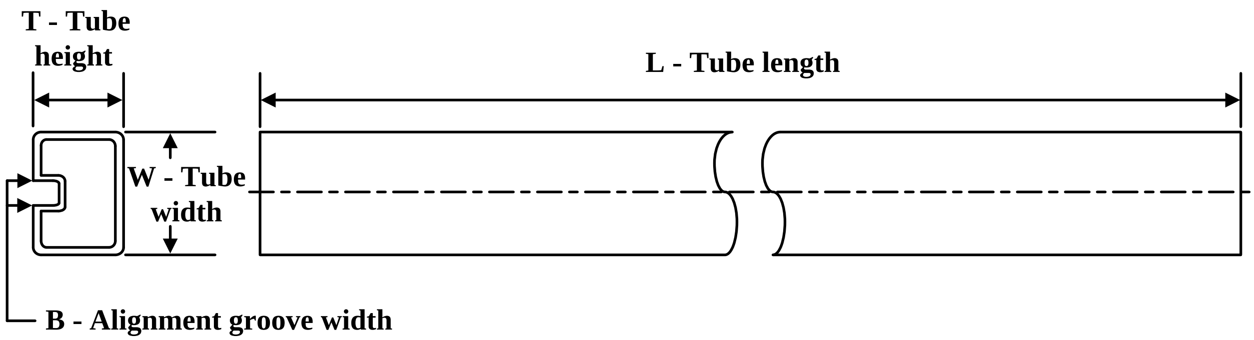
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

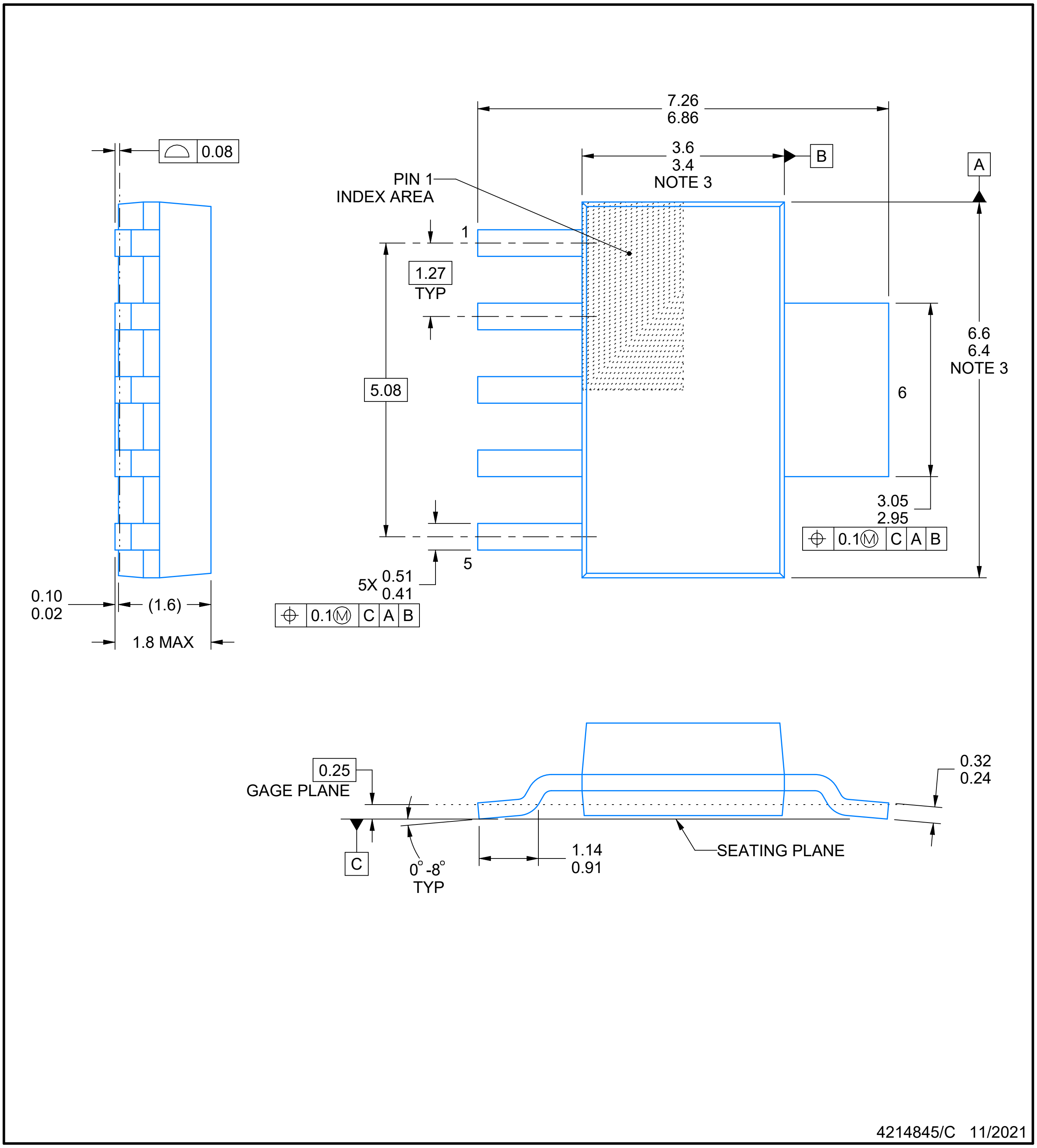
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79501DCQR	SOT-223	DCQ	6	2500	356.0	356.0	35.0
TPS79516DCQR	SOT-223	DCQ	6	2500	346.0	346.0	29.0
TPS79530DCQR	SOT-223	DCQ	6	2500	346.0	346.0	29.0
TPS79533DCQR	SOT-223	DCQ	6	2500	356.0	356.0	35.0
TPS79533DCQRG4	SOT-223	DCQ	6	2500	346.0	346.0	29.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS79501DCQ	DCQ	SOT-223	6	78	543	8.6	3606.8	2.67
TPS79501DCQG4	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
TPS79516DCQ	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
TPS79518DCQ	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
TPS79518DCQG4	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
TPS79525DCQ	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
TPS79525DCQG4	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
TPS79530DCQ	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
TPS79533DCQ	DCQ	SOT-223	6	78	543	8.6	3606.8	2.67
TPS79533DCQG4	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68



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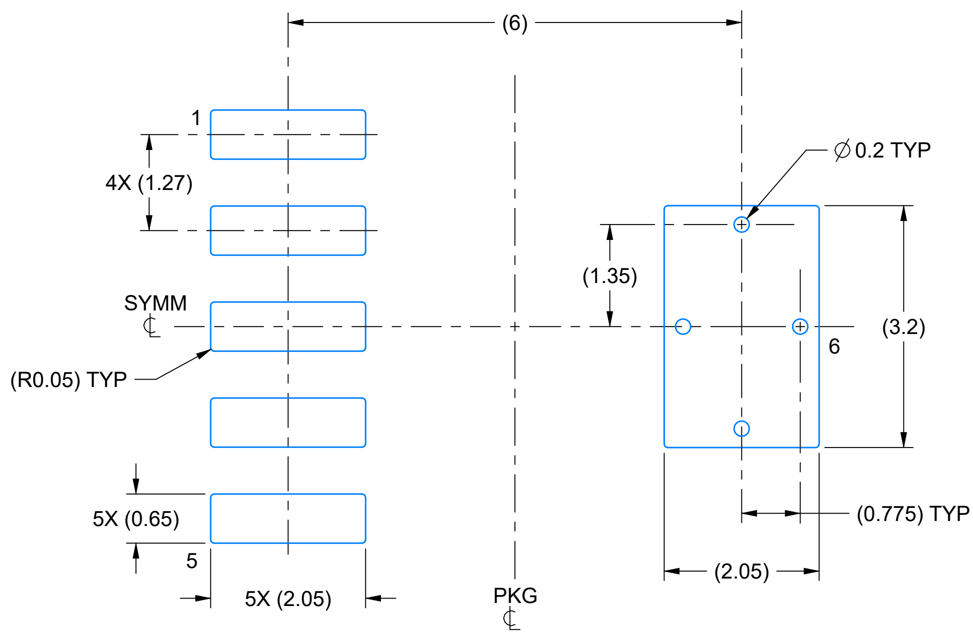
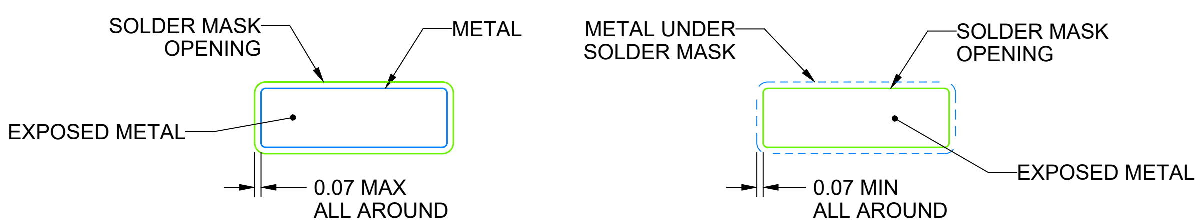
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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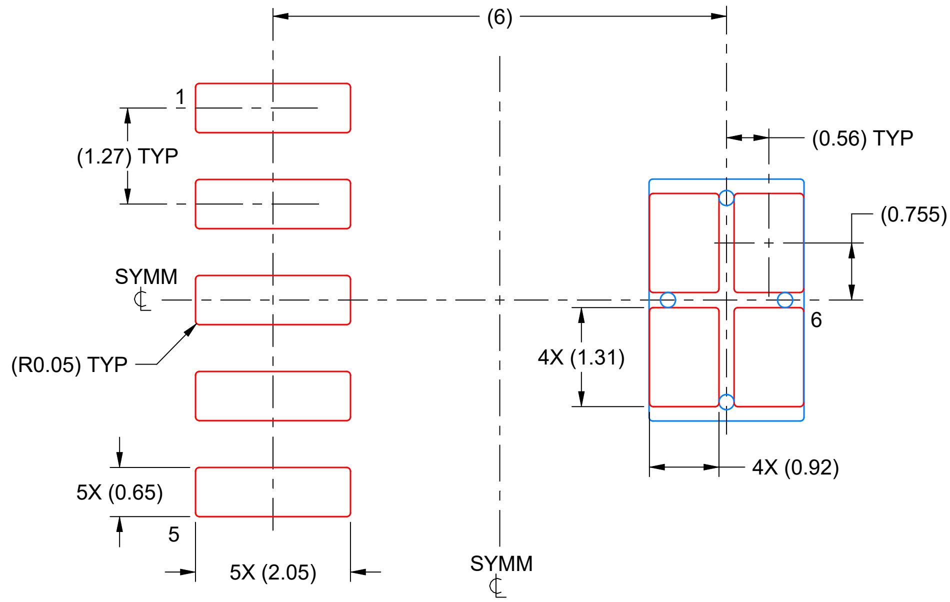
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214845/C 11/2021

NOTES: (continued)

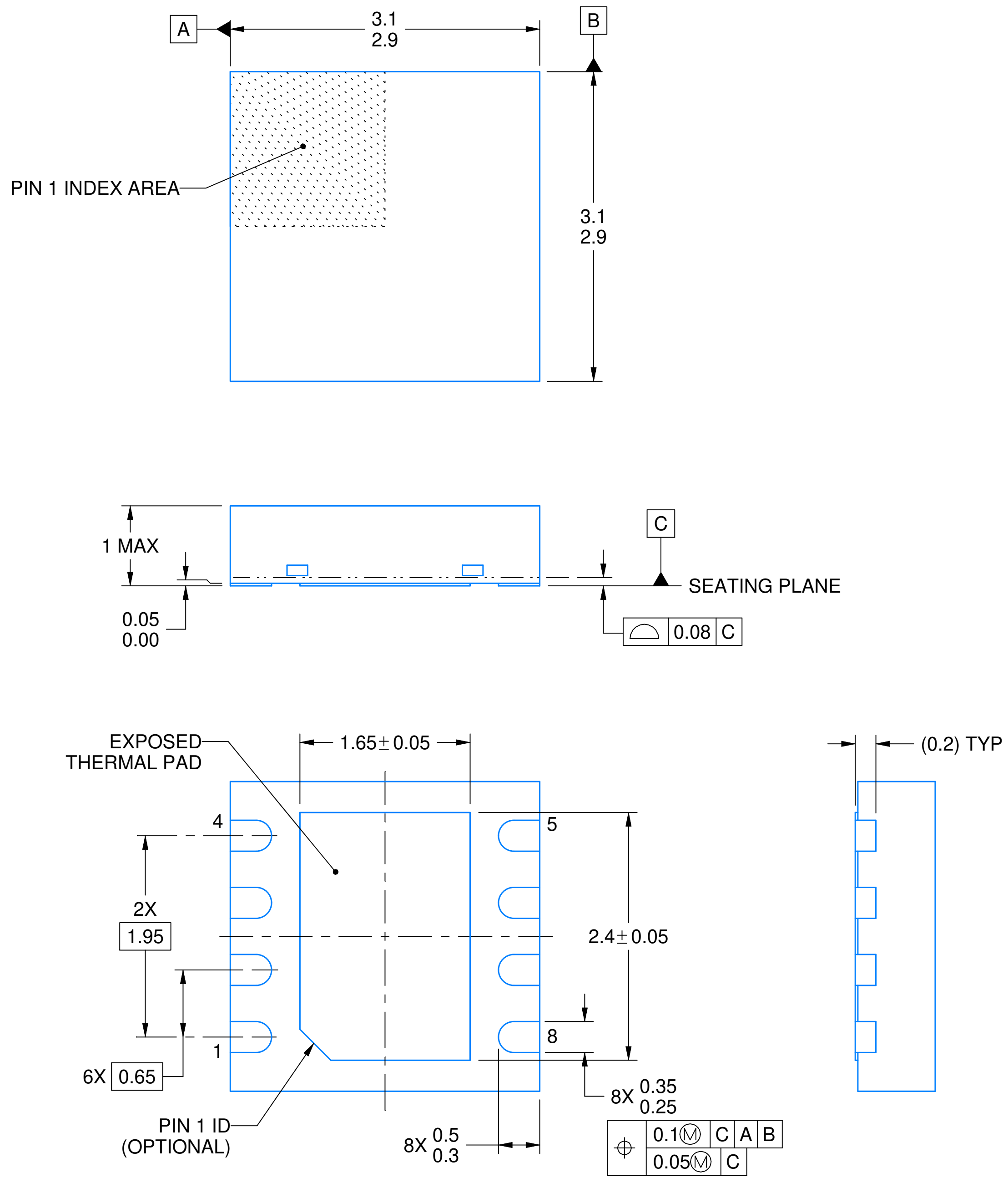
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DRB 8

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

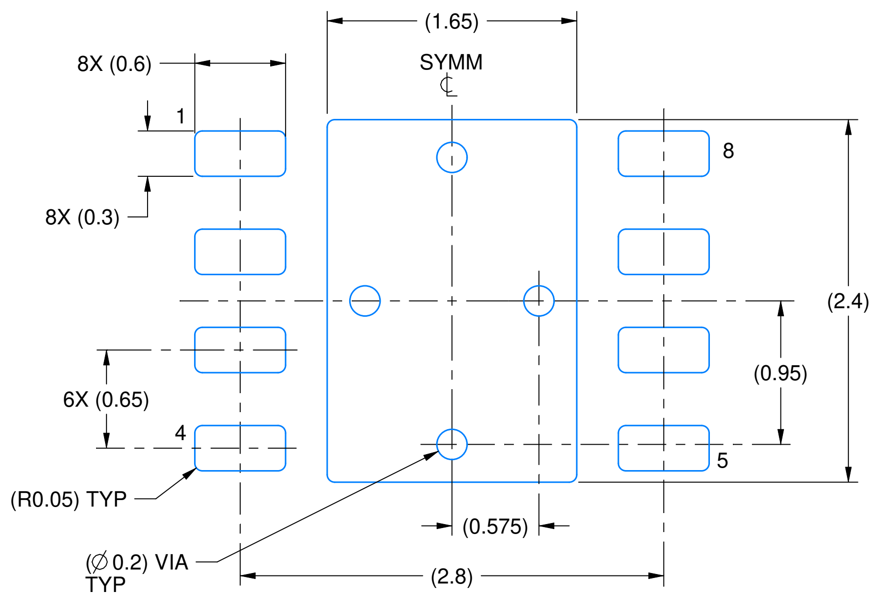
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



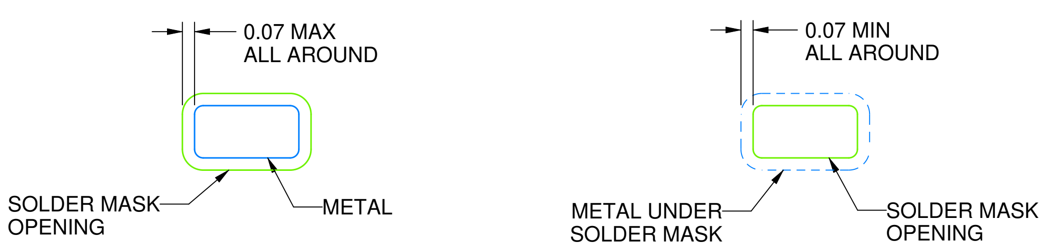
4218876/A 12/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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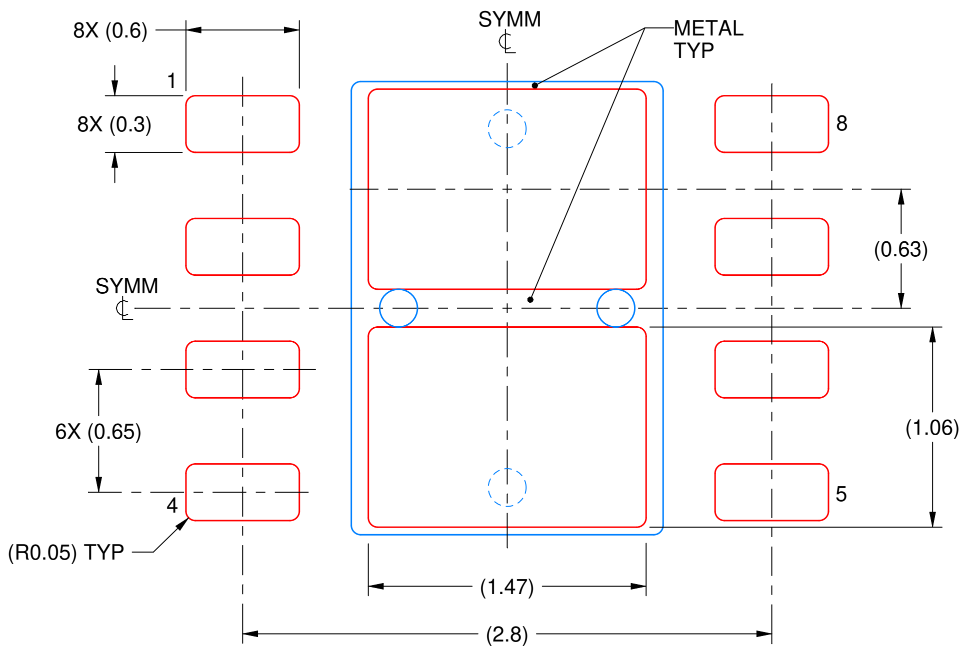
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.