BLS6G2731-120; BLS6G2731S-120

LDMOS S-band radar power transistor

Rev. 2 — 1 September 2015 | **Product data sheet**

1. Product profile

1.1 General description

120 W LDMOS power transistor intended for radar applications in the 2.7 GHz to 3.1 GHz range.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C; t_p = 100 μs; δ = 10 %; I_{Dq} = 100 mA; in a class-AB production test circuit.

Mode of operation	f (GHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	t_r (ns)	t_f (ns)
pulsed RF	2.7 to 3.1	32	120	13.5	48	20	6

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features

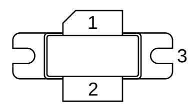
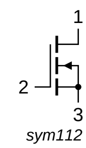
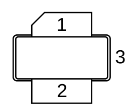
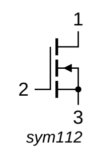
- Typical pulsed RF performance at a frequency of 2.7 GHz to 3.1 GHz, a supply voltage of 32 V, an I_{Dq} of 100 mA, a t_p of 100 μs with δ of 10 %:
  - Output power = 120 W
  - Power gain = 13.5 dB
  - Efficiency = 48 %
- Easy power control
- Integrated ESD protection
- High flexibility with respect to pulse formats
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (2.7 GHz to 3.1 GHz)
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding restriction of hazardous substances (RoHS)

1.3 Applications

- S-band power amplifiers for radar applications in the 2.7 GHz to 3.1 GHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLS6G2731-120 (SOT502A)			
1	drain		
2	gate		
3	source [1]		
BLS6G2731S-120 (SOT502B)			
1	drain		
2	gate		
3	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLS6G2731-120	-	flanged LDMOST ceramic package; 2 mounting holes; 2 leads	SOT502A
BLS6G2731S-120	-	earless flanged LDMOST ceramic package; 2 leads	SOT502B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Min	Max	Unit
V_{DS}	drain-source voltage	-	60	V
V_{GS}	gate-source voltage	−0.5	+13	V
I_D	drain current	-	33	A
T_{stg}	storage temperature	−65	+150	°C
T_j	junction temperature	-	225	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$Z_{th(j-mb)}$	transient thermal impedance from junction to mounting base	T_{case} = 85 °C; P_L = 120 W		
		t_p = 100 μs; δ = 10 %	0.23	K/W
		t_p = 200 μs; δ = 10 %	0.28	K/W
		t_p = 300 μs; δ = 10 %	0.32	K/W
		t_p = 100 μs; δ = 20 %	0.33	K/W

6. Characteristics

Table 6. Characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.6 mA	60	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 180 mA	1.4	1.8	2.4	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	4.2	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	27	33	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	450	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 9 A	8.1	13	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 6.3 A	-	0.085	0.135	Ω

7. Application information

Table 7. Application information

Mode of operation: pulsed RF; t_p = 100 μs; δ = 10 %; RF performance at V_{DS} = 32 V; I_{Dq} = 100 mA; T_{case} = 25 °C; unless otherwise specified, in a class-AB production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_L	output power		-	120	-	W
V_{CC}	supply voltage	P_L = 120 W	-	-	32	V
G_p	power gain	P_L = 120 W	12	13.5	-	dB
RL_{in}	input return loss	P_L = 120 W	-	7	-	dB
$P_{L(1dB)}$	output power at 1 dB gain compression		-	130	-	W
η_D	drain efficiency	P_L = 120 W	40	48	-	%
$P_{droop(pulse)}$	pulse droop power	P_L = 120 W	-	0	0.5	dB
t_r	rise time	P_L = 120 W	-	20	50	ns
t_f	fall time	P_L = 120 W	-	6	50	ns

Table 8. Typical impedance

f GHz	Z_S Ω	Z_L Ω
2.7	3.4 – j7.2	4.6 – j4.4
2.8	3.8 – j5.9	3.8 – j4.6
2.9	4.7 – j4.8	3.0 – j4.6
3.0	6.3 – j4.1	2.3 – j4.3
3.1	8.8 – j4.9	1.8 – j3.9

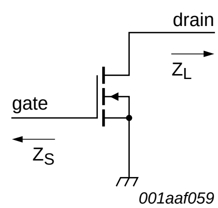
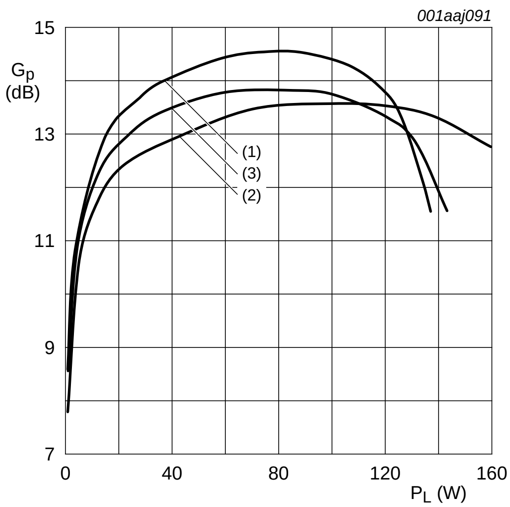


Fig 1. Definition of transistor impedance

7.1 Ruggedness in class-AB operation

The BLS6G2731-120 and BLS6G2731S-120 are capable of withstanding a load mismatch corresponding to VSWR = 5 : 1 through all phases under the following conditions: V_{DS} = 32 V; I_{Dq} = 100 mA; P_L = 120 W; t_p = 100 μs; δ = 10 %.

7.2 Graphs



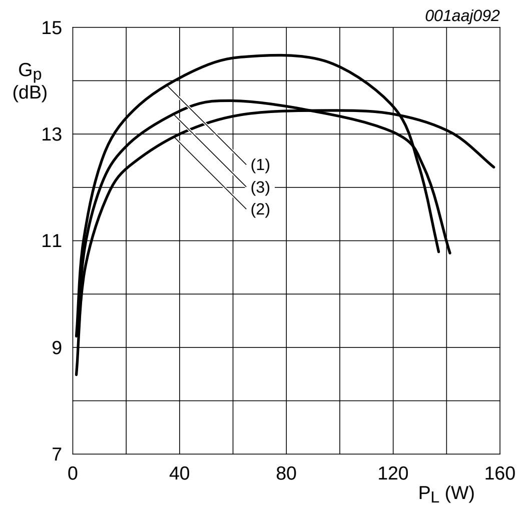
V_{DS} = 32 V; I_{Dq} = 100 mA; t_p = 300 μs; δ = 10 %.

(1) f = 2.7 GHz

(2) f = 2.9 GHz

(3) f = 3.1 GHz

Fig 2. Power gain as a function of load power; typical values



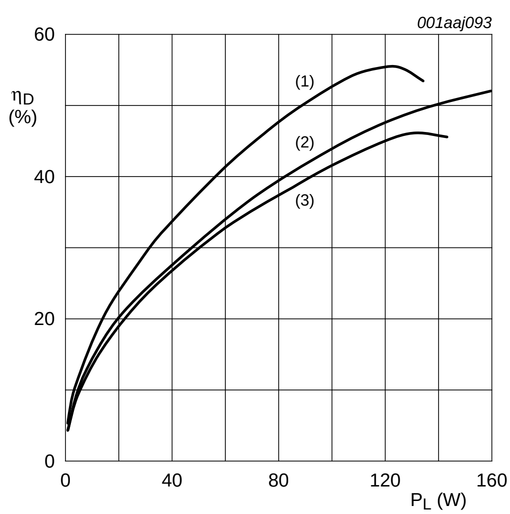
V_{DS} = 32 V; I_{Dq} = 100 mA; t_p = 100 μs; δ = 20 %.

(1) f = 2.7 GHz

(2) f = 2.9 GHz

(3) f = 3.1 GHz

Fig 3. Power gain as a function of load power; typical values



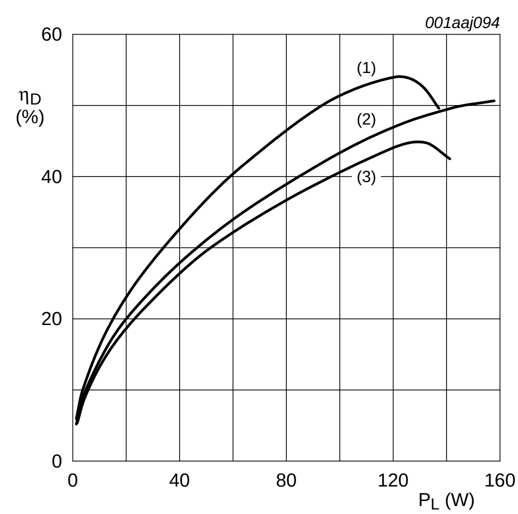
V_{DS} = 32 V; I_{Dq} = 100 mA; t_p = 300 μs; δ = 10 %.

(1) f = 2.7 GHz

(2) f = 2.9 GHz

(3) f = 3.1 GHz

Fig 4. Drain efficiency as a function of load power; typical values



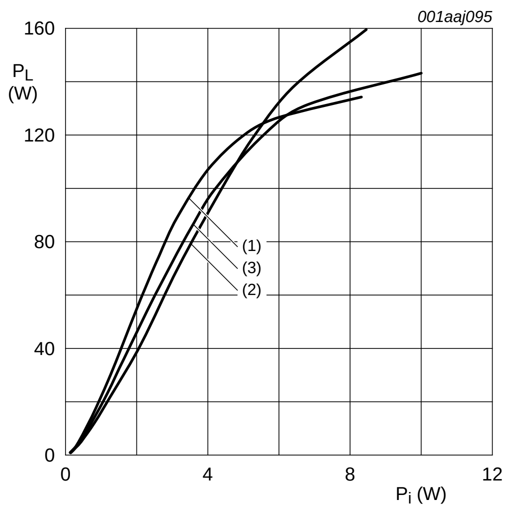
V_{DS} = 32 V; I_{Dq} = 100 mA; t_p = 100 μs; δ = 20 %.

(1) f = 2.7 GHz

(2) f = 2.9 GHz

(3) f = 3.1 GHz

Fig 5. Drain efficiency as a function of load power; typical values



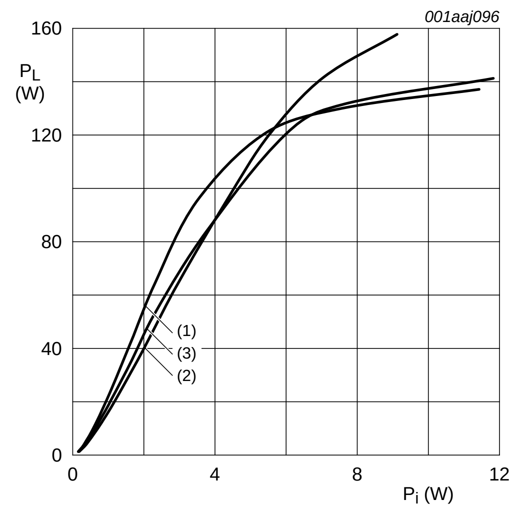
V_{DS} = 32 V; I_{Dq} = 100 mA; t_p = 300 μs; δ = 10 %.

(1) f = 2.7 GHz

(2) f = 2.9 GHz

(3) f = 3.1 GHz

Fig 6. Load power as a function of input power; typical values



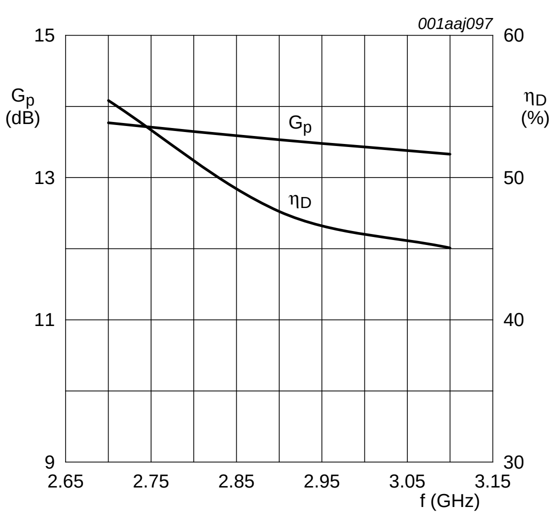
V_{DS} = 32 V; I_{Dq} = 100 mA; t_p = 100 μs; δ = 20 %.

(1) f = 2.7 GHz

(2) f = 2.9 GHz

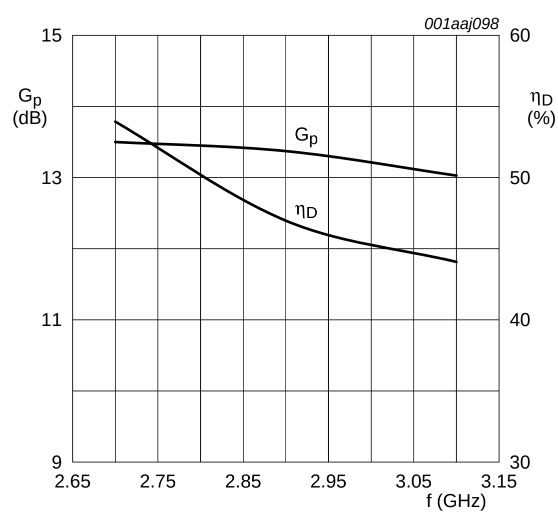
(3) f = 3.1 GHz

Fig 7. Load power as a function of input power; typical values



P_L = 120 W; V_{DS} = 32 V; I_{Dq} = 100 mA; t_p = 300 μs; δ = 10 %.

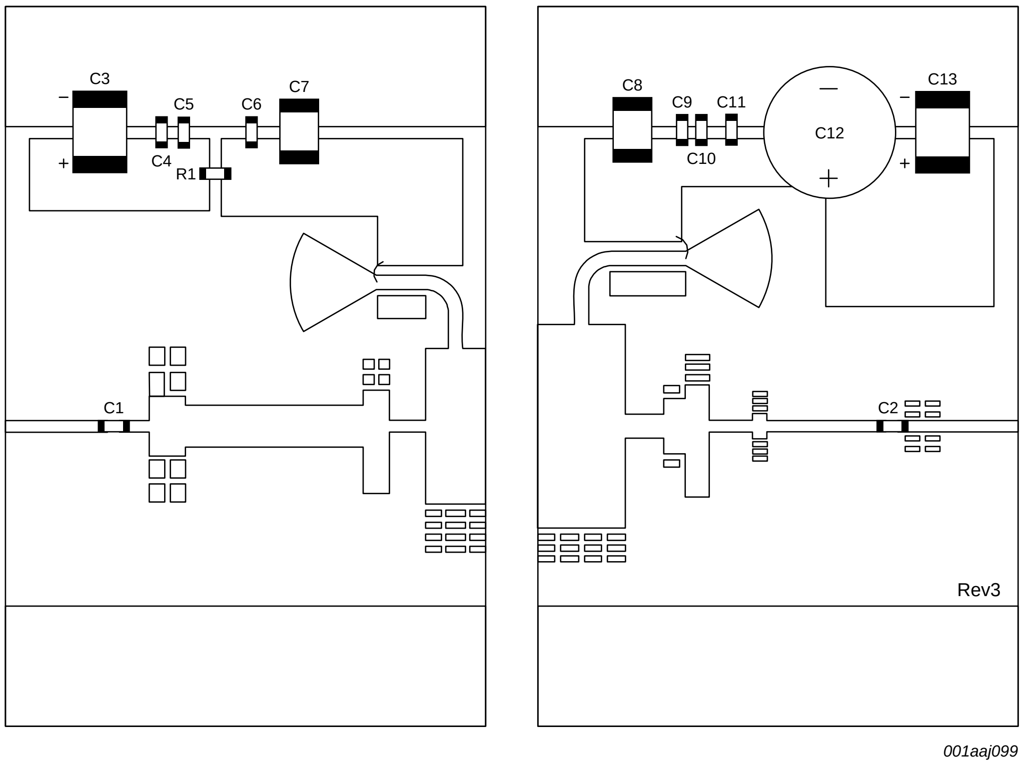
Fig 8. Power gain and drain efficiency as function of frequency; typical values



P_L = 120 W; V_{DS} = 32 V; I_{Dq} = 100 mA; t_p = 100 μs; δ = 20 %.

Fig 9. Power gain and drain efficiency as function of frequency; typical values

8. Test information



Striplines are on a double copper-clad Duroid 6006 Printed-Circuit Board (PCB) with ε_r = 6.15 and thickness = 0.64 mm.

See Table 9 for list of components.

Fig 10. Component layout for 2700 MHz to 3100 MHz test circuit

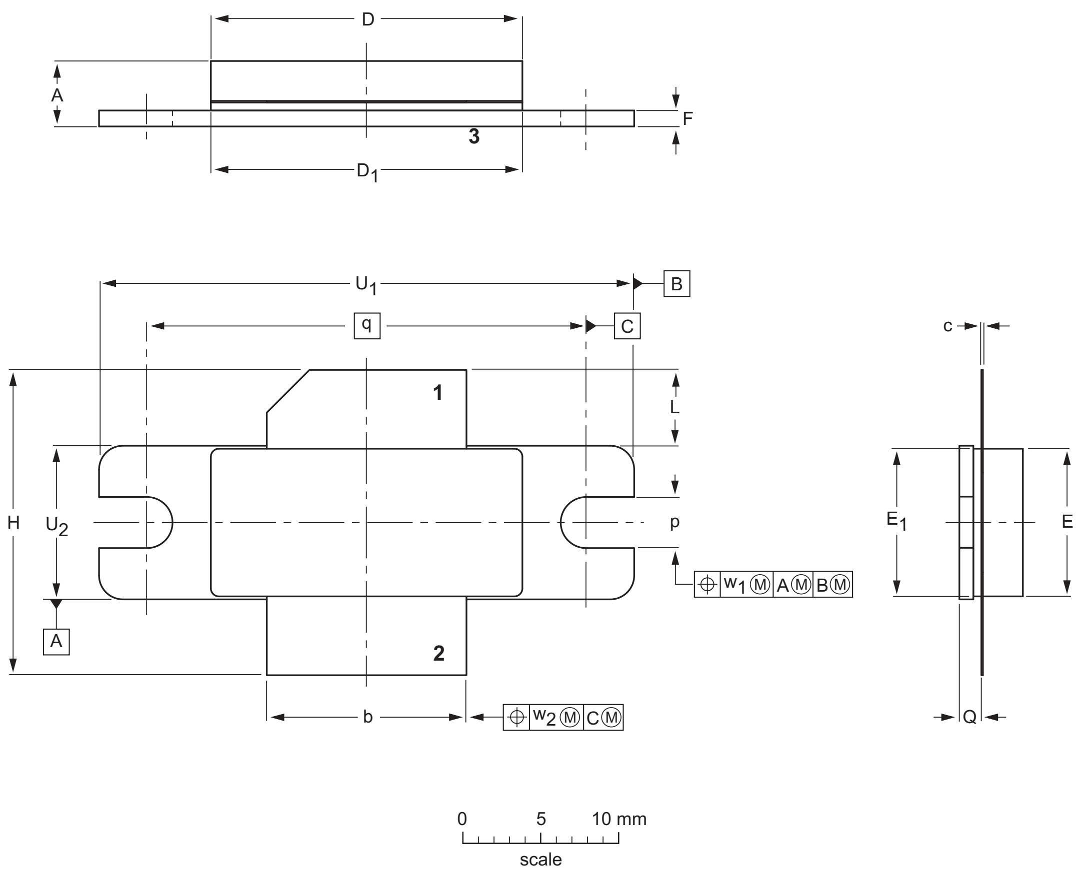
Table 9. List of components

See Figure 10.

Component	Description	Value	Remarks
C1, C2	multilayer ceramic chip capacitor	24 pF	ATC 100A or equivalent
C3	multilayer ceramic chip capacitor	47 μF; 20 V	
C4, C6, C9, C10	multilayer ceramic chip capacitor	33 pF	ATC 100A or equivalent
C5, C11	multilayer ceramic chip capacitor	1 nF	ATC 100A or equivalent
C7, C8	multilayer ceramic chip capacitor	100 pF	ATC 100B or equivalent
C12	electrolytic capacitor	47 μF; 63 V	
C13	multilayer ceramic chip capacitor	10 μF; 35 V	
R1	SMD resistor	56 Ω	SMD 0603

9. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads **SOT502A**



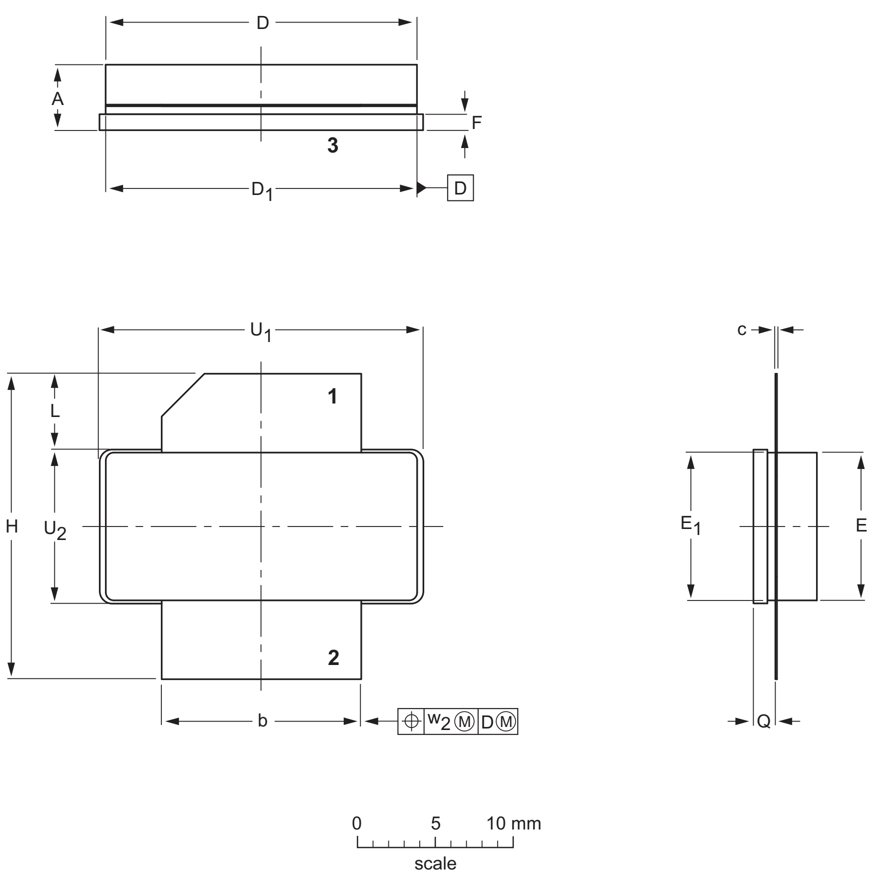
DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	w_1	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502A						~~03-01-10~~ 12-05-02

Fig 11. Package outline SOT502A

Earless flanged ceramic package; 2 leads **SOT502B**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502B						~~07-05-09~~ 12-05-02

Fig 12. Package outline SOT502B

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
RF	Radio Frequency
S-band	Short wave Band
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLS6G2731-120_6G2731S-120#2	20150901	Product data sheet		BLS6G2731-120_6G2731S-120 #1
Modifications:	• The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. • Legal texts have been adapted to the new company name where appropriate.			
BLS6G2731-120_6G2731S-120#1	20081114	Product data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

1	**Product profile**	**1**
1.1	General description	1
1.2	Features	1
1.3	Applications	2
2	**Pinning information**	**2**
3	**Ordering information**	**2**
4	**Limiting values**	**2**
5	**Thermal characteristics**	**3**
6	**Characteristics**	**3**
7	**Application information**	**3**
7.1	Ruggedness in class-AB operation	4
7.2	Graphs	5
8	**Test information**	**7**
9	**Package outline**	**8**
10	**Abbreviations**	**10**
11	**Revision history**	**10**
12	**Legal information**	**11**
12.1	Data sheet status	11
12.2	Definitions	11
12.3	Disclaimers	11
12.4	Trademarks	11
13	**Contact information**	**11**
14	**Contents**	**12**

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