UNITRODE

DV2004L1

Fast Charge Development System

Control of PNP Power Transistor

Features

- bq2004 fast-charge control evaluation and development
- Charge current sourced from an on-board frequency-modulated linear regulator (up to 3.0A)
- Fast charge of 4 to 10 NiCd or NiMH cells and one user-defined selection
- Fast-charge termination by delta temperature/delta time ($\Delta T/\Delta t$), negative delta voltage ($-\Delta V$) or peak voltage detect, maximum temperature, maximum time, and maximum voltage
- $-\Delta V$/peak voltage detect, hold-off, top-off, maximum time, and number of cells are jumper-configurable
- Programmable charge status display
- Discharge-before-charge control with push-button switch or auto discharge-before-charge with jumper
- Inhibit fast charge by logic-level input

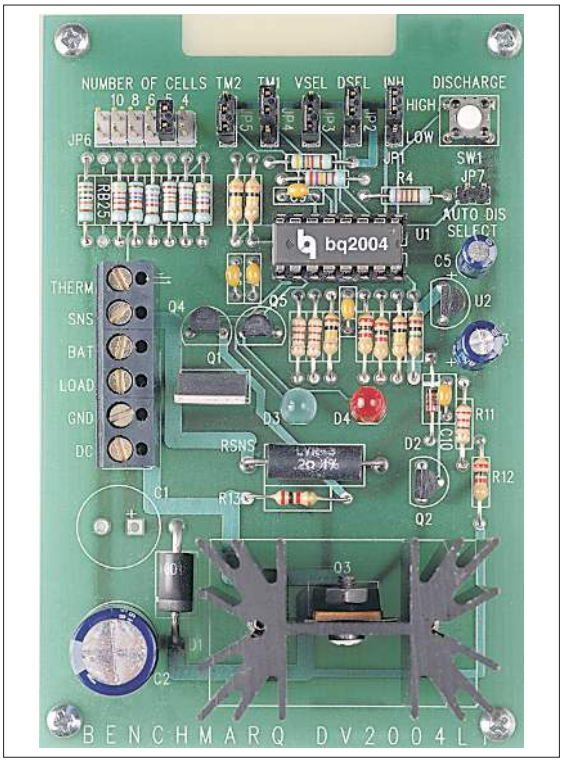
General Description

The DV2004L1 Development System provides a development environment for the bq2004 Fast-Charge IC. The DV2004L1 incorporates a bq2004 and a frequency-modulated linear regulator to provide fast charge control for 4 to 10 NiCd or NiMH cells.

The fast charge is terminated by any of the following: $\Delta T/\Delta t$, $-\Delta V$ or peak voltage detect, maximum temperature, maximum time, maximum voltage, or an inhibit command. Jumper settings select the voltage termination mode, the hold-off, top-off, and maximum time limits, and automatic discharge-before-charge.

The user provides a power supply and batteries. The user configures the DV2004L1 for the number of cells, voltage, charge termination mode, and maximum charge time (with or without top-off), and commands the discharge-before-charge option with the push-button switch S1.

Please review the bq2004 data sheet before using the DV2004L1 board.



Connection Descriptions

J1

	THERM	Thermistor connection
	SNS	Negative battery terminal and thermistor connection
	BAT	Positive battery terminal and high side of discharge load
	LOAD	Low side of discharge load
	GND	Ground from charger supply
	DC	DC input from charger supply
JP1	$\overline{INH}$	Inhibit input

JP2 DSEL	Display select
JP3 VSEL	Voltage termination select
JP4 TM1	TM1 setting
JP5 TM2	TM2 setting
JP6 NOC	Select number of cells
JP7	Auto discharge-before-charge select

Fixed Configuration

The DV2004L1 board has the following fixed characteristics :

- V_{CC} (4.75–5.25V) is regulated on-board from the supply at connector J1 (DC: GND).
- LEDs indicate charge status.
- Charge initiates on the later application of the battery or DC, which provides V_{CC} to the bq2004.

Pin DCMD may be tied to ground through JP7 for automatic discharge-before-charge. With JP7 open, a toggle of switch S1 momentarily pulls DCMD low and initiates a discharge-before-charge. The bq2004 output activates FET Q1, allowing current to flow through an external current-limiting load between BAT and LOAD on connector J1.

As shipped from Benchmarq, the DV2004L1 frequency-modulated linear regulator is configured to a charging current of 1.13A. This current level is controlled by the value of sense resistor R_{SNS} by the relationship:

$$I_{CHG} = \frac{0.225V}{R_{SNS}}$$

The value of R_{SNS} at shipment is 0.200Ω. This resistor can be changed depending on the application.

The suggested maximum I_{CHG} for the DV2004L1 board is 3A. ***Q4 must be mounted to an appropriate heat sink.***

The maximum cell voltage (MCV) is scaled to 1.8V/cell.

Note: Use the bqCharge diskette to calculate the RB1/RB2 resistors to adjust MCV.

With the provided NTC thermistor connected between THERM and SNS, values are: LTF = 10°C, HTF = 49°C, and TCO = 50°C. The $\Delta T/\Delta t$ settings at 30°C ($T_{\Delta T}$) are: minimum = 0.82°C/minute, typical = 1.10°C/minute.

The thermistor is identified by the serial number suffix as follows:

Identifier	Thermistor
K1	Keystone RL0703-5744-103-S1
(blank)	Philips 2322-640-63103
F1	Fenwal Type 16, 197-103LA6-A01
O1	Ozhumi 150-108-00(4)
S1	Semetic 103AT-2

Jumper-Selectable Configuration

The DV2004L1 must be configured as described below.

INH (JP1): Enables/disables charge inhibit (see bq2004 data sheet).

Jumper Setting	Pin State
[1 2] 3	Disabled (high)
1 [2 3]	Enabled (low)

TM1 and TM2 (JP4 and JP5): Select fast charge safety time/hold-off/top-off (see bq2004 data sheet).

Jumper Setting	Pin State
[1 2] 3	High
1 [2 3]	Low
1 2 3	Float

Number of Cells (JP6): A resistor-divider network is provided to select 4 to 10 cells (the resulting resistor

Closed Jumper	Number of Cells
RB25	User-selectable
RB24	10
RB23	8
RB22	6
RB21	5

value equals $N/2 - 1$ cells). RB1 is a 150KΩ resistor, and RB2 (RB20–RB25) is jumper-selected.

Temperature Disable: Connecting a 10KΩ resistor between THERM and SNS disables temperature control.

DSEL (JP2): Selects LED1 and LED2 display state (see bq2004 data sheet, Table 2).

VSEL (JP3): Selects -ΔV or peak-voltage detection, or disables voltage-based termination (see bq2004 data sheet).

AUTO DIS SELECT (JP7): Jumping JP7 enables automatic discharge-before-charge.

Setup Procedure

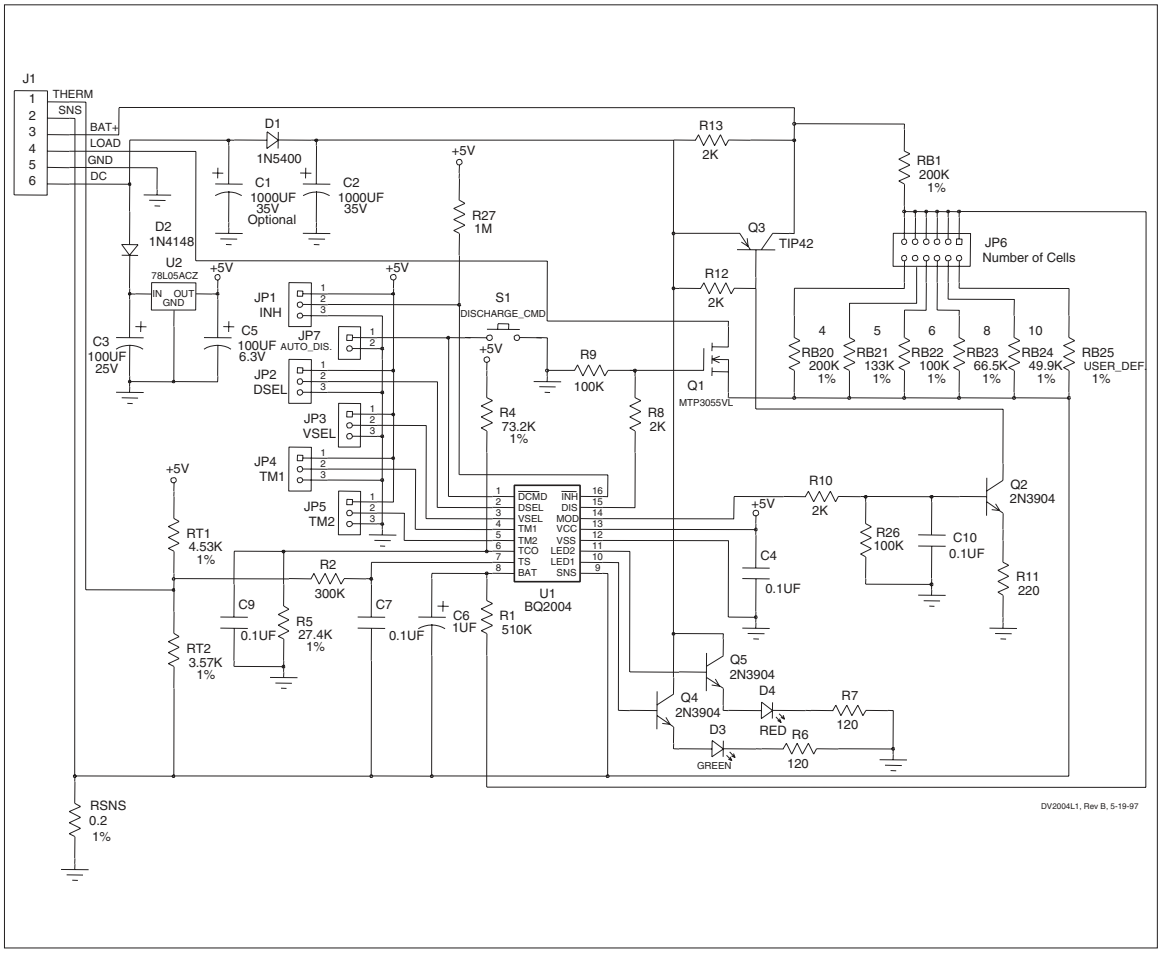
1. Configure VSEL, TM1, TM2, DSEL, INH, and number-of-cells (NOC) jumpers.
2. Connect the provided thermistor or a 10KΩ resistor between THERM and SNS.
3. If using the discharge-before-charge option, connect a current-limiting discharge load between BAT and LOAD.
4. Attach the battery pack to BAT and SNS. For temperature control, the thermistor must contact the cells.
5. Attach DC current source to DC (+) and GND (-) connections in J1. (Note: Capacitors C2 and C3 must be changed from those shipped with the board for input voltage in excess of 25V.)

Recommended DC Operating Conditions

Symbol	Description	Minimum	Typical	Maximum	Unit	Notes
I_{DC}	Maximum input current	-	-	3	A	
V_{DC}	Maximum input voltage	2.0 + V_{BAT} or 8.5	-	18 + V_{BAT} or 35	V	Note 1
V_{BAT}	BAT input voltage	-	-	24	V	
V_{THERM}	THERM input voltage	0	-	5	V	
I_{DSCHG}	Discharge load current	-	-	2	A	

Note: 1. The voltage at R14 is application-specific and limits the dissipation of Q2 to a safe limit during Q4 conduction. See Table 1 for recommended R14 selections per V_{DC+} and I_{CHARGE}.

DV2004L1 Board Schematic



Rev. B Board

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