Freescale Semiconductor
Technical Data

Document Number: MRF5S9101
Rev. 3, 5/2006

Replaced by MRF5S9101NR1/NBR1. There are no form, fit or function changes with this part replacement. N suffix added to part number to indicate transition to lead-free terminations.

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

Designed for GSM and GSM EDGE base station applications with frequencies from 869 to 960 MHz. Suitable for multicarrier amplifier applications.

GSM Application

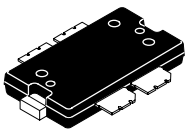
- Typical GSM Performance: V_{DD} = 26 Volts, I_{DQ} = 700 mA, P_{out} = 100 Watts CW, Full Frequency Band (869-894 MHz and 921-960 MHz)
  Power Gain - 17.5 dB
  Drain Efficiency - 60%

GSM EDGE Application

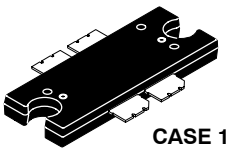
- Typical GSM EDGE Performance: V_{DD} = 28 Volts, I_{DQ} = 650 mA, P_{out} = 50 Watts Avg., Full Frequency Band (869-894 MHz and 921-960 MHz)
  Power Gain — 18 dB
  Spectral Regrowth @ 400 kHz Offset = -63 dBc
  Spectral Regrowth @ 600 kHz Offset = -78 dBc
  EVM — 2.3% rms
- Capable of Handling 10:1 VSWR, @ 26 Vdc, @ 100 W CW Output Power, @ f = 960 MHz
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Matched for Ease of Use
- Qualified Up to a Maximum of 32 V_{DD} Operation
- Integrated ESD Protection
- 200°C Capable Plastic Package
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel.

MRF5S9101MR1
MRF5S9101MBR1

869-960 MHz, 100 W, 26 V
GSM/GSM EDGE
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 1486-03, STYLE 1
TO-270 WB-4
PLASTIC
MRF5S9101MR1



CASE 1484-04, STYLE 1
TO-272 WB-4
PLASTIC
MRF5S9101MBR1

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +68	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	427 2.44	W W/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature	T_J	200	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (1,2)	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 100 W CW Case Temperature 80°C, 50 W CW	$R_{\theta JC}$	 0.41 0.47	°C/W

1. MTTF calculator available at http://www.freescale.com/rf. Select Tools/Software/Application Software/Calculators to access the MTTF calculators by product.
2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

NOTE - **CAUTION** - MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ARCHIVE INFORMATION

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1C (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Zero Gate Voltage Drain Leakage Current (V_{DS} = 68 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 26 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 400 μAdc)	$V_{GS(th)}$	2	2.8	3.5	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 700 mAdc)	$V_{GS(Q)}$	—	3.7	—	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 2 Adc)	$V_{DS(on)}$	—	0.21	0.3	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 6 Adc)	g_{fs}	—	7	—	S
Dynamic Characteristics (1)					
Output Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	70	—	pF
Reverse Transfer Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	2.2	—	pF
Functional Tests (In Freescale Test Fixture, 50 ohm system) V_{DD} = 26 Vdc, P_{out} = 100 W, I_{DQ} = 700 mA, f = 960 MHz					
Power Gain	G_{ps}	16	17.5	19	dB
Drain Efficiency	η_D	56	60	—	%
Input Return Loss	IRL	—	-15	-9	dB
P_{out} @ 1 dB Compression Point, CW	P1dB	100	110	—	W

1. Part is internally input matched.

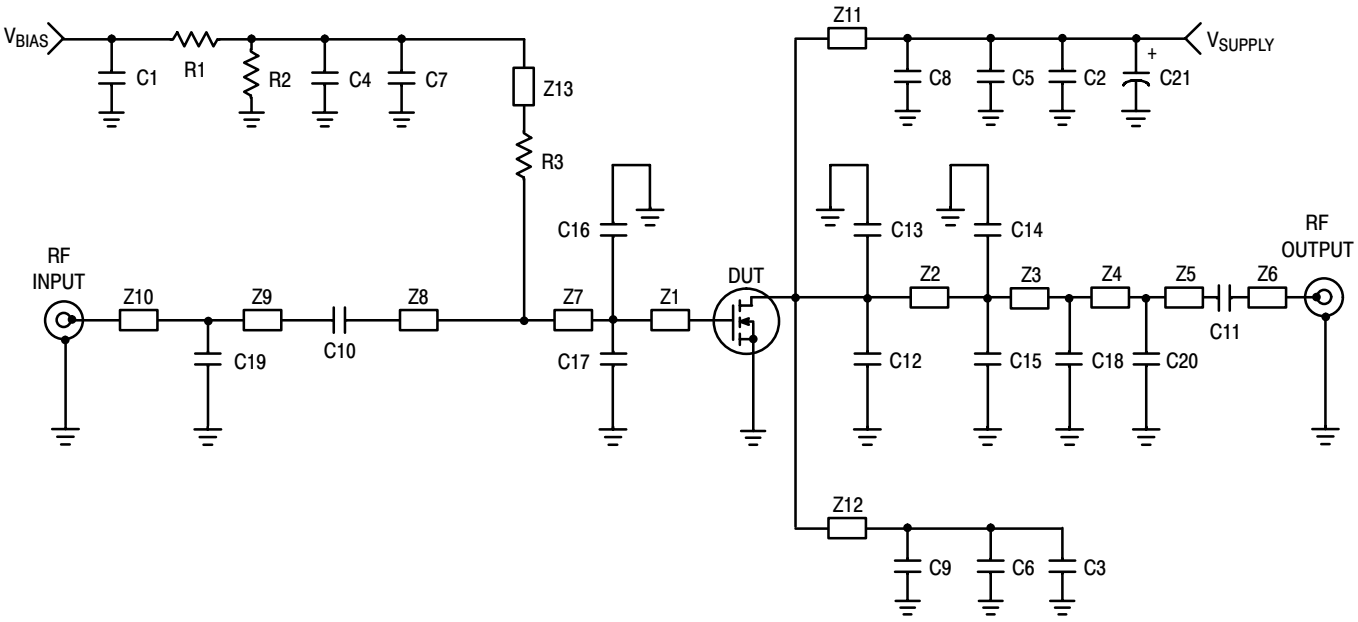
(continued)

ARCHIVE INFORMATION

Table 5. Electrical Characteristics (T_C = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Typical GSM EDGE Performances (In Freescale GSM EDGE Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, P_{out} = 50 W Avg., I_{DQ} = 650 mA, 869 MHz<Frequency<894 MHz, 920 MHz<Frequency<960 MHz					
Power Gain	G_{ps}	—	18	—	dB
Drain Efficiency	η_D	—	42	—	%
Error Vector Magnitude	EVM	—	2.3	—	% rms
Spectral Regrowth at 400 kHz Offset	SR1	—	-63	—	dBc
Spectral Regrowth at 600 kHz Offset	SR2	—	-78	—	dBc

ARCHIVE INFORMATION



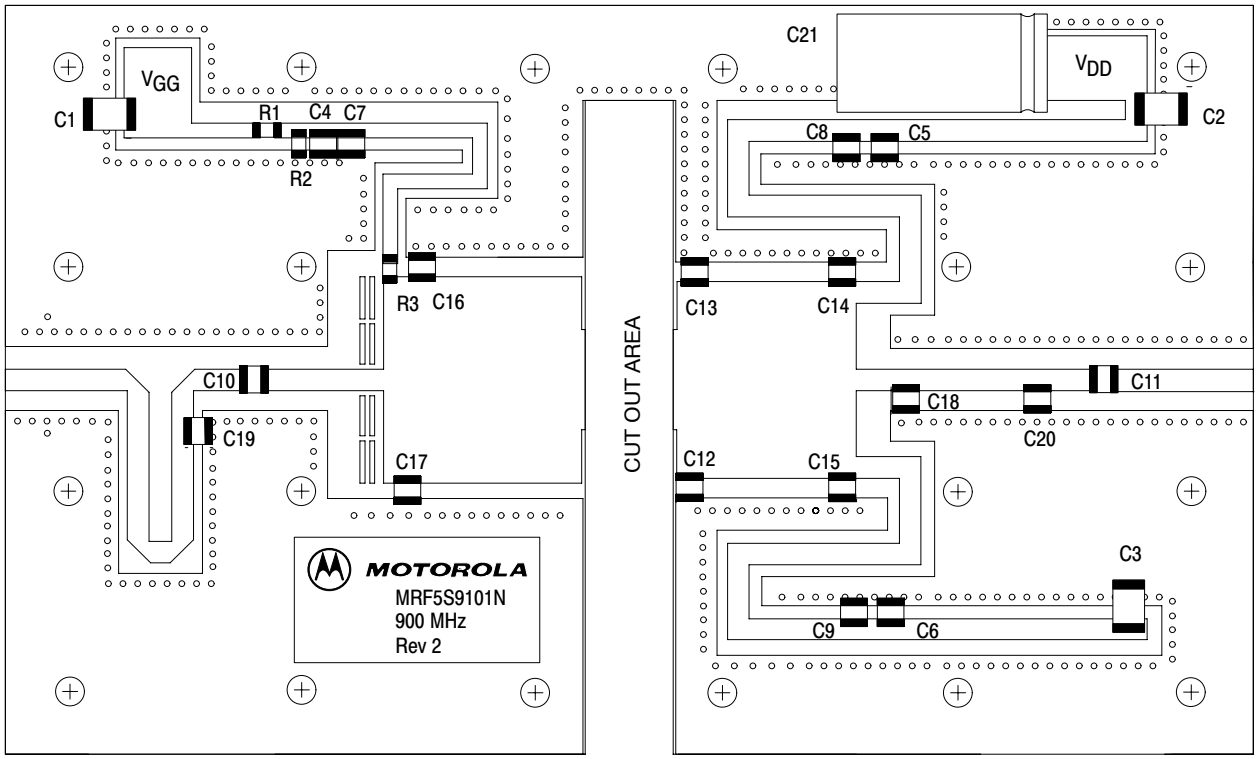
Z1	0.698″ x 0.827″ Microstrip	Z10	1.491″ x 0.087″ Microstrip
Z2	0.720″ x 0.788″ Microstrip	Z11, Z12*	1.6″ x 0.089″ Microstrip (quarter wave length for supply purpose)
Z3	0.195″ x 0.087″ Microstrip		
Z4	0.524″ x 0.087″ Microstrip	Z13*	1.2″ x 0.059″ Microstrip (quarter wave length for bias purpose)
Z5	0.233″ x 0.087″ Microstrip		
Z6	0.560″ x 0.087″ Microstrip	PCB	Taconic TLX8-0300, 0.030″, ε_r = 2.55
Z7	0.095″ x 0.827″ Microstrip		
Z8	0.472″ x 0.087″ Microstrip	*Variable for tuning	
Z9	0.384″ x 0.087″ Microstrip		

Figure 1. MRF5S9101MR1(MBR1) 900 MHz Test Circuit Schematic

Table 6. MRF5S9101MR1(MBR1) 900 MHz Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C3	4.7 μF Chip Capacitors (2220)	GRM55ER7H475KA01	Murata
C4, C5, C6	10 nF 200B Chip Capacitors	200B103MW	ATC
C7, C8, C9	33 pF 100B Chip Capacitors	100B330JW	ATC
C10, C11	22 pF 100B Chip Capacitors	100B220GW	ATC
C12, C13	10 pF 100B Chip Capacitors	100B100GW	ATC
C14, C15, C16, C17	8.2 pF 100B Chip Capacitors	100B8R2CW	ATC
C18	5.6 pF 100B Chip Capacitor	100B5R6CW	ATC
C19	4.7 pF 100B Chip Capacitor	100B4R7BW	ATC
C20	3.9 pF 100B Chip Capacitor	100B3R9BW	ATC
C21	220 μF, 50 V Electrolytic Capacitor, Axial	516D227M050NP7B	Sprague
R1, R2	10 kΩ, 1/4 W Chip Resistors (1206)		
R3	10 Ω, 1/4 W Chip Resistor (1206)		

ARCHIVE INFORMATION



Freescale has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescale Semiconductor signature/logo. PCBs may have either Motorola or Freescale markings during the transition period. These changes will have no impact on form, fit or function of the current product.

Figure 2. MRF5S9101MR1(MBR1) 900 MHz Test Circuit Component Layout

ARCHIVE INFORMATION

TYPICAL CHARACTERISTICS - 900 MHz

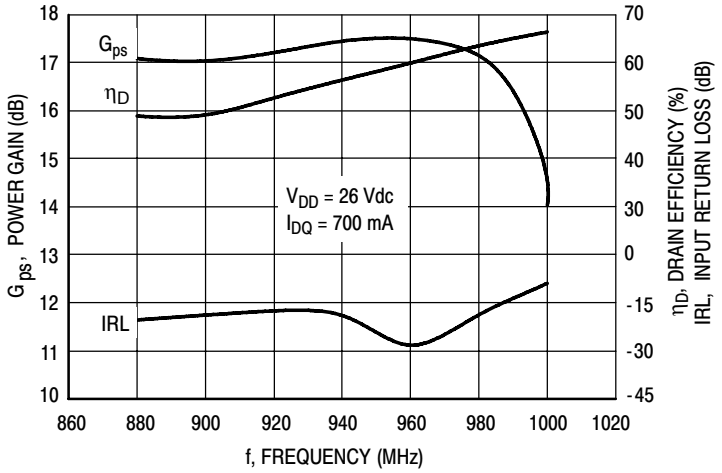


Figure 3. Power Gain, Input Return Loss and Drain Efficiency versus Frequency @ P_{out} = 100 Watts CW

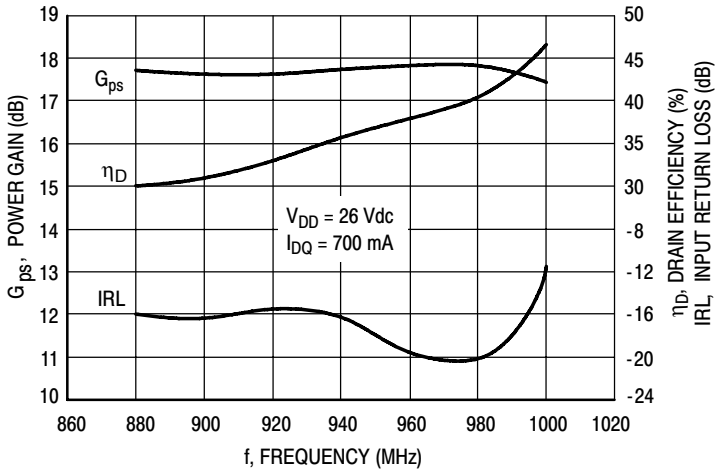


Figure 4. Power Gain, Input Return Loss and Drain Efficiency versus Frequency @ P_{out} = 40 Watts CW

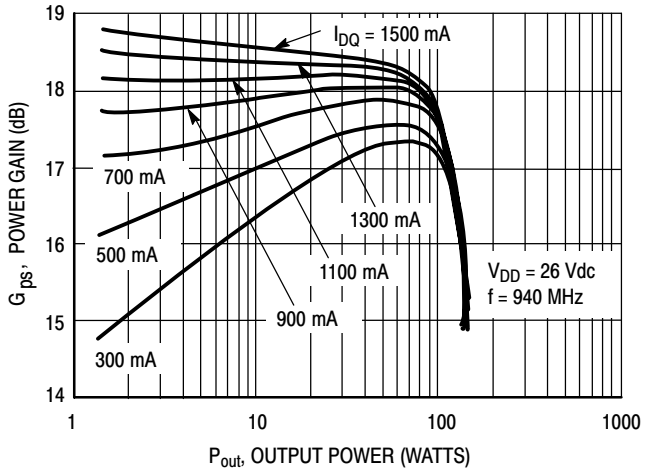


Figure 5. Power Gain versus Output Power

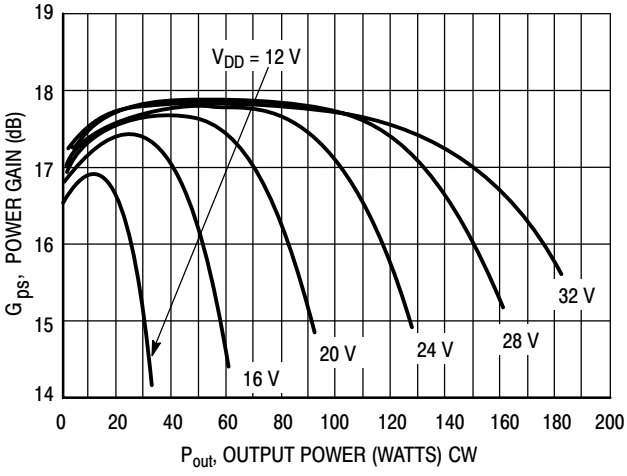


Figure 6. Power Gain versus Output Power

TYPICAL CHARACTERISTICS - 900 MHz

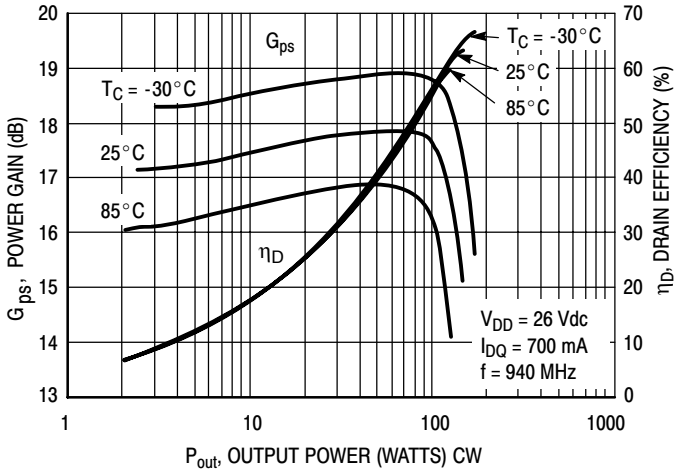


Figure 7. Power Gain and Drain Efficiency versus CW Output Power

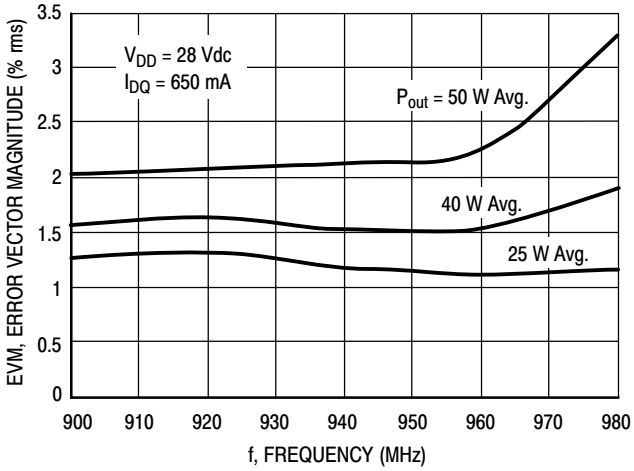


Figure 8. Error Vector Magnitude versus Frequency

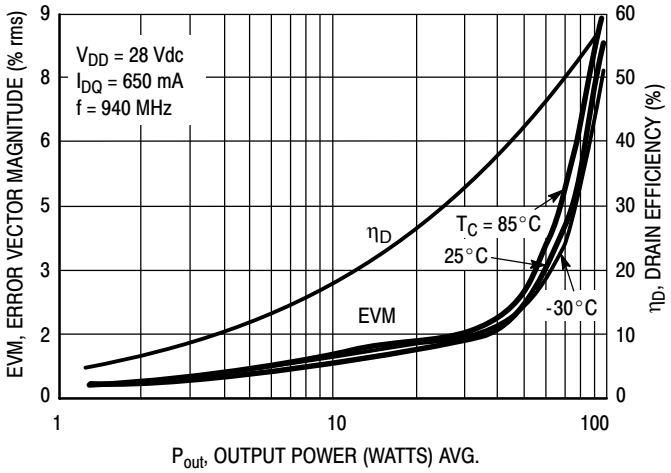


Figure 9. Error Vector Magnitude and Drain Efficiency versus Output Power

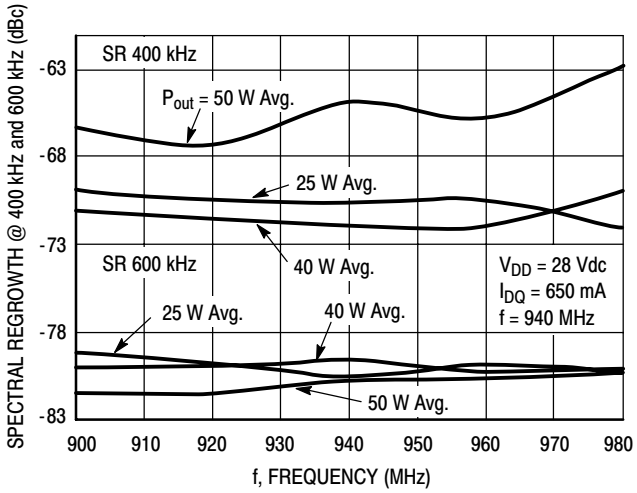


Figure 10. Spectral Regrowth at 400 kHz and 600 kHz versus Frequency

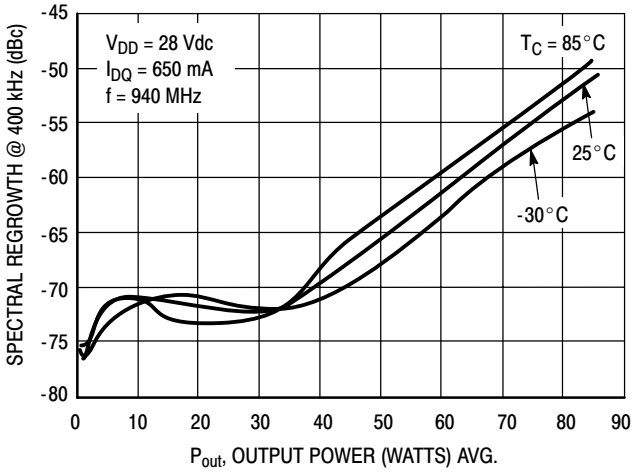


Figure 11. Spectral Regrowth at 400 kHz versus Output Power

TYPICAL CHARACTERISTICS - 900 MHz

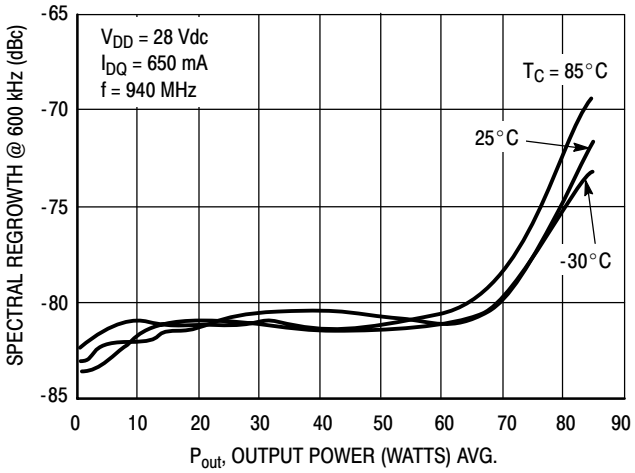
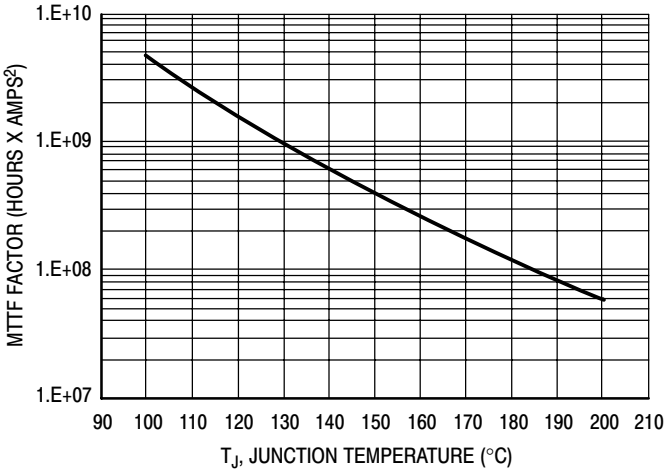
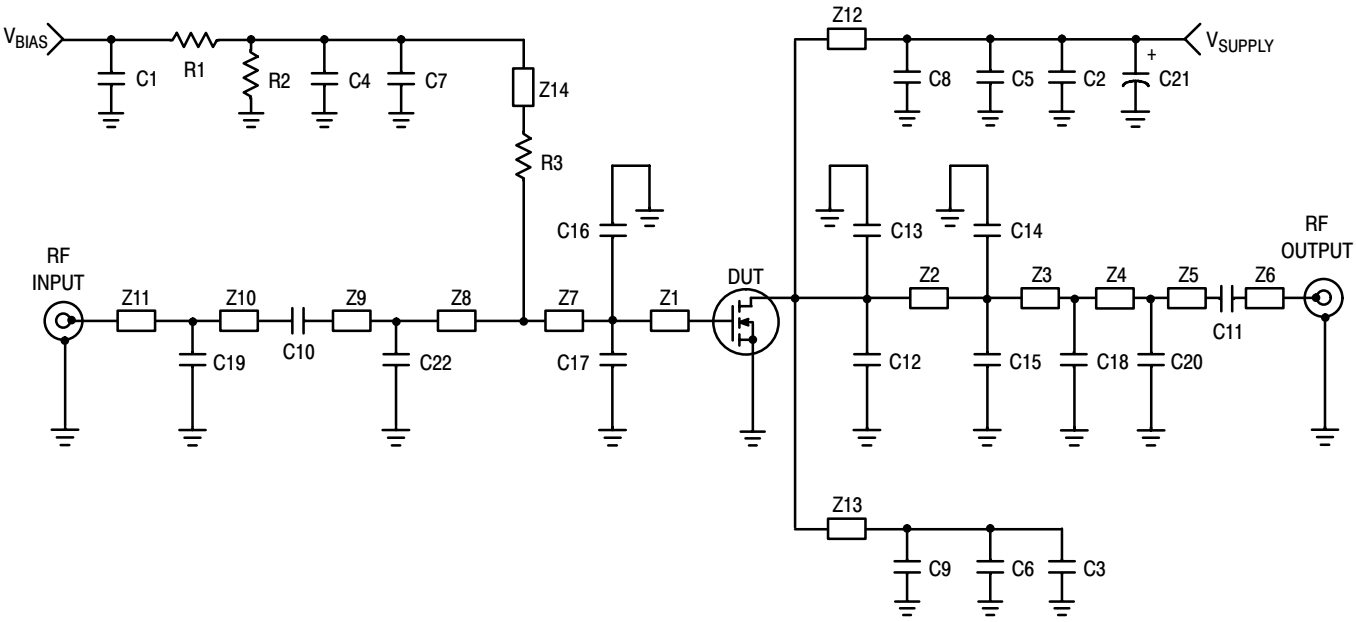


Figure 12. Spectral Regrowth @ 600 kHz versus Output Power



This above graph displays calculated MTTF in hours x ampere^2 drain current. Life tests at elevated temperatures have correlated to better than ±10% of the theoretical prediction for metal failure. Divide MTTF factor by I_D^2 for MTTF in a particular application.

Figure 13. MTTF Factor versus Junction Temperature



Z1	0.432″ x 0.827″ Microstrip	Z10	0.897″ x 0.087″ Microstrip
Z2	0.720″ x 0.788″ Microstrip	Z11	1.161″ x 0.087″ Microstrip
Z3	0.195″ x 0.087″ Microstrip	Z12, Z13*	1.6″ x 0.089″ Microstrip (quarter wave length for supply purpose)
Z4	0.584″ x 0.087″ Microstrip		
Z5	0.173″ x 0.087″ Microstrip	Z14*	1.2″ x 0.059″ Microstrip (quarter wave length for bias purpose)
Z6	0.560″ x 0.087″ Microstrip		
Z7	0.378″ x 0.827″ Microstrip	PCB	Taconic TLX8-0300, 0.030″, ε_r = 2.55
Z8	0.279″ x 0.087″ Microstrip		
Z9	0.193″ x 0.087″ Microstrip	*Variable for tuning	

Figure 14. MRF5S9101MR1(MBR1) 800 MHz Test Circuit Schematic

Table 7. MRF5S9101MR1(MBR1) 800 MHz Test Circuit Component Designations and Values

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C7, C8, C9	33 pF 100B Chip Capacitors	100B330JW	ATC
C10, C11	22 pF 100B Chip Capacitors	100B220GW	ATC
C12, C13, C17	10 pF 100B Chip Capacitors	100B100GW	ATC
C14, C15	8.2 pF 100B Chip Capacitors	100B8R2CW	ATC
C16, C22	6.8 pF 100B Chip Capacitors	100B6R8CW	ATC
C18	5.6 pF 100B Chip Capacitor	100B5R6CW	ATC
C19, C20	2.7 pF 100B Chip Capacitors	100B2R7BW	ATC
C21	220 μF, 50 V Electrolytic Capacitor, Axial	516D227M050NP7B	Sprague
R1, R2	10 kΩ, 1/4 W Chip Resistors (1206)		
R3	10 Ω, 1/4 W Chip Resistor (1206)		

ARCHIVE INFORMATION

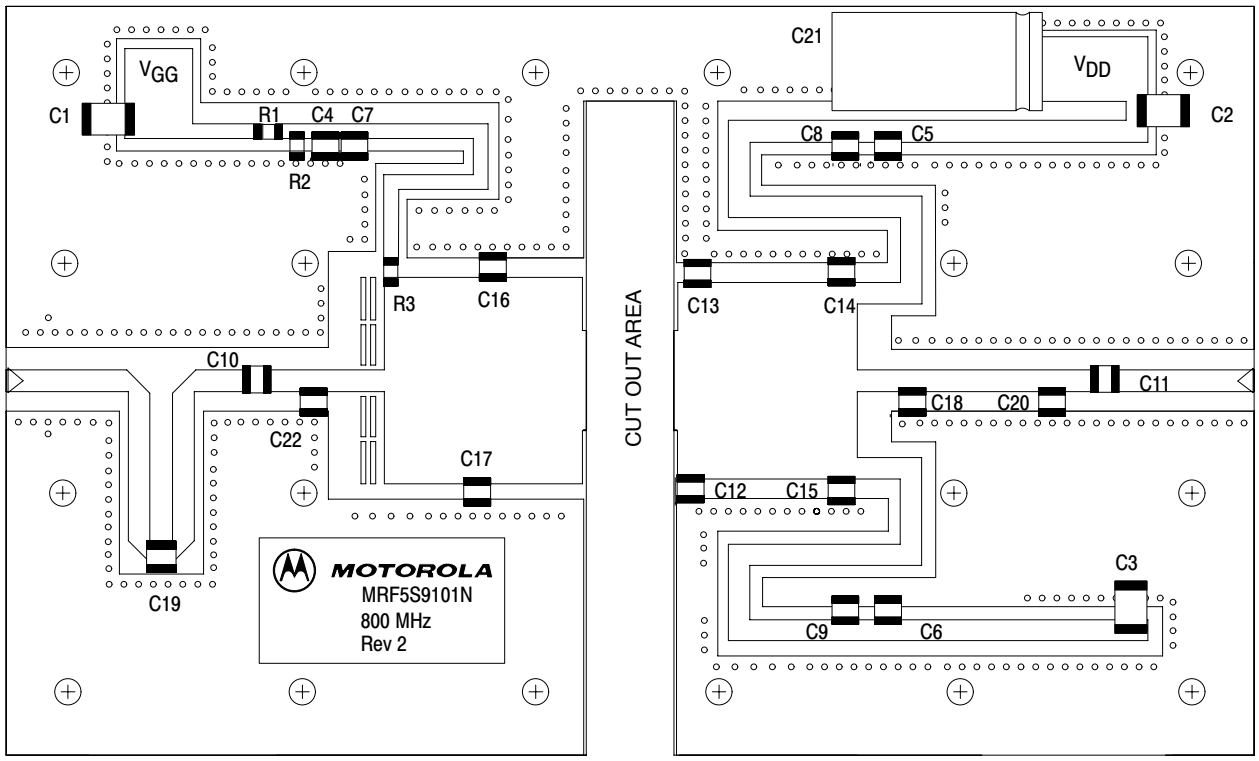

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Figure 15. MRF5S9101MR1(MBR1) 800 MHz Test Circuit Component Layout

ARCHIVE INFORMATION

TYPICAL CHARACTERISTICS - 800 MHz

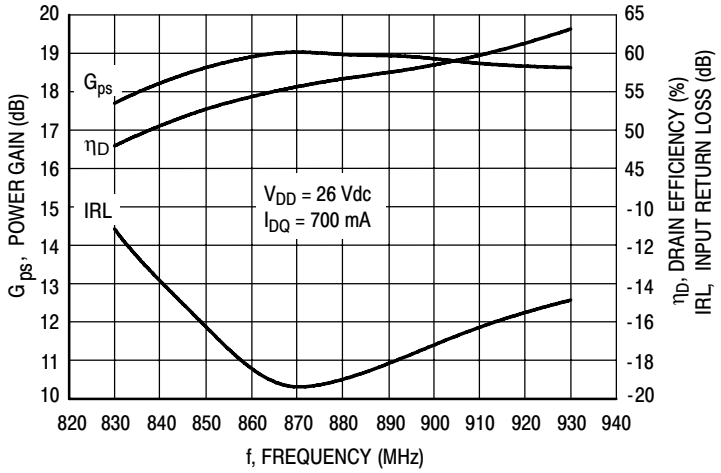


Figure 16. Power Gain, Input Return Loss and Drain Efficiency versus Frequency @ P_{out} = 100 W CW

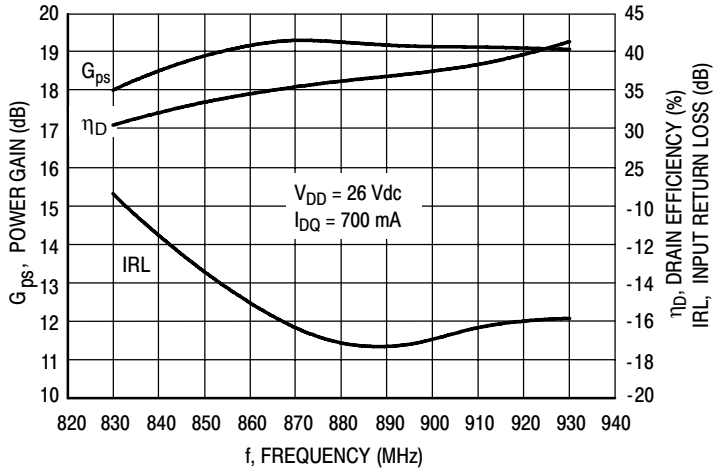


Figure 17. Power Gain, Input Return Loss and Drain Efficiency versus Frequency @ P_{out} = 40 W CW

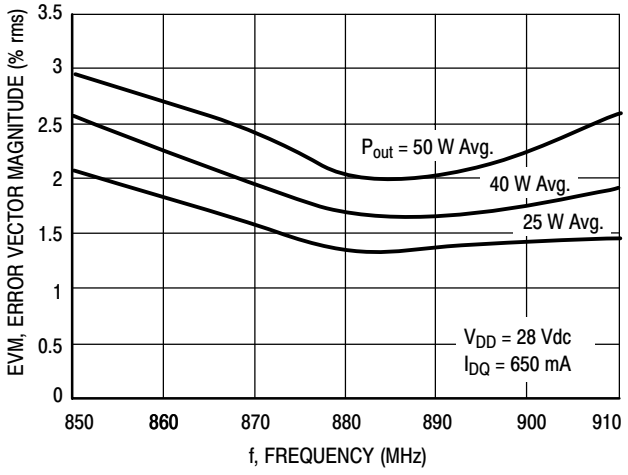


Figure 18. Error Vector Magnitude versus Frequency

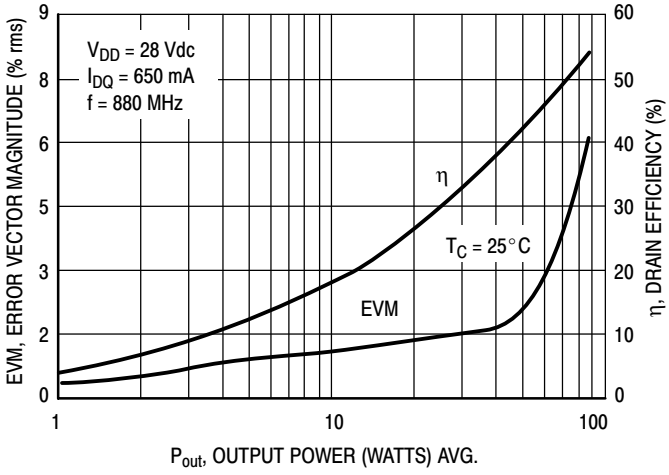


Figure 19. Error Vector Magnitude and Drain Efficiency versus Output Power

TYPICAL CHARACTERISTICS - 800 MHz

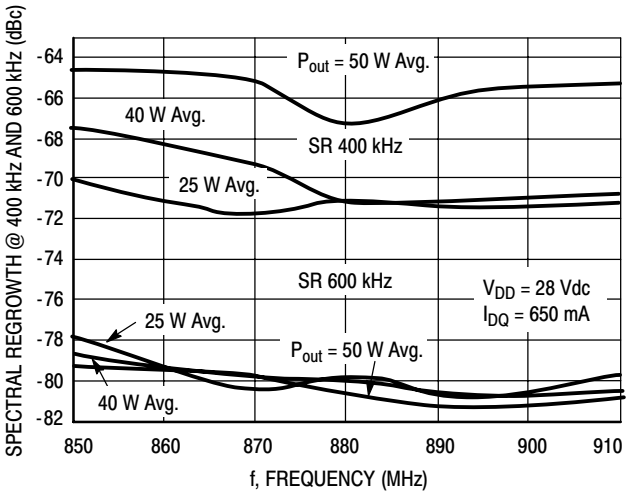


Figure 20. Spectral Regrowth at 400 kHz and 600 kHz versus Frequency

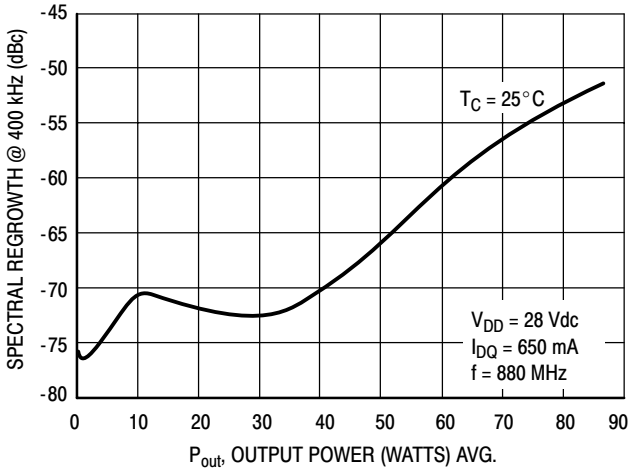


Figure 21. Spectral Regrowth at 400 kHz versus Output Power

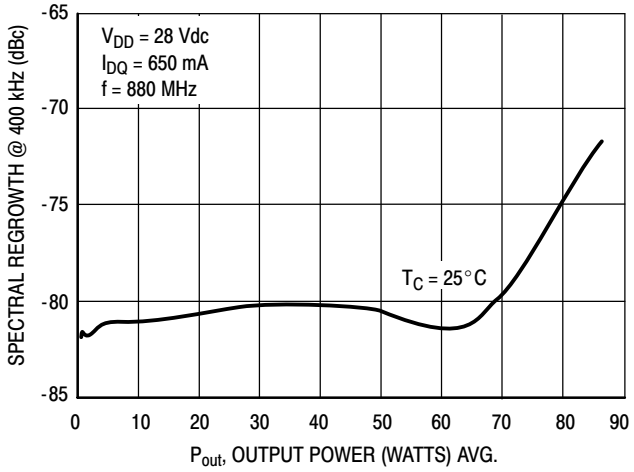
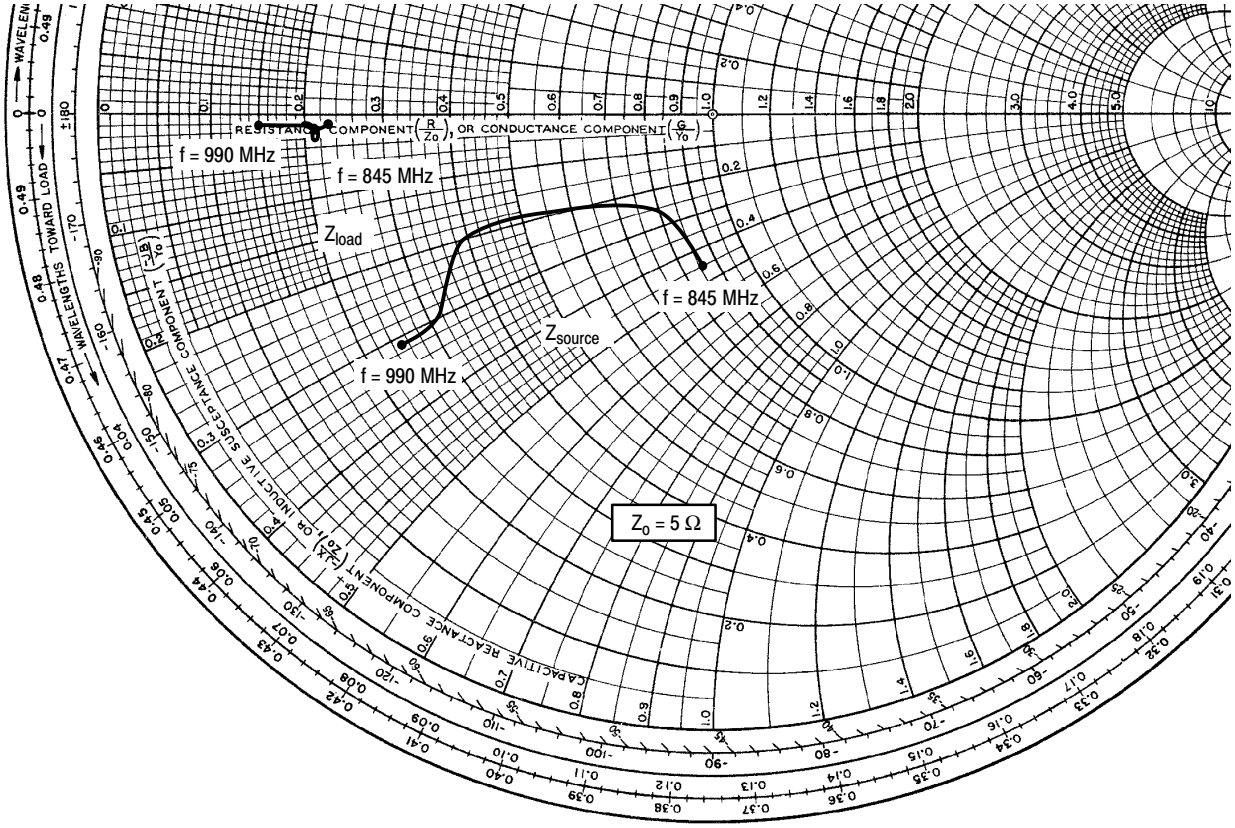


Figure 22. Spectral Regrowth at 600 kHz versus Output Power

ARCHIVE INFORMATION



V_{DD} = 26 Vdc, I_{DQ} = 700 mA, P_{out} = 100 W CW

f MHz	Z_{source} Ω	Z_{load} Ω
845	4.29 - j2.23	1.15 - j0.04
865	3.94 - j1.24	1.05 - j0.10
890	2.72 - j0.96	1.02 - j0.07
920	1.96 - j1.02	1.03 - j0.15
960	1.58 - j1.43	1.03 - j0.05
990	1.27 - j1.54	0.73 - j0.07

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

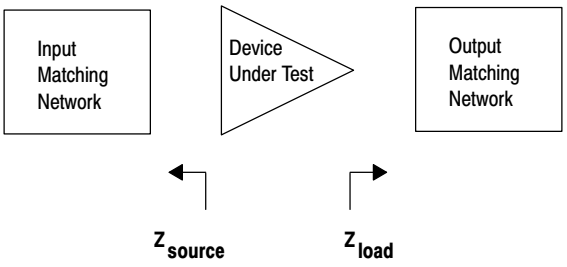
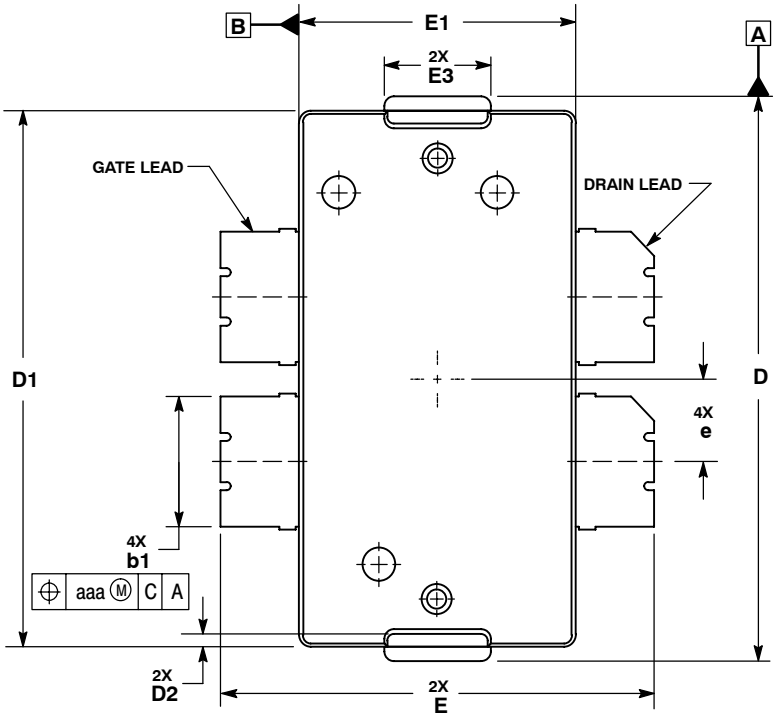


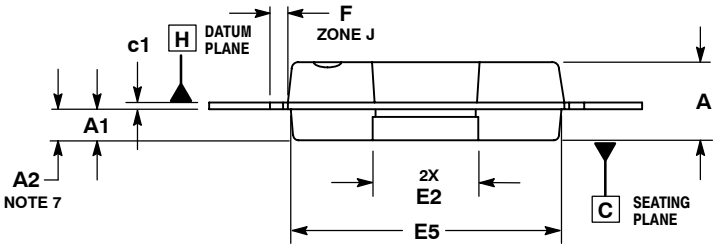
Figure 23. Series Equivalent Source and Load Impedance

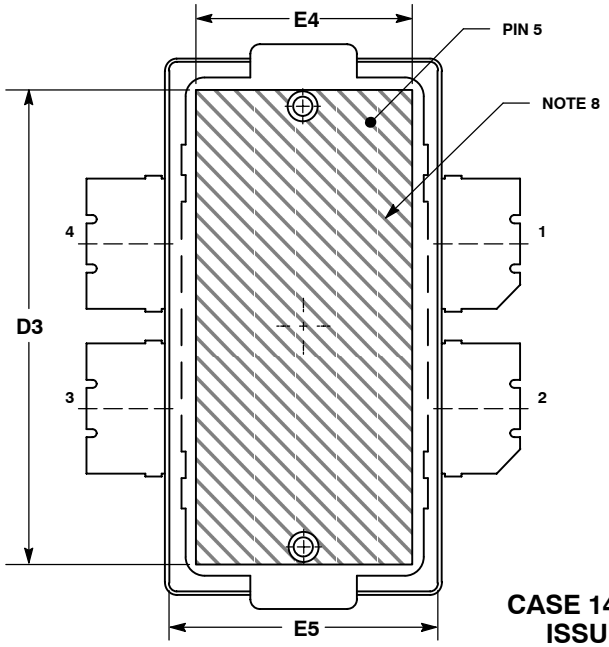
NOTES

NOTES

PACKAGE DIMENSIONS







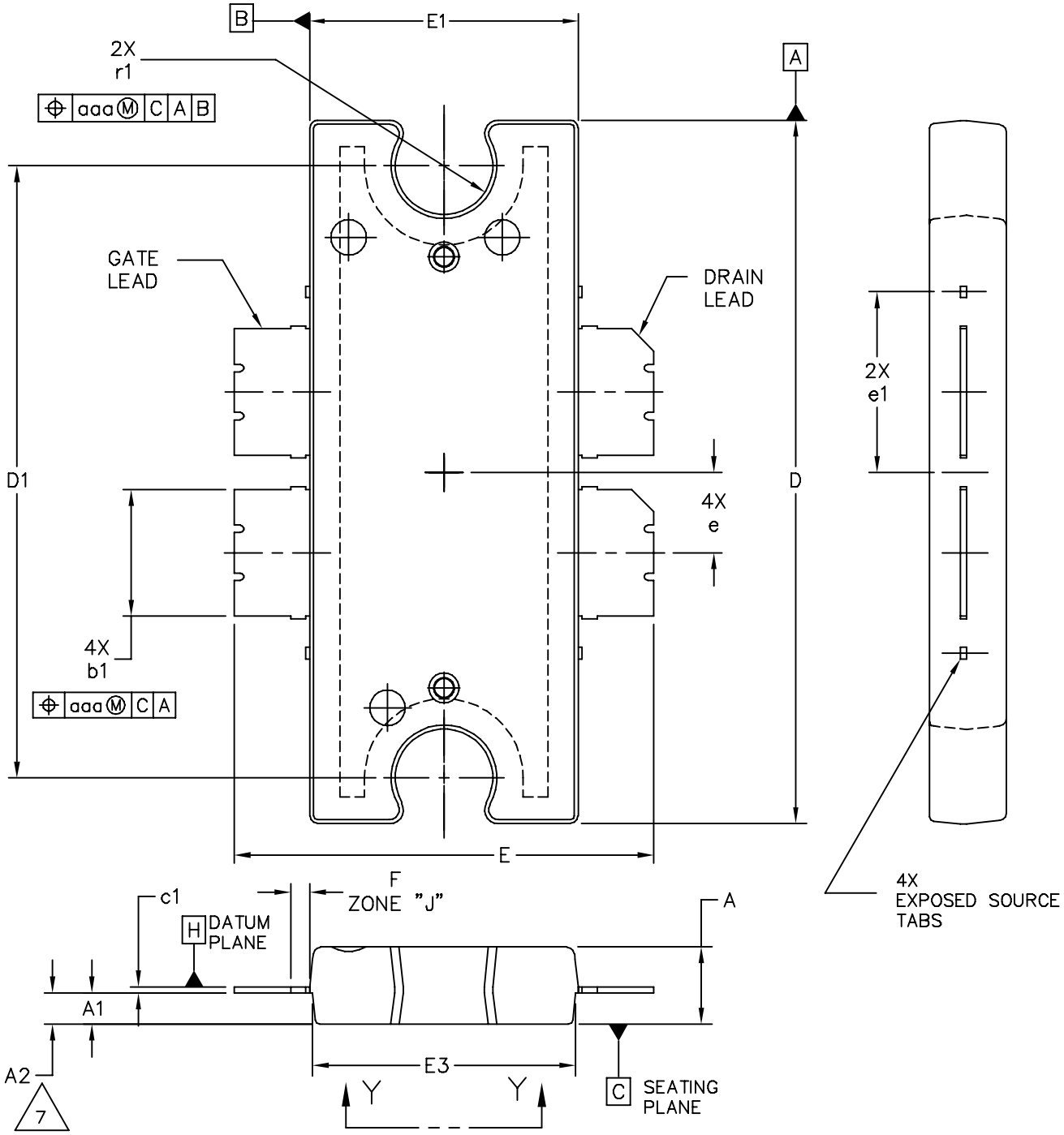
BOTTOM VIEW

NOTES:
1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSION "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64
A1	.039	.043	0.99	1.09
A2	.040	.042	1.02	1.07
D	.712	.720	18.08	18.29
D1	.688	.692	17.48	17.58
D2	.011	.019	0.28	0.48
D3	.600	---	15.24	---
E	.551	.559	14	14.2
E1	.353	.357	8.97	9.07
E2	.132	.140	3.35	3.56
E3	.124	.132	3.15	3.35
E4	.270	---	6.86	---
E5	.346	.350	8.79	8.89
F	.025 BSC		0.64 BSC	
b1	.164	.170	4.17	4.32
c1	.007	.011	0.18	0.28
e	.106 BSC		2.69 BSC	
aaa	.004		0.10	

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

CASE 1486-03
ISSUE C
TO-270 WB-4
PLASTIC
MRF5S9101MR1



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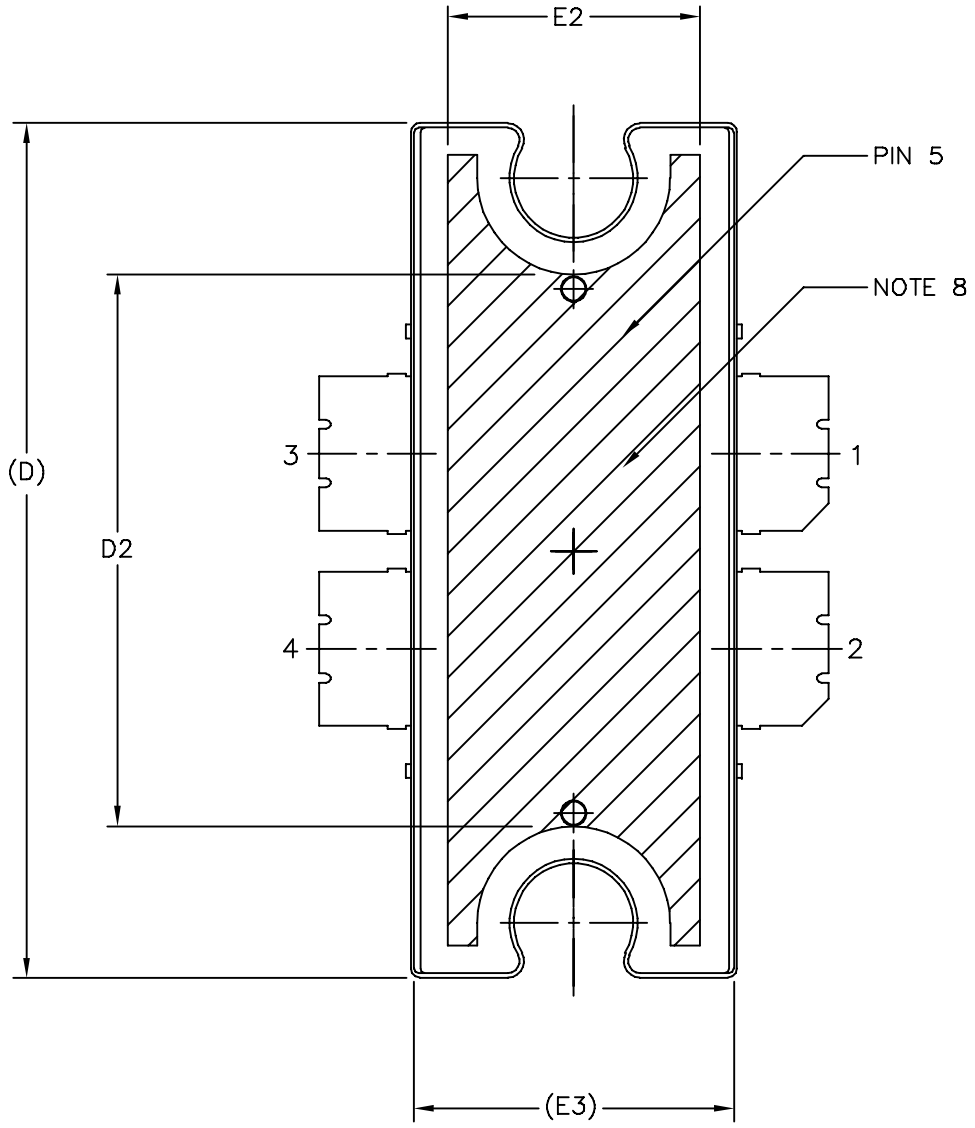
	CASE NUMBER: 1484−04	05 APR 2006
	STANDARD: NON−JEDEC	



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	CASE NUMBER: 1484−04	05 APR 2006
	STANDARD: NON−JEDEC	

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M−1994.
3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUM A AND B TO BE DETERMINED AT DATUM PLANE H.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS EXPOSED AREA OF THE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.

STYLE 1:
PIN 1 − DRAIN PIN 2 − DRAIN
PIN 3 − GATE PIN 4 − GATE
PIN 5 − SOURCE

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.100	.104	2.54	2.64	b1	.164	.170	4.17	4.32
A1	.039	.043	0.99	1.09	c1	.007	.011	.18	.28
A2	.040	.042	1.02	1.07	r1	.063	.068	1.60	1.73
D	.928	.932	23.57	23.67	e	.106 BSC		2.69 BSC	
D1	.810 BSC		20.57 BSC		e1	.239 INFO ONLY		6.07 INFO ONLY	
D2	.600	−−−	15.24	−−−	aaa	.004		.10	
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07					
E2	.270	−−−	6.86	−−−					
E3	.346	.350	8.79	8.89					
F	.025 BSC		0.64 BSC						

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TITLE:	DOCUMENT NO: 98ASA10575D	REV: D
TO−272 4 LEAD WIDE BODY	CASE NUMBER: 1484−04	05 APR 2006
	STANDARD: NON−JEDEC	

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