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# ESD5004

## ESD Protection Diode

### Low Capacitance ESD Protection Diode

The ESD5004 is designed for applications requiring ESD protection. It is intended to be used in sensitive equipment such as smartphone, wireless headsets, digital cameras, computers, printers, communication systems, and other applications. The integrated design provides very effective and reliable protection for four separate lines using only one package. This device is ideal for situations where board space is at a premium.

#### Features

- Low Capacitance (5 pF Max, I/O to GND)
- Four Separate Bi-directional Configurations for Protection
- Protection for the Following IEC Standards:  
IEC 61000-4-2 (Level 4)
- Low ESD Clamping Voltage
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

#### Typical Applications

- Smartphone and Portable Electronics
- Notebooks, Desktops, Servers
- Microprocessor Based Equipment

#### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T <sub>J</sub>	-55 to +125	°C
Storage Temperature Range	T <sub>stg</sub>	-65 to +150	°C
Lead Solder Temperature – Maximum (10 Seconds)	T <sub>L</sub>	260	°C
IEC 61000-4-2 Contact (ESD)	ESD	±12	kV
IEC 61000-4-2 Air (ESD)	ESD	±15	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

See Application Note AND8308/D for further description of survivability specs.



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#### MARKING DIAGRAM

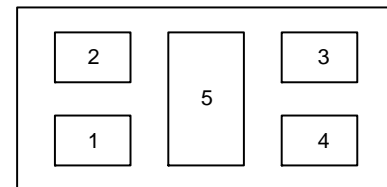


X3DFN4  
CASE 714AA

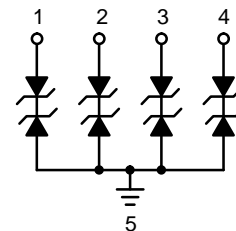


4 = Specific Device Code  
M = Date Code

#### PIN CONFIGURATION AND SCHEMATIC



(Bottom View)



#### ORDERING INFORMATION

Device	Package	Shipping†
ESD5004MXTBG	X3DFN4 (Pb-Free)	8000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# ESD5004

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	$V_{RWM}$	I/O Pin to GND			3.3	V
Breakdown Voltage	$V_{BR}$	$I_T = 1\text{ mA}$ , I/O Pin to GND	3.9			V
Reverse Leakage Current	$I_R$	$V_{RWM} = 3.3\text{ V}$ , I/O Pin to GND			1.0	$\mu\text{A}$
Clamping Voltage	$V_C$	$8 \times 20\ \mu\text{s}$ , $I_{pp} = 1\text{ A}$		5.0	9.1	V
Clamping Voltage TLP (Note 1) See Figures 4 and 5	$V_C$	$I_{PP} = 16\text{ A}$ $I_{PP} = -16\text{ A}$ } IEC 61000-4-2 Level 4 equivalent ( $\pm 8\text{ kV}$ Contact, $\pm 15\text{ kV}$ Air)		10 4.5		V
Junction Capacitance	$C_J$	$V_R = 0\text{ V}$ , $f = 1\text{ MHz}$ between I/O Pins and GND		3.5	5.0	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. ANSI/ESD STM5.5.1 – Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.

TLP conditions:  $Z_0 = 50\ \Omega$ ,  $t_p = 100\text{ ns}$ ,  $t_r = 4\text{ ns}$ , averaging window;  $t_1 = 30\text{ ns}$  to  $t_2 = 60\text{ ns}$ .

### IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

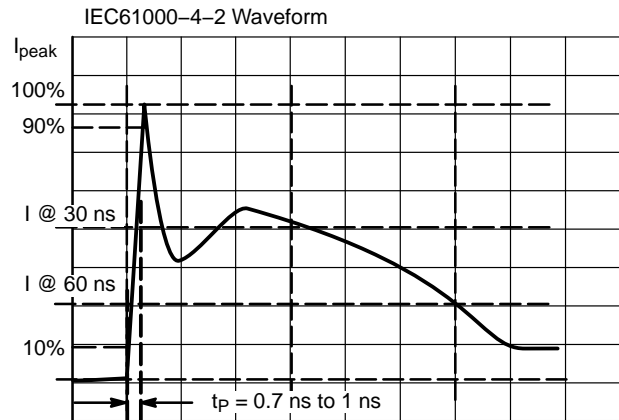


Figure 1. IEC61000-4-2 Spec

TYPICAL CHARACTERISTICS

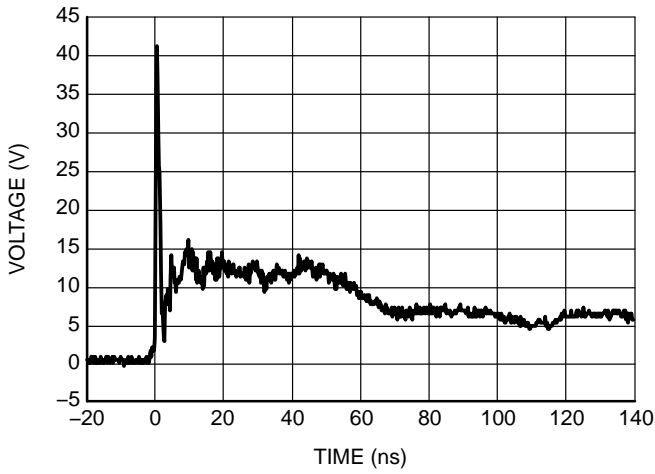


Figure 2. IEC61000-4-2 +8 kV Contact ESD Clamping Voltage

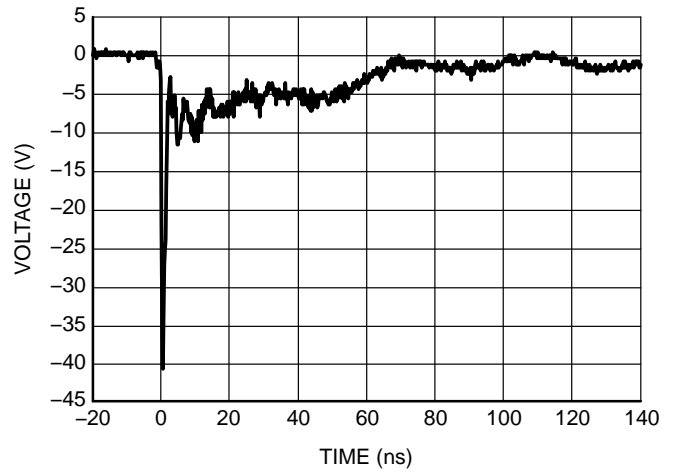


Figure 3. IEC61000-4-2 -8 kV Contact ESD Clamping Voltage

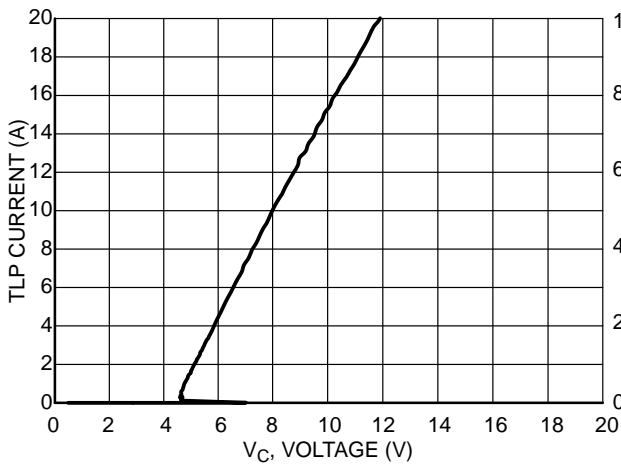


Figure 4. Positive TLP I-V Curve

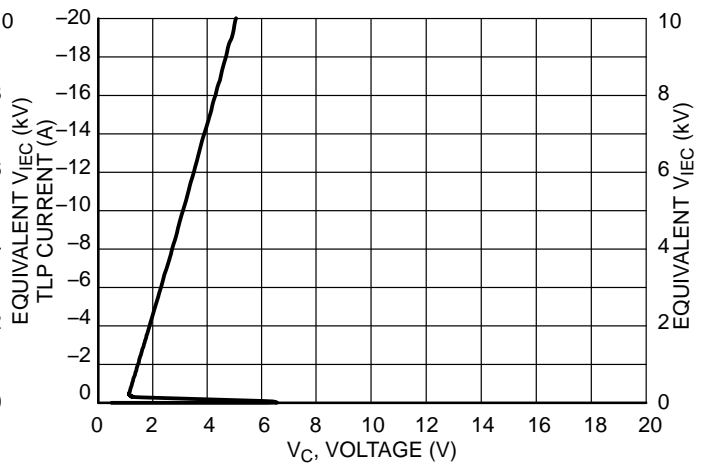


Figure 5. Negative TLP I-V Curve

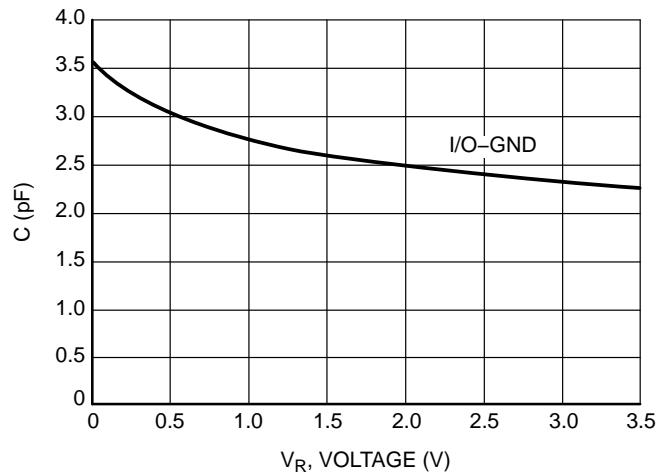
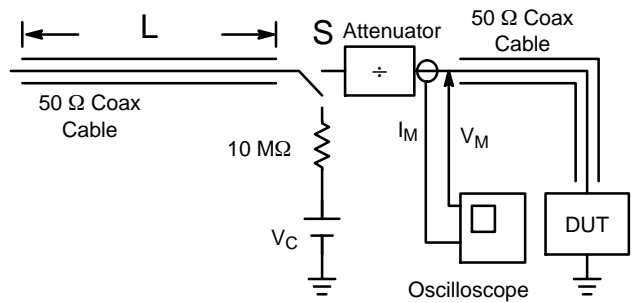


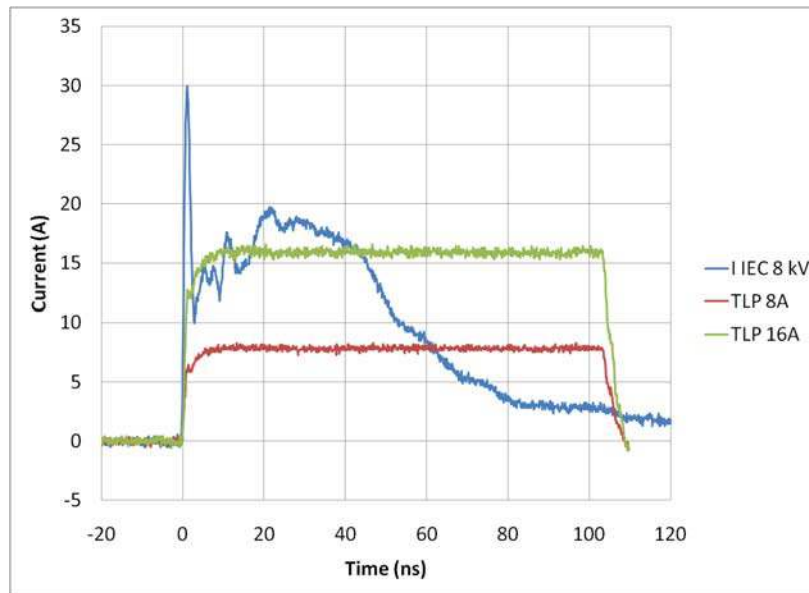
Figure 6. CV Characteristics

**Transmission Line Pulse (TLP) Measurement**

Transmission Line Pulse (TLP) provides current versus voltage (I–V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 7. TLP I–V curves of ESD protection devices accurately demonstrate the product’s ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 8 where an 8 kV IEC 61000–4–2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I–V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels. For more information on TLP measurements and how to interpret them please refer to AND9007/D.



**Figure 7. Simplified Schematic of a Typical TLP System**



**Figure 8. Comparison Between 8 kV IEC 61000–4–2 and 8 A and 16 A TLP Waveforms**

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

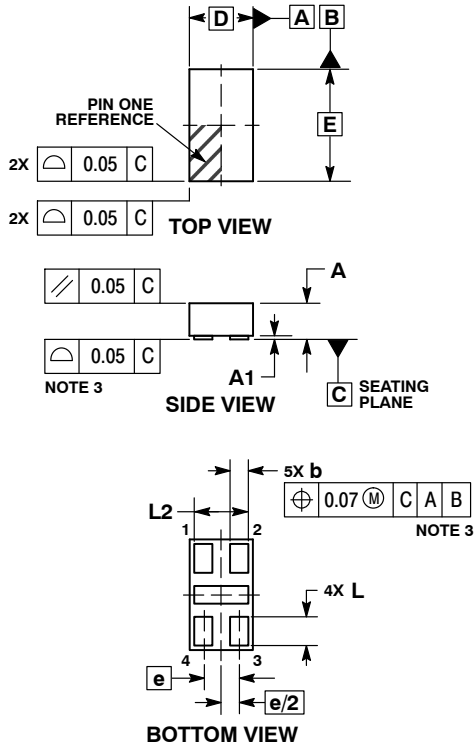
ON Semiconductor®



SCALE 8:1

**X3DFN4 0.525x0.925, 0.3P**  
CASE 714AA  
ISSUE B

DATE 08 DEC 2014



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.24	0.32
A1	0.00	0.05
b	0.12	0.18
D	0.525 BSC	
E	0.925 BSC	
e	0.30 BSC	
L	0.173	0.233
L2	0.42	0.48

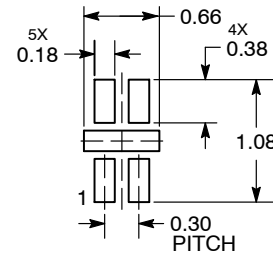
**GENERIC MARKING DIAGRAM\***



- X = Specific Device Code
- M = Date Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G", may or not be present.

**RECOMMENDED SOLDER FOOTPRINT\***




DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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