

MC74VHC244

Octal Bus Buffer

The MC74VHC244 is an advanced high speed CMOS octal bus buffer fabricated with silicon gate CMOS technology.

The MC74VHC244 is a noninverting 3-state buffer, and has two active-low output enables. This device is designed to be used with 3-state memory address drivers, etc.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7 V, allowing the interface of 5 V systems to 3 V systems.

- High Speed: $t_{PD} = 3.9 \text{ ns}$ (Typ) at $V_{CC} = 5 \text{ V}$
- Low Power Dissipation: $I_{CC} = 4 \mu\text{A}$ (Max) at $T_A = 25^\circ\text{C}$
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2 V to 5.5 V Operating Range
- Low Noise: $V_{OLP} = 0.9 \text{ V}$ (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: Human Body Model > 2000 V
Machine Model > 200 V
- Chip Complexity: 136 FETs
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

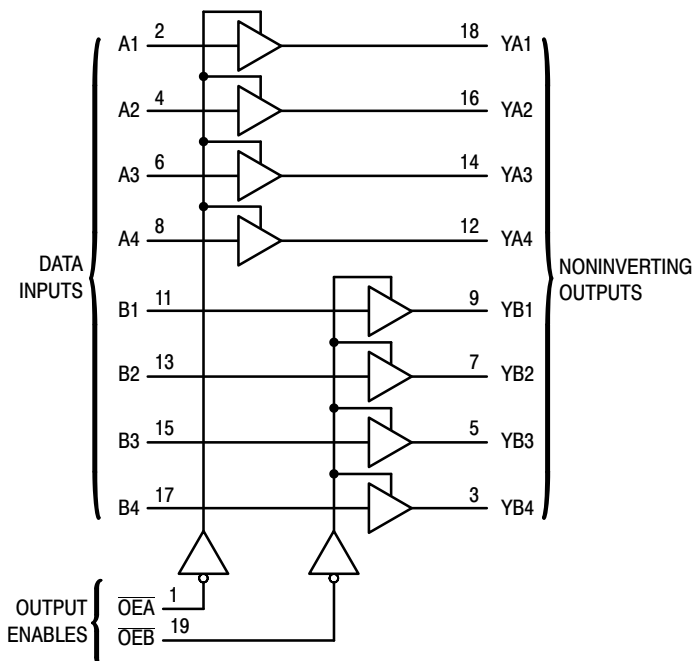


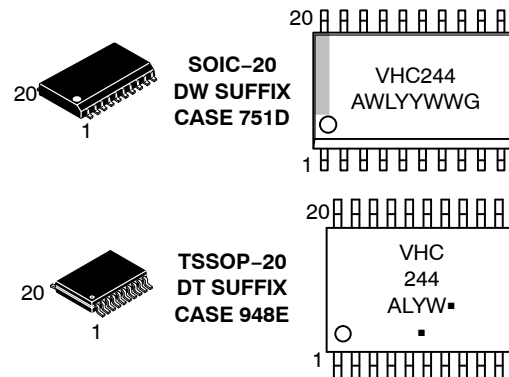
Figure 1. Logic Diagram



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MARKING DIAGRAMS



VHC244 = Specific Device Code
 A = Assembly Location
 WL, L = Wafer Lot
 Y = Year
 WW, W = Work Week
 G or ■ = Pb-Free Package
 (Note: Microdot may be in either location)

PIN ASSIGNMENT

OE A	1	20	V_{CC}
A1	2	19	$\overline{OE} B$
YB4	3	18	YA1
A2	4	17	B4
YB3	5	16	YA2
A3	6	15	B3
YB2	7	14	YA3
A4	8	13	B2
YB1	9	12	YA4
GND	10	11	B1

ORDERING INFORMATION

See detailed ordering and shipping information in the Ordering Information Table on page 2 of this data sheet.

MC74VHC244

FUNCTION TABLE

INPUTS		OUTPUTS
\overline{OEA} , \overline{OEB}	A, B	YA, YB
L	L	L
L	H	H
H	X	Z

ORDERING INFORMATION

Device	Package	Shipping [†]
MC74VHC244DWR2G	SOIC-20 WB (Pb-Free)	1000/Tape & Reel
MC74VHC244DTG	TSSOP-20 (Pb-Free)	75 Units/Rail
MC74VHC244DTR2G		2500/Tape & Reel
NLV74VHC244DTR2G*		2500/Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage	-0.5 to +7.0	V
V_{IN}	Digital Input Voltage	-0.5 to +7.0	V
V_{OUT}	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	Input Diode Current	-20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{OUT}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air	SOIC TSSOP 500 450	mW
T_{STG}	Storage Temperature Range	-65 to +150	°C
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4) >2000 >200 >2000	V
$I_{LATCHUP}$	Latchup Performance	Above V_{CC} and Below GND at 125°C (Note 5)	± 300 mA
θ_{JA}	Thermal Resistance, Junction-to-Ambient	SOIC TSSOP 96 128	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.
- Tested to EIA/JESD22-A114-A
- Tested to EIA/JESD22-A115-A
- Tested to JESD22-C101-A
- Tested to EIA/JESD78

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RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit		
V _{CC}	DC Supply Voltage	2.0	5.5	V		
V _{IN}	DC Input Voltage	0	5.5	V		
V _{OUT}	DC Output Voltage	0	V _{CC}	V		
T _A	Operating Temperature Range, all Package Types	-55	125	°C		
t _r , t _f	Input Rise or Fall Time					
			V _{CC} = 3.3 V ± 0.3 V	0	100	ns/V
			V _{CC} = 5.0 V ± 0.5 V		20	

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

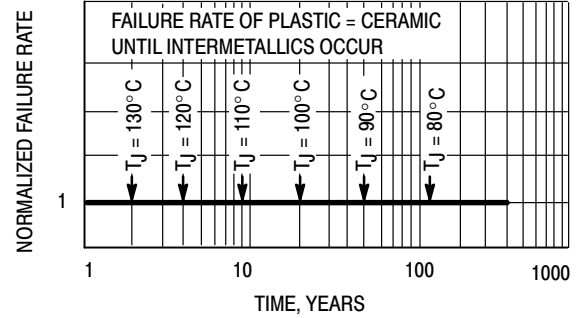


Figure 2. Failure Rate vs. Time Junction Temperature

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			T _A ≤ 85°C		-55°C ≤ T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	Minimum High-Level Input Voltage		2.0 3.0 to 5.5	1.5 V _{CCX} 0.7			1.5 V _{CCX} 0.7	1.5 V _{CCX} 0.7	1.5 V _{CCX} 0.7		V
V _{IL}	Maximum Low-Level Input Voltage		2.0 3.0 to 5.5			0.5 V _{CCX} 0.3		0.5 V _{CCX} 0.3		0.5 V _{CCX} 0.3	V
V _{OH}	Maximum High-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OH} = -50 μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		V _{IN} = V _{IH} or V _{IL} I _{OH} = -4 mA I _{OH} = -8 mA	3.0 4.5	2.58 3.94			2.48 3.8		2.34 3.66		
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OL} = 50 μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		V _{IN} = V _{IH} or V _{IL} I _{OH} = 4 mA I _{OH} = 8 mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	
I _{IN}	Input Leakage Current	V _{IN} = 5.5 V or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I _{OZ}	Maximum 3-State Leakage Current	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND	5.5			±0.25		±2.5		±2.5	μA
I _{CC}	Maximum Quiescent Supply Current (per package)	V _{IN} = V _{CC} or GND	5.5			4.0		40.0		40.0	μA

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AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$			$T_A \leq 85^\circ\text{C}$		$-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, A to YA or B to YB	$V_{CC} = 3.3 \pm 0.3$ V $C_L = 15$ pF		5.8	8.4	1.0	10.0	1.0	11.0	ns
		$C_L = 50$ pF		8.3	11.9	1.0	13.5	1.0	14.5	
		$V_{CC} = 5.0 \pm 0.5$ V $C_L = 15$ pF		3.9	5.5	1.0	6.5	1.0	7.5	
		$C_L = 50$ pF		5.4	7.5	1.0	8.5	1.0	9.5	
t_{PZL} , t_{PZH}	Output Enable Time $\overline{OE}A$ to YA or $\overline{OE}B$ to YB	$V_{CC} = 3.3 \pm 0.3$ V $C_L = 15$ pF		6.6	10.6	1.0	12.5	1.0	13.5	ns
		$R_L = 1$ k Ω $C_L = 50$ pF		9.1	14.1	1.0	16.0	1.0	17.0	
		$V_{CC} = 5.0 \pm 0.5$ V $C_L = 15$ pF		4.7	7.3	1.0	8.5	1.0	9.5	
		$R_L = 1$ k Ω $C_L = 50$ pF		6.2	9.3	1.0	10.5	1.0	11.5	
t_{PLZ} , t_{PHZ}	Output Disable Time $\overline{OE}A$ to YA or $\overline{OE}B$ to YB	$V_{CC} = 3.3 \pm 0.3$ V $C_L = 50$ pF		10.3	14.0	1.0	16.0	1.0	17.0	ns
		$R_L = 1$ k Ω								
		$V_{CC} = 5.0 \pm 0.5$ V $C_L = 50$ pF		6.7	9.2	1.0	10.5	1.0	11.5	
		$R_L = 1$ k Ω								
t_{OSLH} , t_{OSHL}	Output to Output Skew	$V_{CC} = 3.3 \pm 0.3$ V $C_L = 50$ pF (Note 6)			1.5		1.5		1.5	ns
		$V_{CC} = 5.0 \pm 0.5$ V $C_L = 50$ pF (Note 6)			1.0		1.0		1.5	
C_{in}	Maximum Input Capacitance			4	10		10		10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)			6						pF

C_{PD}	Power Dissipation Capacitance (Note 7)	Typical @ 25°C, $V_{CC} = 5.0$ V		pF
		19		

6. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.

7. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}/8$ (per bit). C_{PD} is used to determine the no-load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns, $C_L = 50$ pF, $V_{CC} = 5.0$ V)

Symbol	Parameter	$T_A = 25^\circ\text{C}$		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.6	0.9	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	-0.6	-0.9	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

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SWITCHING WAVEFORMS

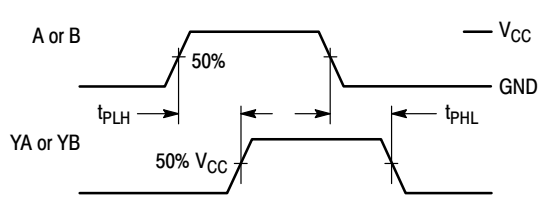


Figure 3. Switching Waveform

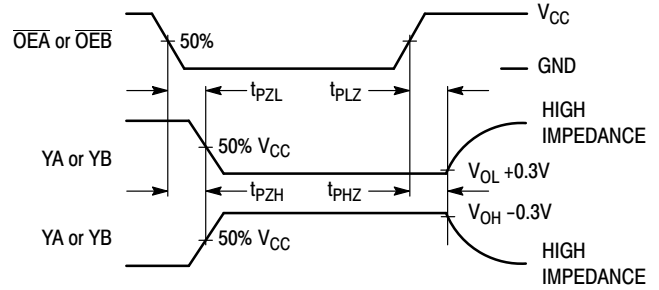
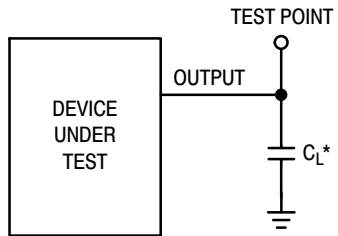


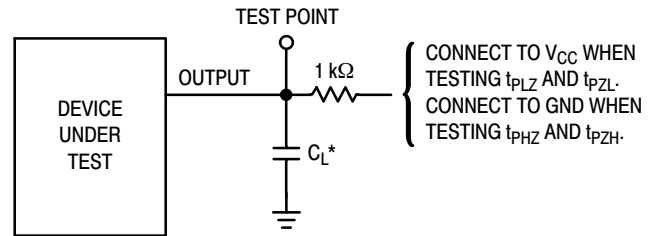
Figure 4. Switching Waveform

TEST CIRCUITS



*Includes all probe and jig capacitance

Figure 5. Test Circuit



*Includes all probe and jig capacitance

Figure 6. Test Circuit

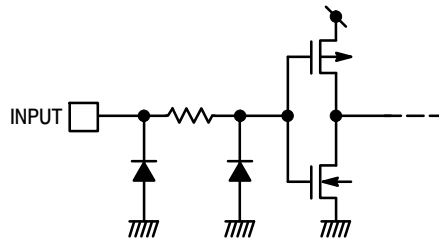
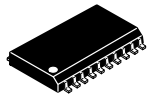


Figure 7. Input Equivalent Circuit

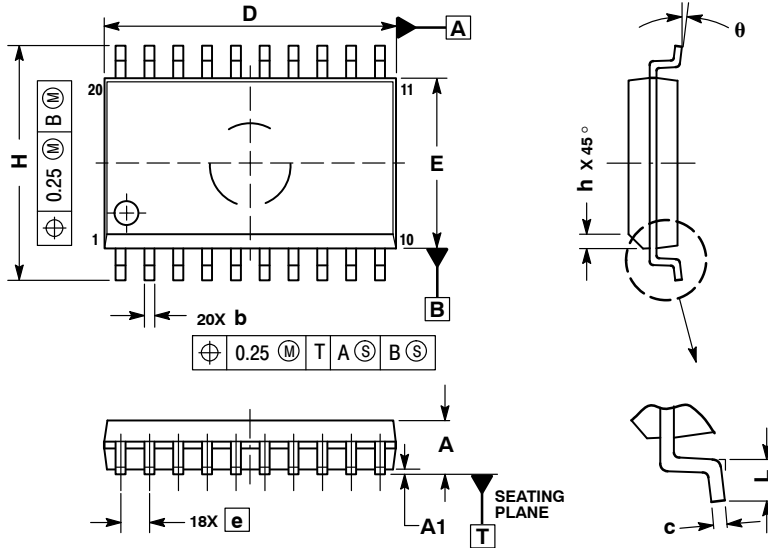
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-20 WB
CASE 751D-05
ISSUE H

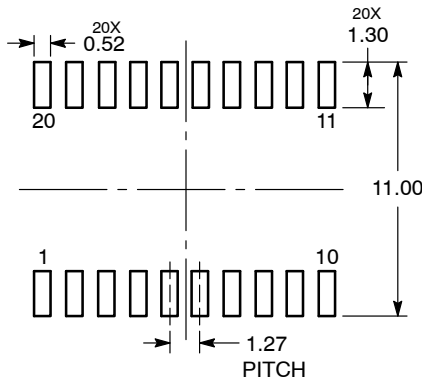
DATE 22 APR 2015



- NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
 5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

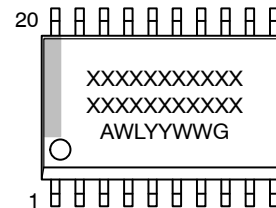
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

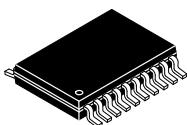
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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

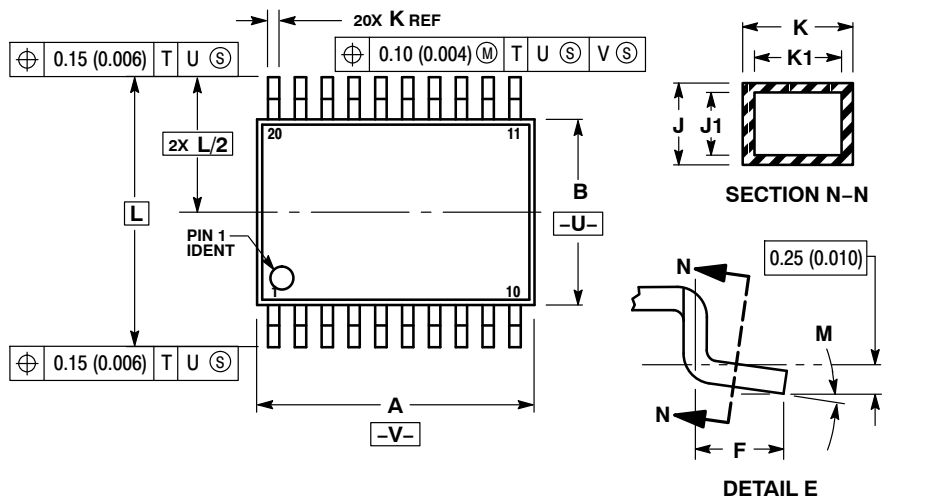
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TSSOP-20 WB
CASE 948E
ISSUE D

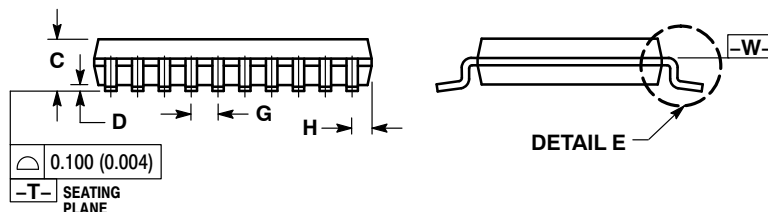
DATE 17 FEB 2016

SCALE 2:1

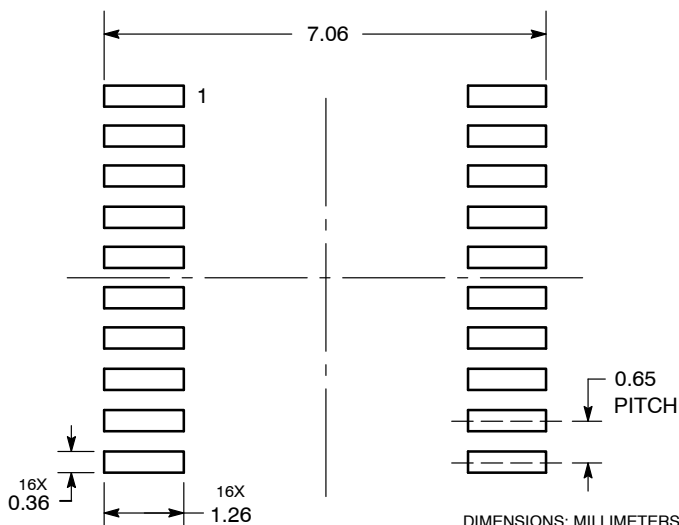


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

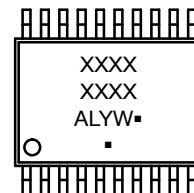


SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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