High Frequency Switch Mode Dual Li-Ion Battery Chargers

ADP3801/ADP3802

FEATURES

Stand-Alone Li-Ion Battery Chargers
High End-of-Charge Voltage Accuracy
±0.4% @ +25°C
±0.75% @ –10°C to +70°C
Intelligent End-of-Charge Output Signal
Pin Programmable Cell Number Select
On Chip 3.3 V LDO Regulator
Programmable Charge Current with High Side Sense
Softstart Charge Current
Undervoltage Lockout
Drives External PMOS
±10% Adjustable End-of-Charge Voltage
Charges NiCad, NiMH (with External µController)
PWM Oscillator Frequency:
ADP3801: 200 kHz
ADP3802: 500 kHz

APPLICATIONS

Fast Chargers
Universal Chargers
Cellular Phones
Portable Computers
Portable Instrumentation
Desktop Chargers
Personal Digital Assistants

FUNCTIONAL BLOCK DIAGRAM

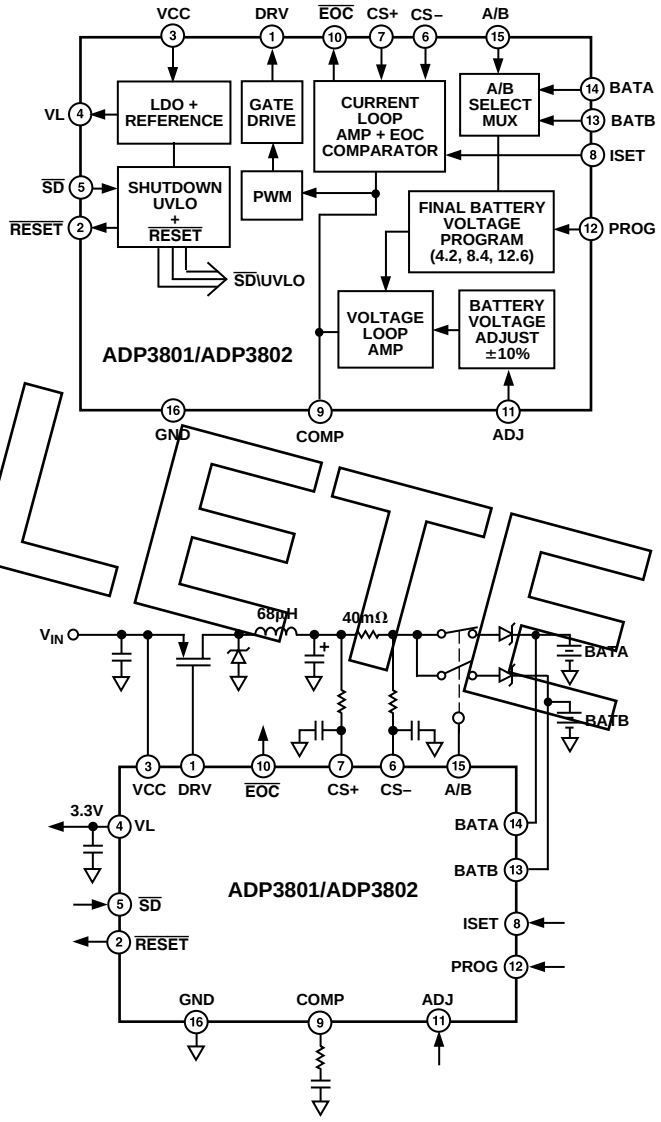

Figure 1. 4 Amp Dual Battery Charger

GENERAL DESCRIPTION

The ADP3801 and ADP3802 are complete battery charging ICs. The devices combine a high accuracy final battery voltage control with a constant charge current control and an on-board Low Drop-Out Regulator (LDO). The accuracy of the final battery voltage control is guaranteed to ±0.75% to safely charge Li-Ion batteries. An internal multiplexer allows the alternate charging of two separate battery stacks. The final voltage is pin programmable to one of three Li-Ion options: 4.2 V (one Li-Ion cell), 8.4 V (two Li-Ion cells), or 12.6 V (three Li-Ion cells). Paired with an external microcontroller for charge termination, the ADP3801/ADP3802 works as a fast charger for NiCad/NiMH batteries or as a universal charger for all three battery chemistries. In addition, a pin is provided for changing the final battery voltage by up to ±10% to adjust for variations in battery chemistry from different Li-Ion manufacturers without loss of accuracy in the final battery voltage.

REV. 0

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ADP3801/ADP3802–SPECIFICATIONS (@ –40°C ≤ T_A ≤ +85°C, VCC = 10.0 V, unless otherwise noted)

Parameter	Conditions	Symbol	Min	Typ	Max	Units
FINAL BATTERY VOLTAGE						
One Li-Ion Cell	PROG = V_{T1}, ADJ = VL, T_A = +25°C	V_{BAT}	4.180	4.200	4.220	V
	PROG = V_{T1}, ADJ = VL, –10°C ≤ T_A ≤ +70°C	V_{BAT}	4.168		4.232	V
	PROG = V_{T1}, ADJ = VL, –40°C ≤ T_A ≤ +85°C	V_{BAT}	4.150		4.250	V
Two Li-Ion Cells[1]	PROG = V_{T2}, ADJ = VL, T_A = +25°C	V_{BAT}	8.366	8.400	8.434	V
	PROG = V_{T2}, ADJ = VL, –10°C ≤ T_A ≤ +70°C	V_{BAT}	8.337		8.463	V
	PROG = V_{T2}, ADJ = VL, –40°C ≤ T_A ≤ +85°C	V_{BAT}	8.300		8.500	V
Three Li-Ion Cells[1]	PROG = V_{T3}, ADJ = VL, T_A = +25°C	V_{BAT}	12.550	12.600	12.650	V
	PROG = V_{T3}, ADJ = VL, –10°C ≤ T_A ≤ +70°C	V_{BAT}	12.505		12.695	V
	PROG = V_{T3}, ADJ = VL, –40°C ≤ T_A ≤ +85°C	V_{BAT}	12.450		12.750	V
BATTERY PROGRAMMING INPUT (PROG)						
One Li-Ion Cell (4.2 V)		V_{T1}	0.00		0.20	V
Two Li-Ion Cells (8.4 V)		V_{T2}	1.00		1.20	V
Three Li-Ion Cells (12.6 V)		V_{T3}	2.05		2.30	V
Fail Safe Voltage (4.2 V)	Defaults to 1 Li-Ion Cell		3.10		3.30	V
PROG Input Current		I_B		1.5	5	µA
A/B SELECT MUX						
Select Battery BATB		V_{IH}	2.0			V
Select Battery BATA		V_{IL}			0.8	V
A/B Input Current		I_{IN}		0.02	1	µA
BATA or BATB Input Resistance	Channel Selected	R_{IN}	185	265		kΩ
BATA or BATB Input Current	Channel Not Selected	I_{BA}, I_{BB}		0.2	1	µA
BATA or BATB Shutdown Current	Part in Shutdown	I_{BA}, I_{BB}		0.2	1	µA
BATTERY ADJUST INPUT[2] (ADJ)						
% of Final Battery Voltage	ADJ = 1.0 V, –10°C ≤ T_A ≤ +70°C		89	90	91	%
% of Final Battery Voltage	ADJ = 2.3 V, –10°C ≤ T_A ≤ +70°C		109	110	111	%
ADJ Disable Voltage Threshold	0% Change			2.475	2.6	V
ADJ Bias Current	1.0 V ≤ ADJ ≤ 2.3 V	I_B		10	100	nA
OVERVOLTAGE COMPARATOR						
Trip Point	Percent Above V_{BAT}			8		%
Response Time	DRV Goes High	tr		2		µs
OSCILLATOR						
200 kHz Option	(ADP3801)	f_{OSC}	150	200	250	kHz
500 kHz Option	(ADP3802)	f_{OSC}	375	500	625	kHz
0% Duty Cycle Threshold	@ COMP Pin			1.0		V
100% Duty Cycle Threshold	@ COMP Pin			2.0		V
GATE DRIVE						
Rise Time	C_L = 1 nF, VCC – 4 V to 90%	t_r		35		ns
Fall Time	C_L = 1 nF, 90% to VCC – 4 V	t_f		75		ns
Output High Saturation Voltage	VCC – V_{DRV}	V_{OH}		275		mV
Output Low Voltage	VCC = 8 V	V_{OL}	1.0	2.0		V
	VCC > 8 V	V_{OL}	VCC – 7	VCC – 6		V
CURRENT SENSE AMPLIFIER						
Input Common-mode Range	V_{CS+} and $V_{CS–}$	V_{CSCM}	0.0		VCC – 2	V
Input Differential Mode Range	V_{CS}[3]	V_{CSDM}	0.0		185	mV
Input Offset Voltage[4]	0.0 V ≤ V_{CSCM} ≤ VCC – 2 V	V_{CSVOS}		1		mV
Input Bias Current	0.0 V ≤ V_{CSCM} ≤ VCC – 2 V	V_{CSIB}		0.3	1	µA
Input Offset Current	0.0 V ≤ V_{CSCM} ≤ VCC – 2 V	V_{CSIOS}		0.01	0.15	µA
Over Current Trip Point	V_{CS}[3]			185		mV
Response Time	DRV Goes High	tr		2		µs
ISET INPUT						
Charge Current Programming Function	0.0 V ≤ V_{ISET} ≤ 1.65 V	V_{CS}/V_{ISET}[3]		0.1		V/V
Programming Function Accuracy	V_{ISET} = 1.65 V, –10°C ≤ T_A ≤ +70°C		–5	±1.0	+5	%
	V_{ISET} = 0.10 V, –10°C ≤ T_A ≤ +70°C		–25	±10	+25	%
ISET Bias Current	0.0 V ≤ V_{ISET} ≤ 1.65 V	I_B		15	100	nA

Parameter	Conditions	Symbol	Min	Typ	Max	Units
$\overline{EOC}$ OUTPUT[5]						
Trip Point	100 kΩ to VL	V_{CS}[3]		10		mV
Hysteresis	100 kΩ to VL	V_{CS}[3]		0.2		mV
SHUTDOWN ($\overline{SD}$)						
ON		$\overline{SD}_H$	2.0			V
OFF		$\overline{SD}_L$			0.8	V
$\overline{SD}$ Input Current				0.2	1	µA
LOW DROPOUT REGULATOR						
Output Voltage[6]	0 mA ≤ I_{LOAD} ≤ 10 mA, 4.1 V ≤ VCC ≤ 20 V, –10°C ≤ T_A ≤ +70°C	VL	3.267	3.3	3.333	V
	0 mA ≤ I_{LOAD} ≤ 10 mA, 4.1 V ≤ VCC ≤ 20 V, –40°C ≤ T_A ≤ +85°C	VL	3.250		3.350	V
Dropout Voltage (VCC – VL)	I_{LOAD} = 10 mA	V_{DO}		0.4	0.8	V
Output Current Drive		I_{VL}	10	20		mA
$\overline{RESET}$ OUTPUT						
VL Rising Threshold	$\overline{RESET}$ High		2.5	2.7	2.9	V
VL Falling Threshold	$\overline{RESET}$ Low		2.4	2.55	2.8	V
Output High Logic Level	1 MΩ to Ground External		2.4	2.9		V
POWER SUPPLY						
ON Supply Current	No External Loads	I_{SYON}		5.0	7.0	mA
OFF Supply Current	No External Loads	I_{SYOFF}		115	180	µA
UVLO[6, 7]						
VCC Rising Threshold	Turn On		3.8	3.9	4.0	V
VCC Falling Threshold	Turn Off, I_{VL} = 1 mA			3.4		V

NOTES
[1] VCC = V_{BAT} + 2 V.
[2] See Figure 5.
[3] V_{CS} = (V_{CS+}) – ($V_{CS–}$).
[4] Accuracy guaranteed by ISET INPUT, Programming Function Accuracy specification.
[5] $\overline{EOC}$ Output Comparator monitors charge current, and it is enabled when V_{BAT} ≥ 95% of the final battery voltage.
[6] LDO is active during $\overline{SD}$ and UVLO.
[7] Turn-off threshold depends on LDO dropout.

All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Input Voltage (VCC to GND) . . . . . –0.3 V to 20 V
DRV, V_{CS+}, V_{CS-} to GND . . . . . –0.3 V to VCC
BATA, BATB to GND . . . . . –0.3 V to 14.0 V
A/B, ISET, PROG, ADJ to GND . . . . . –0.3 V to VL
$\overline{SD}$, $\overline{RESET}$, COMP, $\overline{EOC}$ to GND . . . . . –0.3 V to VL
Power Dissipation . . . . . Internally Limited
θ_{JA} . . . . . 75°C/W
Ambient Temperature Range . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 10 sec) . . . . . +300°C

NOTES

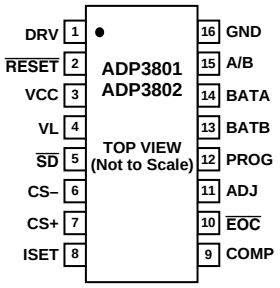
*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

θ_{JA} is specified for worst case conditions with device soldered on a circuit board.

ORDERING GUIDE

Model	Package Option	Oscillator Frequency
ADP3801AR	R-16A	200 kHz
ADP3802AR	R-16A	500 kHz

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin Number	Mnemonic	Function
1	$\overline{DRV}$	External Transistor Drive
2	$\overline{RESET}$	Power on $\overline{RESET}$ Output
3	VCC	Supply Voltage
4	VL	LDO Output
5	$\overline{SD}$	Shutdown Control Input
6	CS–	Negative Current Sense Input
7	CS+	Positive Current Sense Input
8	ISET	Charge Current Program Input
9	COMP	External Compensation Node
10	$\overline{EOC}$	End-of-Charge Output Signal
11	ADJ	Adjust Battery Voltage ± 10%
12	PROG	Program Final Battery Voltage Input
13	BATB	Battery "B" Voltage Sense
14	BATA	Battery "A" Voltage Sense
15	A/B[1]	"A" or "B" Battery Select Input
16	GND	Ground

NOTE

[1]"L" = Battery "A."

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP3801/ADP3802 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

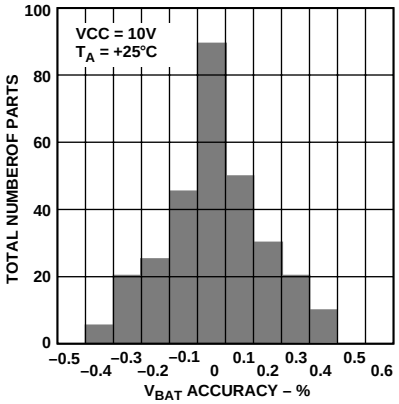


Figure 2. V_{BAT} Accuracy Distribution

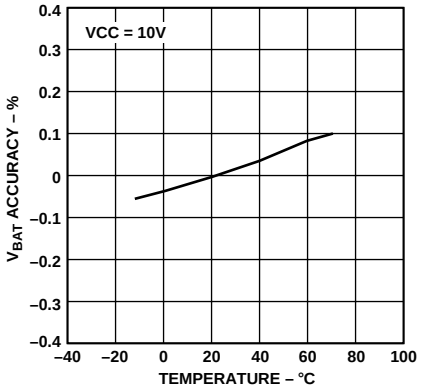


Figure 3. V_{BAT} Accuracy vs. Temperature

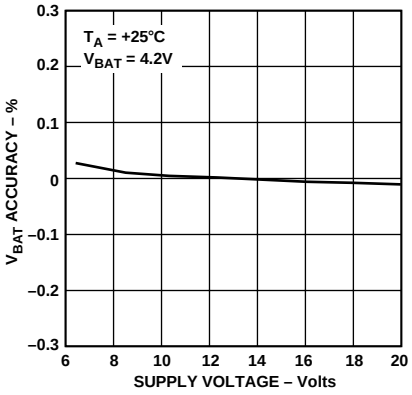


Figure 4. V_{BAT} Accuracy vs. Supply Voltage

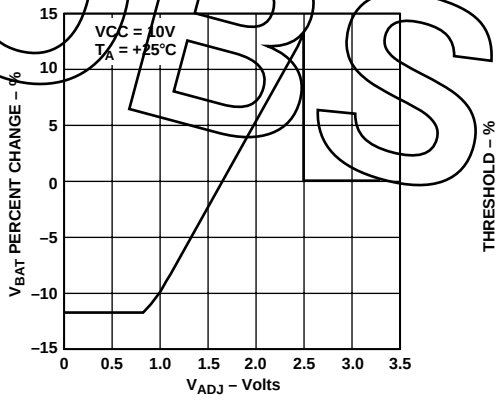


Figure 5. V_{BAT} Percent Change vs. V_{ADJ}

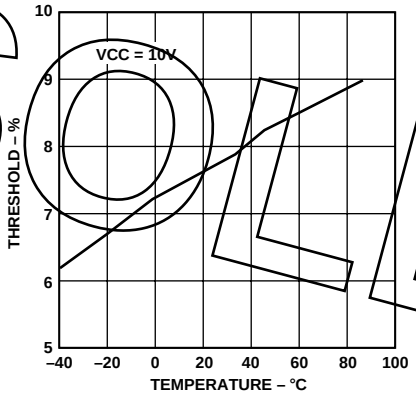


Figure 6. Overvoltage Comparator Threshold vs. Temperature

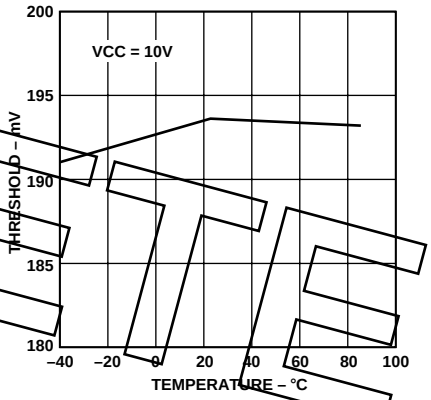


Figure 7. Overcurrent Comparator Threshold vs. Temperature

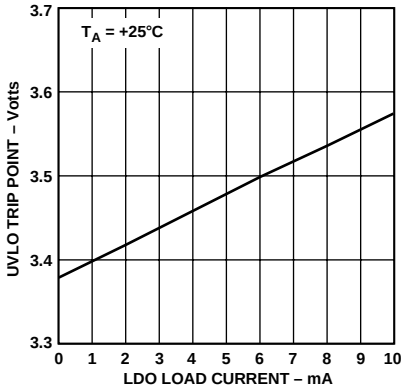


Figure 8. UVLO Trip Point-Off vs. LDO Load Current

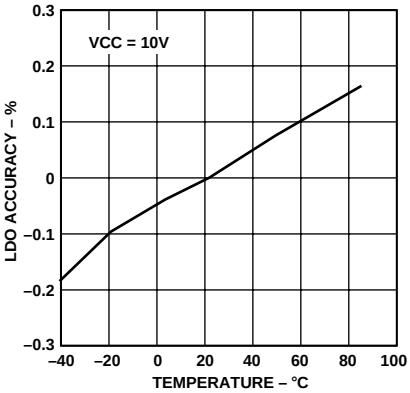


Figure 9. LDO Accuracy vs. Temperature

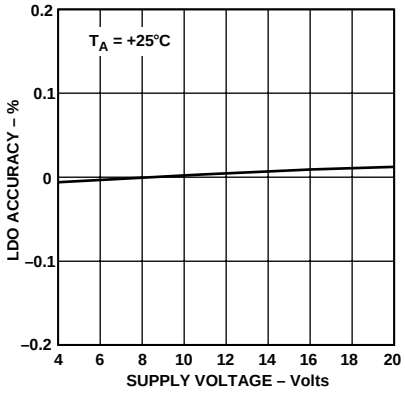


Figure 10. LDO Accuracy vs. Supply Voltage

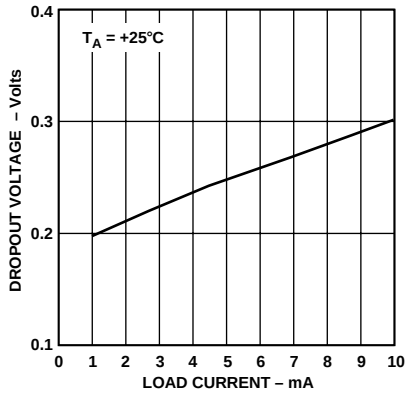


Figure 11. LDO Dropout Voltage vs. Load Current

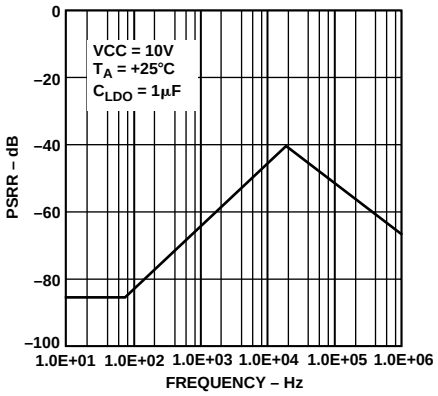


Figure 12. LDO PSRR vs. Frequency

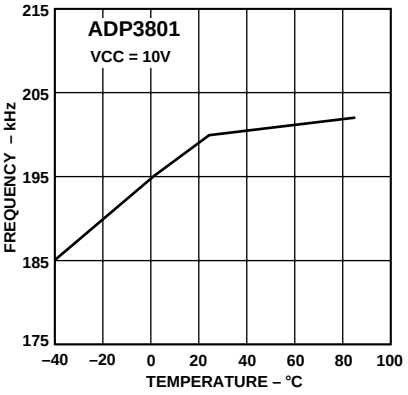


Figure 13. Oscillator Frequency vs. Temperature

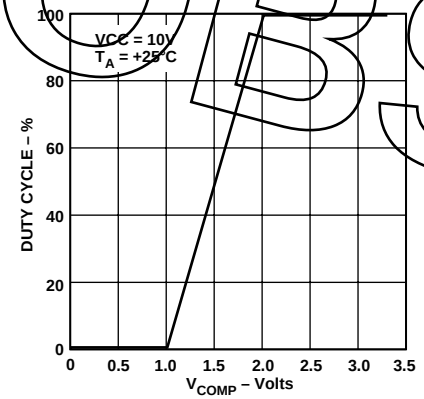


Figure 14. Duty Cycle vs. COMP Pin Voltage

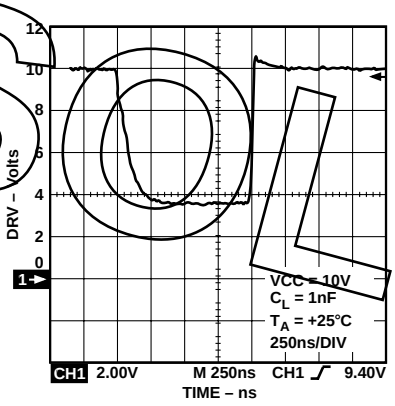


Figure 15. DRV Rise and Fall Times

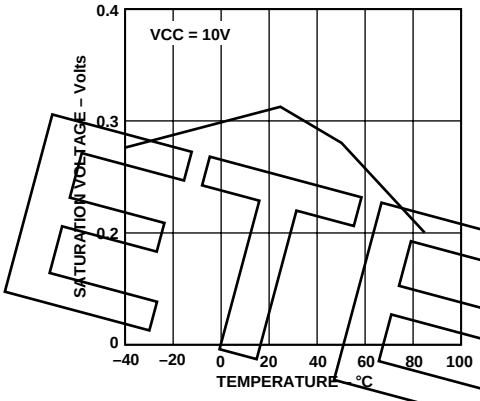


Figure 16. DRV High Saturation Voltage vs. Temperature

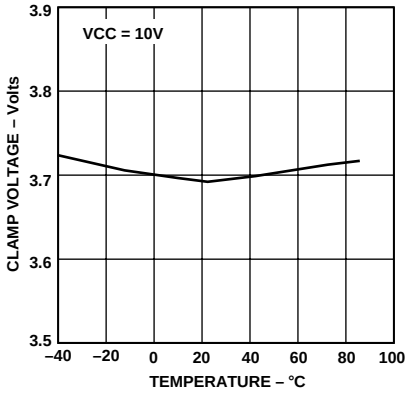


Figure 17. DRV Output Low Voltage with VCC = 10 V vs. Temperature

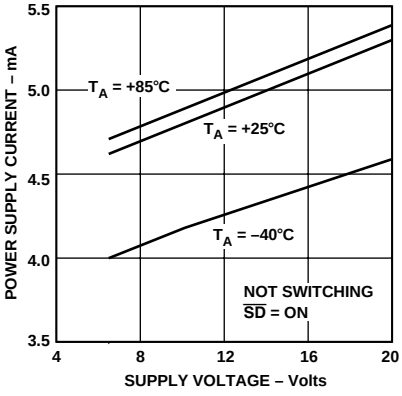


Figure 18. Power Supply Current vs. Supply Voltage @ Three Temperatures

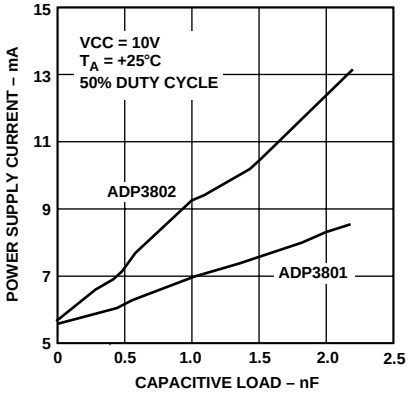


Figure 19. Power Supply Current vs. Capacitive Load on DRV

APPLICATIONS SECTION

PRODUCT DESCRIPTION

The ADP3801 and ADP3802 are complete Li-Ion battery charging ICs. Combined with a microcontroller, they also function as voltage limited, µC programmable constant current source chargers for NiCad and NiMH chemistries. Utilizing an external PMOS pass transistor, the devices realize a buck type constant current, constant voltage (CCCV) charger controller that is capable of charging two separate battery packs for such applications as portable computer chargers and cellular phone chargers. The Functional Block Diagram shows the ICs' functional blocks, which are detailed below:

- A/B SELECT MUX—Two-channel multiplexer for charging two battery stacks.
- FINAL BATTERY VOLTAGE PROGRAM—Multiplexer to program 4.2 V, 8.4 V, or 12.6 V final battery voltage.
- VOLTAGE LOOP AMP—GM-type amplifier to control the final battery voltage. It includes a built-in overvoltage comparator.
- $\overline{\text{EOC}}$ COMPARATOR—End-of-charge detection output to signal when the battery is fully charged.
- BATTERY VOLTAGE ADJUST—Amplifier to adjust the final battery voltage up to ±10%.
- CURRENT LOOP AMP—High-side-current-sense amplifier to sense and control the charge current at a programmable level. It includes an overcurrent comparator.
- PWM—Pulsewidth modulator and oscillator (ADP3801-200 kHz, ADP3802-500 kHz).
- GATE DRIVE—Gate drive to control an external pass transistor. It includes a clamp to limit the drive voltage to protect the external PMOS.
- LDO + REFERENCE—3.3 V low dropout regulator to supply an external microcrontroller and for on-chip supply. Includes an internal precision reference (VREF = VL/2).
- SHUTDOWN—Logic input to shut down the charger. The LDO remains on.
- UVLO—Undervoltage lockout circuit to shut down the charger for low supply voltages.
- RESET—Active LOW output to reset external logic on power-up.

During charging, the ADP3801/ADP3802 maintains a constant, programmable charge current. The high side current sense amplifier has low offset allowing the use of a low voltage drop for current sensing: 165 mV for the maximum charge current. The input common-mode range extends from ground to VCC – 2 V ensuring current control over the full charging voltage of the battery, including a short circuit condition. A high impedance dc voltage input (ISET) is provided for programming the charge current over a wide range. When the battery voltage approaches its final limit, the part automatically transfers to voltage control mode. Both the current control loop and the voltage control loop share the same compensation pin minimizing the number of external components. An internal comparator monitors the charge current to detect the end-of-charge ($\overline{\text{EOC}}$). When the current decreases such that $V_{CS} \leq 8$ mV, the $\overline{\text{EOC}}$ output pulls low.

A 3.3 V LDO is used to generate a regulated supply for internal circuitry. Additionally, the LDO can deliver up to 10 mA of current to power external circuitry such as a microcontroller. An Undervoltage Lockout (UVLO) circuit is included to safely shut down the charging circuitry when the input voltage drops below its minimum rating. A shutdown pin is also provided to turn off the charger when, for example, the battery has been fully charged. The LDO remains active during shutdown or UVLO and has a quiescent current of 110 µA.

Battery Charging Overview

Figure 20 shows a simplified Buck type battery charger application circuit for the ADP3801/ADP3802. When a discharged battery is first placed in the charger, the battery voltage is well below the final charge voltage, so the current sense amplifier controls the charge loop in constant current mode. The charge current creates a voltage drop across the sense resistor R_{CS}. This voltage drop is buffered and amplified by amplifier GM1. Amplifier GM2 compares the output of GM1 to an external current control voltage provided at the ISET pin and servos the charger loop to make these voltages equal. Thus, the charge current is programmed using the ISET input voltage.

The output of GM2 is analog "OR'ed" with the output of GM3, the voltage loop amplifier. Only one or the other amplifier controls the charge loop at any given time. As the battery voltage approaches its final voltage, GM3 comes into balance. As this occurs, the charge current decreases, unbalancing GM2, and control of the feedback loop naturally transfers to GM3.

The ADP3801/ADP3802 can control the charging of two independent battery stacks or a single battery stack. The A/B SELECT MUX has a logic input to choose between the two batteries. See Figure 31 for more information on dual battery charging. The output of the multiplexer is applied to a precision thin-film resistor string to divide down the battery voltage. The final battery voltage is chosen by selecting the proper resistor divider tap with the PROG multiplexer. The output of this mux goes directly to the input of GM3, comparing the divided down battery voltage to the internal reference. To guarantee ±0.75% accuracy, a high precision internal reference and high accuracy thin film resistors are used. Including these components on-chip saves the significant cost and design effort of adding them externally.

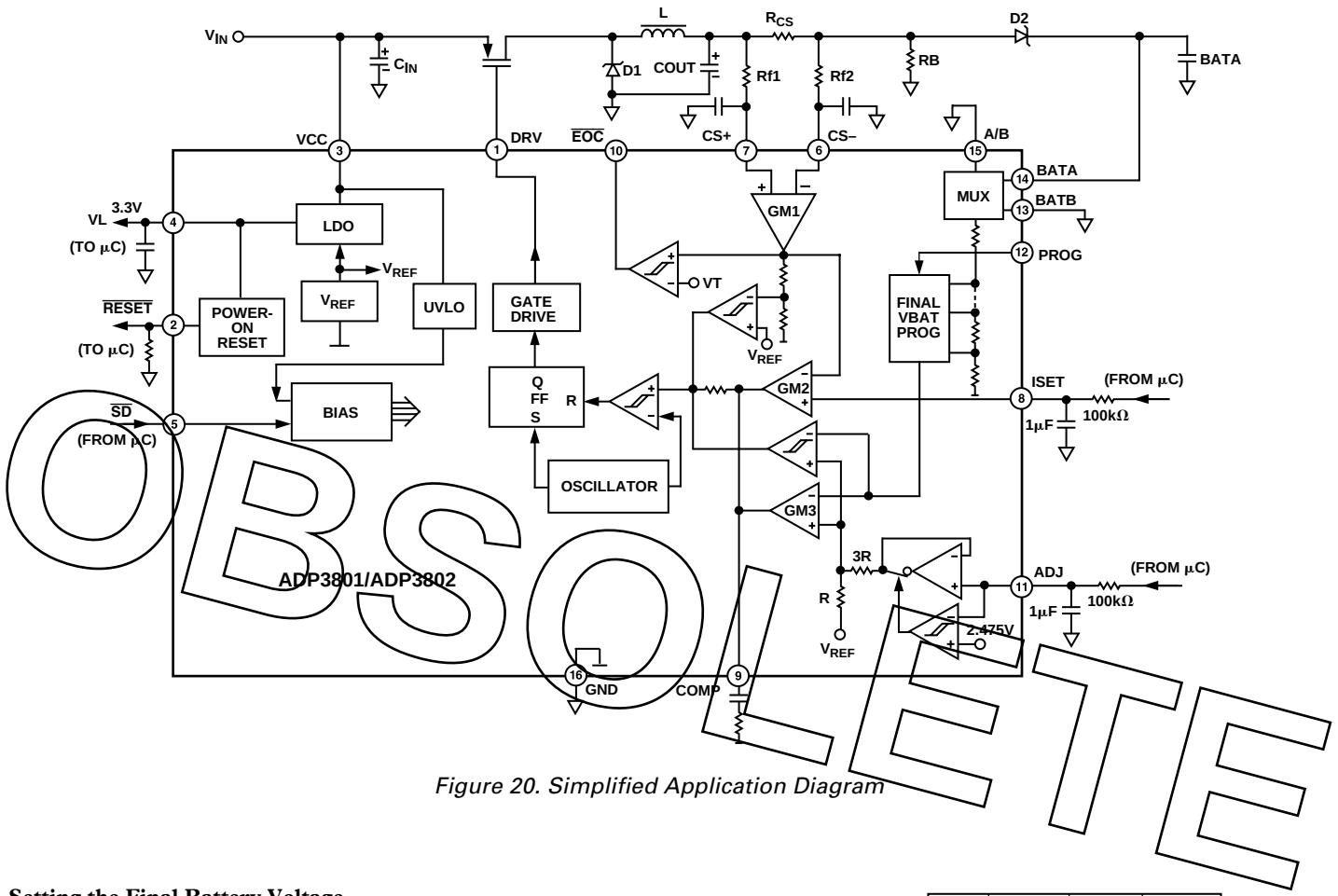
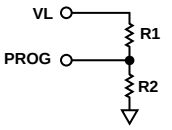


Figure 20. Simplified Application Diagram

Setting the Final Battery Voltage

The final battery voltage is determined by the voltage on the Battery Programming (PROG) pin. This pin controls the state of the PROG multiplexer, which selects the appropriate tap from the internal battery voltage resistor divider. The specification table details the PROG voltages for each final battery voltage. A resistor divider from the LDO can be used to set the PROG voltage as shown in Figure 21. To provide fail safe operation, a PROG voltage equal to 0.0 V or 3.3 V results in the minimum final battery voltage of 4.2 V. The PROG input is high impedance, so the voltage can be set with a high impedance resistor divider from VL. Alternatively, a PWM output from a microcontroller can be used with an RC filter to generate the desired threshold voltage.



V_{BAT}	SETTING	R1 (5%)	R2 (5%)
4.2	V_{T1} = 0.0V	∞	0*
8.4	V_{T2} = 1.1V	200kΩ	100kΩ
12.6	V_{T3} = 2.2V	100kΩ	200kΩ

*CONNECT PROG TO GND FOR V_{BAT} = 4.2V

Figure 21. Resistor Divider Sets the Final Battery Voltage

Adjusting the Final Battery Voltage

In addition to the PROG input, the ADP3801/ADP3802 provides an input (ADJ) for fine adjustment of the final battery voltage. For example, the ADJ amplifier allows the nominal 4.2 V per cell setting for Li-Ion battery cells to be adjusted to 4.1 V for certain chemistries. An internal amplifier buffers the ADJ pin and adjusts the internal reference voltage on the input to GM3. Figure 5 shows a graph of the percent change in final battery voltage vs. the ADJ voltage. The linear portion between 0.6 V_{REF} and 1.4 V_{REF} follows the formula below:

$$\Delta V_{BAT}(\%) = \frac{V_{ADJ} - V_{REF}}{4\,V_{REF}} \times 100$$

The factor of four in the denominator is due to internal scaling. When V_{ADJ} is above 2.5 V, an internal comparator switches off the ADJ amplifier, giving a 0% change in V_{BAT}. Whenever the ADJ function is not used it should be connected to VL.

The total range of adjustment is ±10%. For example, the 4.2 V final battery voltage setting can be adjusted from 3.78 V to 4.62 V. Of course, care must be taken not to adjust the final battery voltage to an unsafe charging level for Li-Ion batteries. Follow the battery manufacturers specifications for the appropriate final battery voltage. Never charge a Li-Ion battery above the manufacturers rated maximum!

Voltage Loop Accuracy

The ADP3801/ADP3802 guarantees that the battery voltage be within ±0.75% of the setpoint over the specified temperature range and the specified charge current range. This inclusive specification saves the designer the time and expense of having to design-in additional high accuracy components such as a reference and precision resistors.

To maintain the ±0.75% specification, the layout and design of the external circuitry must be considered. The input impedance of BATA and BATB is typically 265 kΩ, so any additional impedance on these inputs will cause an error. As a result, do not add external resistors to the battery inputs. Furthermore, if the output voltage is being used for other purposes, such as to supply additional circuitry, the current to this circuitry should be routed separately from the sense lines to prevent voltage drops due to impedance of the PC-board traces. In general, route the sense lines as Kelvin connections as close to the positive terminals of the battery as possible.

The same care must be given to the ground connection for the ADP3801/ADP3802. Any voltage difference between the battery ground and the GND pin will cause an error in the charge voltage. This error includes the voltage drop due to the ground current of the part. Thus, the GND pin should have a thick trace or ground plane connected as close as possible to the battery's negative terminal. Any current from additional circuitry should be routed separately to the supply return and not share a trace with the GND pin.

Dual Battery Operation

The ADP3801/ADP3802 is designed to charge two separate battery packs. These batteries can be of different chemistries and have a different number of cells. At any given time, only one of the two batteries is being charged. To select which battery is being monitored, and therefore which battery is being charged, the ADP3801/ADP3802 includes a battery selector mux. This two-channel mux is designed to be "break-before-make" to ensure that the two batteries are not shorted together momentarily when switching from one to the other. The A/B input is a standard logic input, with a logic low selecting BATA and a logic high selecting BATB. See the application in Figure 31 for more information.

Overvoltage Comparator

GM3 includes an overvoltage comparator. Its output bypasses the COMP node to quickly reduce the duty cycle of the PWM to 0% when an overvoltage event occurs. A second output is connected to the COMP node and, with slower response, reduces the voltage on the COMP cap to provide a soft start recovery. The threshold of the comparator is typically 8% above the final battery voltage. This comparator protects external circuitry from any condition that causes the output voltage to quickly increase. The most likely reason is if the battery is suddenly removed while it is being charged with high current. Figure 27 shows the transient response when the battery is removed. Notice that the output voltage increases to the comparator trip point, but it is quickly brought under control and held at the final battery voltage.

Current Sense Amplifier

A differential, high side current sense amplifier (GM1 in Figure 20) amplifies the voltage drop across a current sense resistor R_{CS}. The input common-mode range of GM1 extends from ground to VCC – 2 V. Sensing to ground ensures current regulation even in short circuit conditions. To stay within the common-mode range of GM1, VCC must be at least 2 V greater than the final battery voltage or a circuit such as shown in Figure 32 must be used. RC filters are included to filter out high frequency transients, which could saturate the internal circuitry. The filter's cutoff is typically set at half the switching frequency of the oscillator.

The charge current is controlled by the voltage on the ISET pin according to the following formula:

$$I_{CHARGE} = \frac{V_{ISET}}{10 \times R_{CS}}$$

The factor of 10 is due the GM1's gain of 10 V/V. To set a charge current of 1.5 A with R_{CS} = 0.1 Ω, V_{ISET} must be 1.5 V. Figure 22 shows the linearity of the charge current control as the voltage is increased from 0 V to the programmed final battery voltage (12.6 V in this case). It is important to state that this curve is taken with an ideal, zero impedance load. An actual Li-Ion battery will exhibit a more gradual drop in charge current due to the internal impedance of the battery as shown in Figure 25.

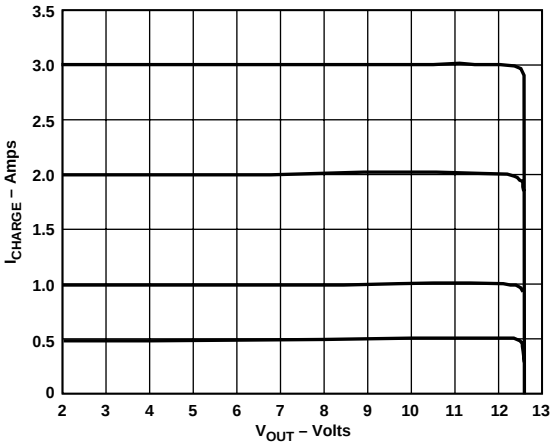


Figure 22. CCCV Characteristic with Ideal Load

Overcurrent Comparator

Similar to the voltage loop, the current loop includes a comparator to protect the external circuitry from an overcurrent event. This comparator trips when GM1's differential input voltage exceeds 185 mV. Like the overvoltage comparator, it has two outputs to quickly reduce the duty cycle to 0% and to provide a soft-start recovery. The response time of the internal comparator is approximately 1 µs; however, the filter on the input of GM1 may slow down the total response time of the loop.

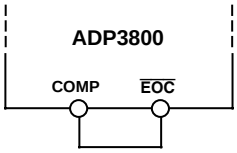
End-of-Charge Output

The ADP3801/ADP3802 provides an active low, end-of-charge ($\overline{EOC}$) logic output to signal when the battery has completed charging. The typical Li-Ion charging characteristic in Figure 25 shows that when the battery reaches its final voltage the current decreases. To determine $\overline{EOC}$, an internal comparator senses when the current falls below 6% of full scale, ensuring that the battery has been fully charged. The comparator has hysteresis to prevent oscillation around the trip point.

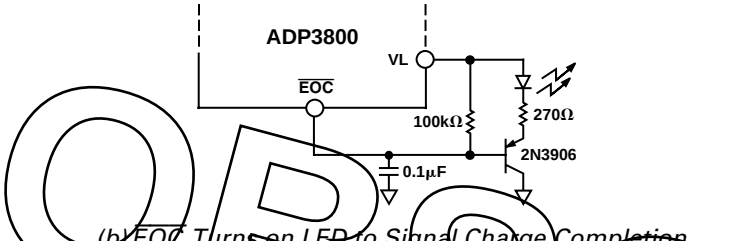
To prevent false triggering (such as during soft-start), the comparator is only enabled when the battery voltage is within 5% of its final voltage. As the battery is charging up, the comparator will not go low even if the current falls below 6% as long as the battery voltage is below 95% of full scale. Once the battery has risen above 95%, the comparator is enabled.

There are two important reasons for this functionality. First, when the circuit is initially powered on, the charge current is zero because of the soft start. If the comparator is not gated by the battery voltage, then $\overline{EOC}$ would go low erroneously. Second, a provision must be made for battery discharge. Assume that a battery has been fully charged. $\overline{EOC}$ goes low, and the charger is gated off. When the battery voltage falls to 95%, due to self-discharge for example, $\overline{EOC}$ will return high. Then the charger can start up and top off the battery, preventing the battery from "floating" at the end-of-charge voltage.

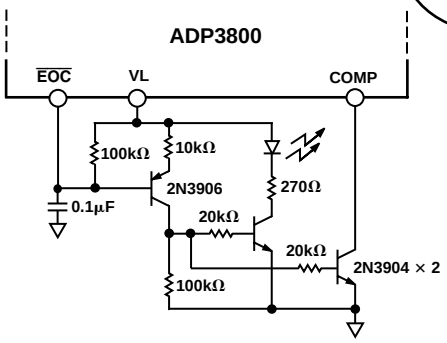
The $\overline{EOC}$ output has many possible uses as shown in Figure 23. One simple function is to terminate the charging to prevent floating (Figure 23a). It can be used as a logic signal to a microcontroller to indicate that the battery has finished charging. The microcontroller can then switch to the next battery if appropriate or shutdown the ADP3801/ADP3802. It can also be used to turn on an LED to signal charge completion (Figure 23b). Using a flip-flop, $\overline{EOC}$ can control the switching from BATA to BATB (Figure 23d). The RC filter delays switching between the two batteries to ensure that the output capacitor is discharged.



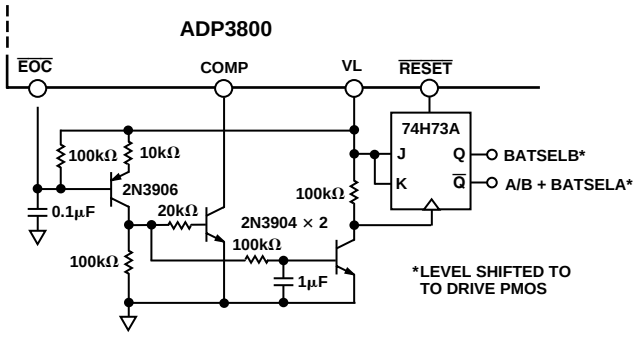
(a) $\overline{EOC}$ Output Terminates Charge



(b) $\overline{EOC}$ Turns on LED to Signal Charge Completion



(c) $\overline{EOC}$ Terminates Charge and Turns on LED



(d) Flip-Flop Switches Between Batteries on $\overline{EOC}$ Signal

Figure 23. $\overline{EOC}$ Output Circuits

COMP Node

Both the current loop and the voltage loop share a common, high impedance compensation node, labeled COMP. A series capacitor and resistor on this node help to compensate both loops. The resistor is included to provide a zero in the loop response and boost phase margin.

The voltage at the COMP node determines the duty cycle of the PWM. The threshold levels are typically 1.0 V for 0% duty cycle and 2.0 V for 100% duty cycle, resulting in a total range of 1.0 V. When the ADP3801/ADP3802 first turns on, the COMP capacitor is at 0.0 V. It has to charge up to at least 1.0 V before the duty cycle rises above 0% and the pass transistor turns on. This "soft-start" behavior is desirable to avoid undue stress on the external components. In addition, whenever the part is placed in Shutdown or in UVLO, the COMP capacitor is discharged to ensure soft start upon recovery.

The current available to charge and discharge the COMP capacitor during normal operation is 100 µA. Thus, the slew rate at this node is equal to 100 µA divided by the capacitor. For a typical capacitance of 1 µF, the slew rate is 0.1 V/ms. Thus, it takes about 10 ms before the ADP3801/ADP3802 starts to operate from a soft-start state. This is regardless of the internal oscillator frequency. One important note is that the COMP node is a high impedance point. Any external resistance or leakage current on this node will cause an error in both the charge current control and the final battery voltage.

Gate Drive

The ADP3801/ADP3802 gate drive is designed to provide high transient currents to drive the pass transistor. The rise and fall times are typically 20 ns and 200 ns respectively when driving a 1 nF load, which is typical for a PMOSFET with $R_{DS(ON)}$ = 60 mΩ. Figure 15 shows the typical transient response of the output stage driving this load from a 10 V supply.

A voltage clamp is added to limit the pull-down voltage to 7 V below VCC. For example, if VCC is 10 V then the output will pull down to 3 V minimum, limiting the V_{GS} voltage applied to the external FET.

Low Dropout Regulator and Reference

A 3.3 V LDO is used to generate a regulated supply for internal circuitry. Additionally, the LDO can deliver up to 10 mA of current to power external circuitry such as a microcontroller. A 1.0 µF capacitor must be placed close to the VL pin to ensure stability of the regulator. Due to the design of the regulator, stability is not contingent on the ESR for the output capacitor. Many different types of capacitors can be used providing flexibility and ease of design. The LDO also includes a high accuracy, low drift internal reference equal to half of VL to set levels within the part. During shutdown and UVLO, both the reference and the LDO remain active.

Shutdown

The IC may be placed in shutdown at any time to stop charging of the batteries and to conserve power. For example, to safely switch from one battery to the next, the part should be shut down to momentarily interrupt charging. Also, if the batteries have completed charging or no batteries are present, then the part may be placed in shutdown to save power. A logic low on

$\overline{SD}$ results in shutdown. All internal circuitry is shut off except for the LDO and the reference, and the supply current is typically 110 μA. When $\overline{SD}$ returns high, the part resumes full operation. The compensation capacitor at the COMP node is discharged during shutdown, so the part will resume operation in soft-start mode.

Undervoltage Lockout—UVLO

The internal Undervoltage Lockout (UVLO) circuit monitors the input voltage and keeps the part in shut-down mode until VCC rises above 3.9 V. During UVLO, the LDO and reference are still active, but the analog front end, the oscillator, and the gate drive are off. UVLO helps to prevent the circuitry from entering an unknown state that could incorrectly charge a battery.

To prevent oscillation around VCC = 3.9 V, the UVLO circuitry has built-in hysteresis. Once the part is on, the UVLO circuitry does not shut it off until the LDO enters dropout. Because the dropout voltage depends on the LDO's load, the UVLO trip point-off also depends on the load. Refer to Figure 8 for a graph of the UVLO trip point-off versus LDO load.

$\overline{RESET}$

When the power is first applied to the ADP3801/ADP3802, the $\overline{RESET}$ pin is held at ground by an external 1 MΩ resistor. It remains low until the LDO output voltage rises to above 80% of its final value. When this threshold is reached, the $\overline{RESET}$ pin is pulled high. The internal $\overline{RESET}$ comparator includes about 150 mV of hysteresis to avoid oscillation around the threshold.

Supply Considerations

The guaranteed operating supply voltage range of the ADP3801/ADP3802 is from 4 V to 20 V, and it typically consumes 5.0 mA of quiescent current when not switching. However, the part needs at least 2 V of headroom between VCC and the voltage on the CS+ and CS– pins. This is for the common-mode range on the current sense amplifier. In applications where the input supply does not offer enough headroom, the circuits in Figures 32 and 33 can be used as explained in the section on low overhead charging.

Overtemperature Shutdown

The ADP3801/ADP3802 has an on-chip temperature detector to shut the part down when the die temperature reaches typically +160°C. Such a condition could occur with a short-circuit on the LDO or a short on the DRV pin. In either case, the operation of the charger will stop and the DRV pin will be pulled high. With approximately +10°C hysteresis, the overtemperature shutdown releases at typically +150°C. These temperatures are higher than the absolute maximum ratings for the die, and are included as a safety feature only.

Li-Ion Battery Charger

The ADP3801 and ADP3802 are ideally suited for a single or dual Li-Ion batterypack charger. They combine 200 kHz or 500 kHz switching with a PMOS pass transistor drive to realize a Buck topology CCCV charger. The following discussion goes through the complete design of a charger using the ADP3801. This information also applies to the ADP3802.

Charger Specifications

Battery: 3 Series Cell Li-Ion Pack.
Input Voltage: V_{IN} = 15 V dc to 20 V dc.
Final Battery Voltage: V_{BAT} = 12.6 V.
Charge Current: I_{CHARGE} = 4.0 A (for V_O = 0 V to 12.6 V)

Circuit Topology

The complete Buck charger circuit is shown in Figure 24. The dc-source voltage can be supplied from an ac/dc adaptor or an external dc/dc supply.

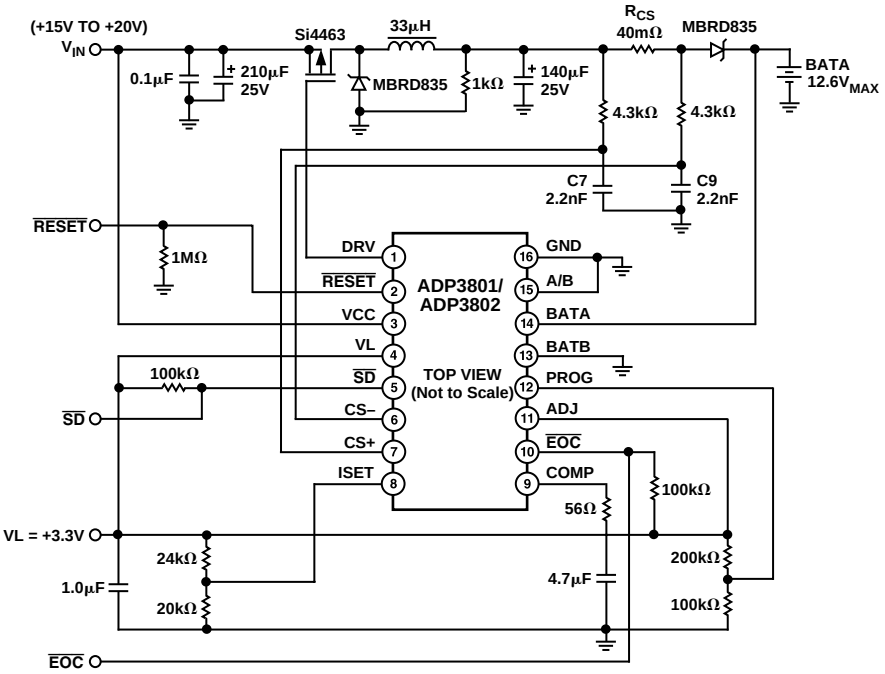


Figure 24. Li-Ion Battery Charger

Current Sense

The maximum charging current is specified by the battery manufacturer as 4.0 A. To avoid losing excessive power on the current-sense resistor, it is advisable to keep the voltage drop across the resistor at maximum current to 160 mV or below. Thus, R_{CS} = 0.16 V/4 A = 40 mΩ. The resistor's maximum power rating can be calculated using the data sheet specification for the Overcurrent Comparator. The overcurrent protection is specified at 4.9 A when using a 40 mΩ resistor; therefore, the resistor has to be rated at $P_R = (4.9)^2 \times 0.04 = 0.96$ W. Thus a 1.0 W or higher power rated resistor should be used. Two 2.2 nF capacitors are connected from the CS+ and CS– inputs to ground to filter out high frequency switching noise.

ISET Programming Voltage

This voltage programs the charge current based on the above calculated R_{CS}. Using the data sheet specification for the current programming at the ISET input of 0.1 V/V, we need:

$$V_{ISET} = \frac{R_{CS} \times I_{CHARGE}}{0.1 V/V} = \frac{0.04\,\Omega \times 4.0\,A}{0.1 V/V} = 1.6\,V$$

The 1.6 V can be obtained from the 3.3 V LDO by a resistor divider of 20 kΩ and 22 kΩ.

PROG Voltage

Next, the PROG voltage has to be determined to set the proper final battery voltage. From the data sheet, V_{PROG} for two Li-Ion batteries in series (12.6 V) is between 2.05 V and 2.3 V. A 2.2 V input can be obtained from the 3.3 V LDO by a resistor divider of 66.5 kΩ and 33.2 kΩ.

ADJ Voltage

Since no further adjustment of the final battery voltage is required, this pin is tied to the VL pin, which disables the internal amplifier.

Output Voltage and Duty Cycle

A Buck type of converter's output voltage V_O can be calculated as follows:

$$V_O = \frac{V_{IN} \times D}{100} = \frac{V_{IN} \times T_{ON}}{100 \times T}$$

In the above equation, D is the maximum duty cycle of the converter in percentage, and T_{ON} and T are the ON time and total period respectively. Setting V_{INMIN} = 15 V provides margin for external voltage drops and the common-mode input range of the current sense amplifier.

For $V_{IN} = 11\,V$: $D_{MAX} = V_O \times 100 / V_{IN} = 12.6 \times 100 / 15 = 84\%$

For $V_{IN} = 20\,V$: $D_{MAX} = V_O \times 100 / V_{IN} = 12.6 \times 100 / 20 = 63\%$

Buck Inductor

The inductor value can be calculated after determining the allowable amount of inductor ripple current. For continuous buck operation, and considering low cost inductor core materials and acceptable core losses at 200 kHz, the usual peak-to-peak inductor ripple current (I_{RPP}) used is 20%-40% of the maximum dc current. Using 25% of 4.0 A_{DC} gives I_{RPP} = 1.0 A_{PP}.

The maximum off-time of the Buck switch (T_{OFFMAX}) occurs at the maximum input voltage of 20 V:

$$T_{OFFMAX} = \frac{100 - D_{MAX}}{f_{OSC} \times 100} = \frac{100 - 63}{200\,kHz \times 100} = 1.9\,\mu s$$

This gives an inductor value of:

$$L > \frac{V_{OMAX} \times T_{OFFMAX}}{I_{RPP}} = \frac{12.6\,V \times 1.9\,\mu s}{1.0\,A} = 24\,\mu H$$

The max inductor peak current is calculated as follows:

$$I_{LPEAK} = I_{DC} + I_{RPP}/2 = 4.0 + 1.0/2 = 4.5\,A_{PEAK}$$

The max inductor rms current is calculated (where 0.577 is the conversion factor for a peak to RMS value):

$$I_{LRMS} = \frac{0.577 \times 0.5 \times V_O \times T_{OFF}}{L} = \frac{0.577 \times 0.5 \times 12.6 \times 1.9\,\mu s}{24\,\mu H} = 0.3\,A$$

An appropriate inductor is the Coiltronix UP4B330, which is specified at 33 µH and can carry the 4.5 A current with about a 20°C temperature rise. For the ADP3802, the above formulas give: T_{OFFMAX} = 0.74 µs and L = 10 µH.

PFET Selection and Thermal Design

We have to consult the available P-channel MOSFET (PFET) transistor selection charts for switch-mode power supply applications to find a PFET in the desired package whose Safe Operation Area (SOA) would meet the maximum V_{IN} and I_O requirements with acceptable margin. For this application, the Temic Si4463 was selected in an SO-8 package. This transistor is specified at V_{DSS} = –20 V, V_{GSMAX} = 12 V, $R_{DS(ON)}$ = 0.013 Ω (for V_{GS} = 4.5 V), and I_{DMAX} = 10 A. Its SOA covers the 20 V, 4.0 A_{DC}, and 4.5 A_{PEAK} application requirements with adequate margin.

Since the switching losses are negligible for properly driven PFETs compared to conduction losses, the worst-case conduction losses can be estimated from the worst case ON resistance ($R_{DS(ON)}$) of the selected PFET when subjected to short circuit current at the minimum input voltage and close to 100% duty cycle. $R_{DS(ON)}$ increases about 50% at T_J = 150°C. Thus the worst case value we can use is 0.023 Ω. The maximum PFET dissipation is calculated as follows:

$$P_{DMAX} = I_{PEAK}^2 \times R_{DS(ON)} = 4.5\,A^2 \times 0.023\,\Omega = 0.47\,W$$

Next the maximum junction temperature T_{JMAX} of the transistor can be calculated:

$$T_{JMAX} = T_A + (R_{\theta JA}) \times P_{DMAX} = 50 + (50) \times 0.47 = 74°C$$

where T_A = 50°C and $R_{\theta JA}$ = 50°C/W, as specified on the transistor's data sheet for a 1 inch square PCB-pad. The calculated T_{JMAX} should be below the maximum allowed junction temperature of the transistor with adequate margin. The Si4463 specifies a T_{JMAX} of 150°C, which we meet with more than adequate margin.

Gate Drive

The ADP3801 and ADP3802 are designed to directly drive the gate of a PFET with no additional circuitry as shown on the circuit diagram. The DRV pin pulls the gate up to within 250 mV of VCC, which is more than enough to ensure that the transistor turns off. To turn the PFET on, the DRV pin pulls down to a clamped voltage that is at most 7 V below VCC. Check the specified PFET's maximum Gate-Source rating to see if this voltage does not exceed its breakdown. The Si4463 is rated at V_{GSMAX} = 12 V, which is well above the maximum gate drive for the ADP3801/ADP3802.

Schottky Rectifier Selection and Thermal Design

The Schottky diode's peak current and average power dissipation must not exceed the diode ratings. The most stressful condition for the output diode is under short circuit (V_O = 0 V), where the diode duty cycle D_D is at least 95%. Under this condition, the diode must safely handle I_{PK} at close to 100% duty cycle.

The diode power dissipation (P_D) is calculated by multiplying the forward voltage drop (V_F) times the Schottky diode duty cycle multiplied by the short circuit current. The worst-case forward voltage drop of MBRD835 diode is 0.41 V at I_{PK} = 4.5 A, thus:

$$P_D = I_{PK} \times D_D \times V_F = 4.5 \times 0.95 \times 0.41 = 1.8W$$

From the diode's worst-case dissipation, the maximum junction temperature T_{JMAX} of the diode can be calculated:

$$T_{JMAX} = T_A + R_{\theta JA} \times P_D = 25 + (40) \times 1.8 = 97°C$$

$R_{\theta JA}$ is the junction to ambient thermal impedance of the diode. The calculated T_{JMAX} should be below the maximum allowed junction temperature of the diode with adequate margin. T_{JMAX} of the MBRD835 is 125°C, which is met with adequate margin.

Input Capacitor Selection

In continuous mode, the source current of the PMOS is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum rms current must be used. The maximum rms capacitor current is given by:

$$I_{RMS} \approx \frac{I_{OUT}}{V_{IN}} \times \sqrt{V_{OUT}\left(V_{IN} - V_{OUT}\right)}$$

This formula has a maximum at $V_{IN} = 2\ V_{OUT}$, where $I_{RMS} = I_{OUT}/2$ = 2.0 A.

This simple worst case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. As a first choice, three 68 µF/20 V Sprague type 593D tantalum capacitors are used in parallel. Each is specified as follows: ESR = 0.2 Ω, maximum ripple current of 0.91A_{RMS}. In addition to C_{IN}, a 0.1 µF decoupling capacitor is required as close as possible to the VCC pin.

Once the capacitor is chosen, the input ripple voltage should be checked:

$$V_{INRIPPLE} = I_O \times \left[ESR + \frac{D_{ON}/100}{f_{OSC} \times C_{IN}}\right] = 4.0\ A \times \left[0.07\ \Omega + \frac{84/100}{200\ kHz \times 210\ \mu F}\right] = 360\ mV_{PP}$$

This is low enough for most applications. For cost reduction, one of the 68 µF capacitors could be removed, or a cheaper electrolytic could be used instead.

Output Capacitor Selection

As a first choice, we'll use two of the same type of 68 µF Sprague capacitors for the output. The inductor rms ripple current was calculated as 0.3 A, which is far below the specification for these capacitors. The other consideration is the allowable output ripple voltage. Assuming high battery internal resistance, all of the worst case inductor ripple current may flow through the output capacitor. This results in a ripple voltage of:

$$V_{OUTRIPPLE} = I_{LPP} \times \left[ESR + \frac{D_{ON}/100}{f_{OSC} \times C_{OUT}}\right] = 1.0\ A \times \left[0.1\ \Omega + \frac{84/100}{200\ kHz \times 140\ \mu F}\right] = 130\ mV_{PP}$$

This ripple is low enough for most applications. Again, one of the capacitors could be removed or lower cost electrolytic capacitors could be used to reduce cost.

Charger Performance Summary

The circuit properly executes the charging algorithm, exhibiting stable operation regardless of battery conditions, including an open circuit load in which the battery is removed.

Li-Ion charging characteristics are given in Figure 25. The charge current is maintained at its programmed level until the battery reaches its final voltage. Then the current begins to decrease. The shape of the current decrease is dependent on the internal impedance of the battery. When the current drops below 240 mA, the $\overline{EOC}$ comparator signals the end-of-charge of the battery.

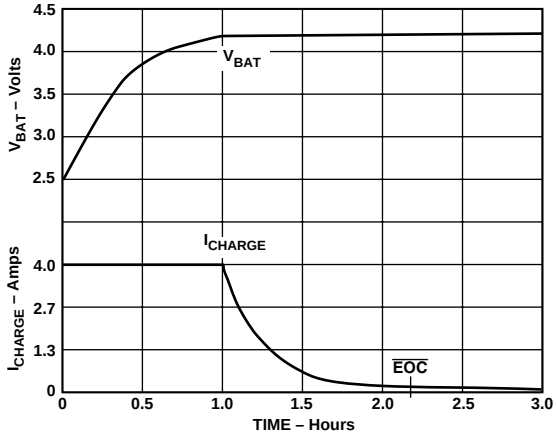


Figure 25. Li-Ion Charging Characteristic

The efficiency of this circuit is shown in Figure 26 for a charge current of 4 Amps. As expected, the efficiency increases with the output voltage, up to a maximum of 92% at 12.6 V.

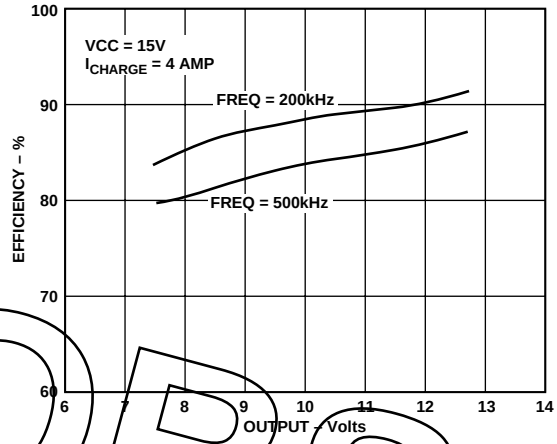


Figure 26. Efficiency for I_{CHARGE} = 4.0 Amp

Figure 27 shows the output voltage transient when a battery load is snapped off. The output is charging a battery (which is currently discharged to 5 V) at 4.0 A when the battery is removed. The high charge current causes the output voltage to quickly increase and exceed the final battery voltage. However, the overvoltage comparator quickly controls the output and only a small overshoot results. When the battery is returned to the circuit, VBAT is pulled back down to the battery's voltage.

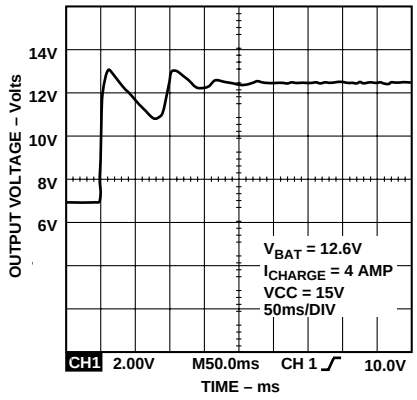


Figure 27. Output Voltage Transient Due to Battery Snap Off

The behavior of the circuit when it is powered on with a dead battery inserted is important to check to make sure that the charger does not exhibit irregular behavior during power-up. In this case, the ADP3801 needs to regulate the output current to 4.0 A. Figure 28 shows the average Si4463 source current under such a condition. When the input power is applied to the charger, the source current ramps up in a controlled manner due to the ADP3801's soft start.

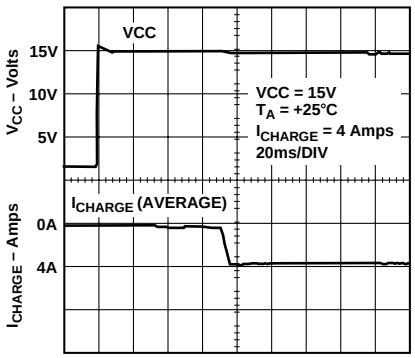
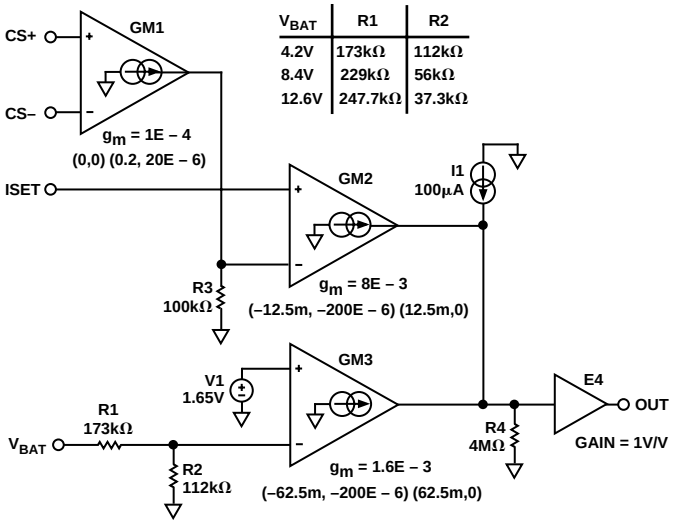


Figure 28. Source Current Due to Input Turn-On

Feedback Loop Compensation Design

The ADP3801 and ADP3802 have two separate feedback loops, the current control loop and the voltage control loop. Each loop must be compensated properly so that the circuit is stable during the entire charging cycle of a battery including the case where no battery is present. A series RC from the COMP pin to ground provides pole/zero compensation for both loops. The circuit in Figure 24 is properly compensated for the ADP3801 and ADP3802 and can be used as is.

Figure 29 shows a typical ac model of the ADP3801/ADP3802. The current loop and voltage loop are comprised of voltage controlled current sources (GM stages). The gains given in the schematic and the impedance at the COMP node are typical values for both the ADP3801 and ADP3802. This model can be used to simulate the small signal ac behavior of the part using a SPICE-based simulator when paired with an ac model of a buck regulator. However, transient and dc behavior is not modeled with this model. The GM stages are actually modeled using the "Table" component in PSpice, which limits the dc levels to ease dc convergence. The coefficients on the schematic give the table coefficients. The input resistors (R1 and R2) are currently set for a 4.2 V final battery voltage. Use the accompanying table to adjust R1 and R2 for the other voltage options. Doing so is important to properly set the voltage loop gain.



V_{BAT}	R1	R2
4.2V	173kΩ	112kΩ
8.4V	229kΩ	56kΩ
12.6V	247.7kΩ	37.3kΩ

Figure 29. AC Behavioral SPICE Model for the ADP3801 and ADP3802

NiCad/NiMH Charging

When paired with a low cost, 8-bit microcontroller, the ADP3801/ADP3802 charges NiCad and NiMH batteries. The ADP3801/ADP3802 is used to provide a programmable charge current limit with a fail-safe voltage limit, and the microcontroller monitors the battery and determines the charge termination. Common methods for termination are "negative delta V" and "delta T." Both methods require that the present value of either the voltage or temperature be compared to a previous value. Such functionality is performed by an µC with an on-board ADC.

The µC and the ADP3801/ADP3802 are configured as shown in Figure 30 for the universal charger. The voltage setting on the ADP3801/ADP3802 should not interfere with normal charging, but still provide a fail safe voltage if the battery is removed. For example, if a 6-cell NiCad battery is being charged, the output voltage of the ADP3801/ADP3802 should be programmed to 12.6 V. The 6-cell battery has a peak voltage of approximately 1.7 V–1.8 V per cell, giving a total voltage of 9.6 V–10.8 V. Thus, the 12.6 V setting provides enough headroom for normal charging.

Universal Battery Charger

The combination of a µC and the ADP3801/ADP3802 can be extended to a low cost universal charger for Li-Ion and NiCad/NiMH as shown in Figure 30. The µC with on-board A/D converter monitors the battery's voltage and temperature to determine the end-of-charge for either NiCad or NiMH batteries. The ADP3801/ADP3802 also monitors the battery voltage to determine the end-of-charge for Li-Ion. The $\overline{EOC}$ output is connected to a digital input on the µC for signaling. The µC can shutdown the charger circuitry when it is not required. The µC shown operates from 3.3 V, so it can be powered directly from the LDO of the ADP3801/ADP3802. The LDO voltage also serves as a 1% reference for the µC's ADC.

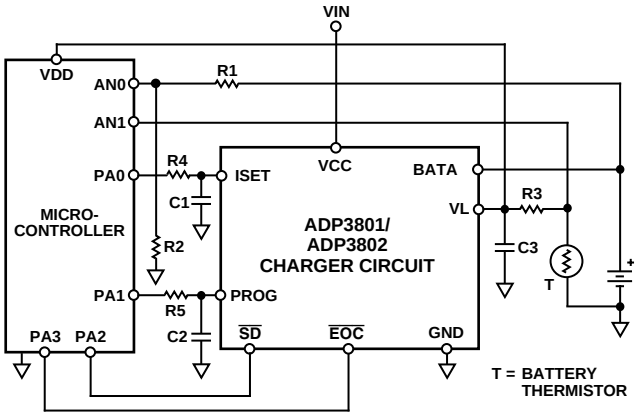


Figure 30. Universal Battery Charger Block Diagram

Both the charge current and the final battery voltage can be dynamically set by using a PWM output from the µC. The PWM inputs to ISET and PROG are filtered by an RC combination to generate a dc voltage on the pins. This functionality allows multiple battery types and chemistries to be accommodated in a single charger circuit.

Dual Li-Ion Battery Charger

Some applications such as certain desktop chargers for cellular phones or laptops with two batteries require that two separate battery stacks be charged independently. The ADP3801/ADP3802 is designed to handle these applications with two battery sense inputs and a multiplexer to select between the two. The application circuit is essentially the same as Figure 24 except that external FETs must be added to direct the charge current to the proper battery stack. Figure 31 shows the additional circuitry needed.

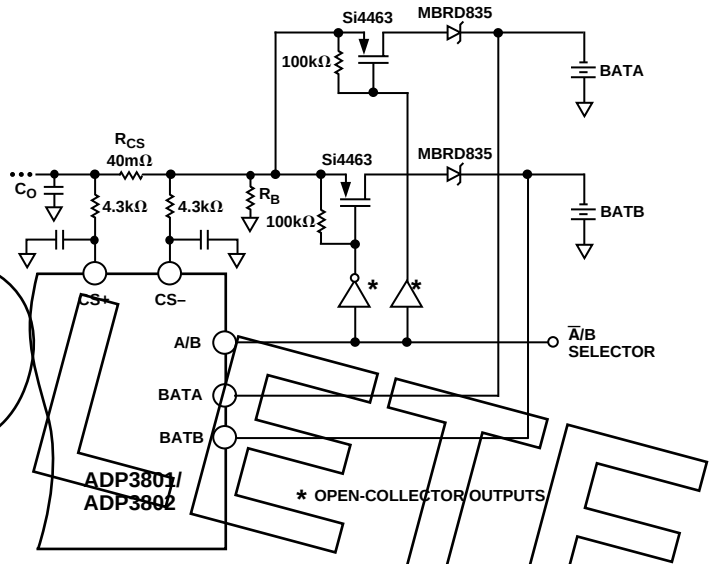


Figure 31. Dual Li-Ion Battery Charger

To provide alternate or sequential charging, the two separate batteries are alternately connected to the output of the charger by two Si4463 PFETs. The control of these FETs is accomplished by open-collector logic outputs and 100 kΩ pull-up resistors. The programming of the A/B terminal should come from a 0 V to 3.3 V logic output. Most likely a dedicated logic circuit or a microcontroller would control the system. The BATB sense input is enabled by connecting a >2 V potential to the A/B input (or <0.8 V to select BATA). The A and B battery voltages are directly sensed by the BATA and BATB inputs.

Two Schottky diodes are also included to prevent one battery stack from shorting to the other through the body diodes of the FETs. When the charger has finished charging one battery (signaled by the $\overline{EOC}$ output), the MUX and external FETs can be switched to charge the second battery. When switching from one battery to the next the following procedure is recommended to minimize transient currents:

1. Turn off the ADP3801/ADP3802 PWM by bringing the $\overline{SD}$ pin low.
2. Turn off the FET to the battery being charged.
3. Wait approximately 60 seconds for C_O to discharge through R_B.
4. Turn on the FET to the second battery.
5. Change the A/B SELECT MUX to the second battery.
6. Turn on the ADP3801/ADP3802 by bringing the $\overline{SD}$ pin high.

The 60 second wait period allows the output capacitor to discharge before switching from one battery to the next. Without this wait period, the capacitor would be fully charged when switched to an uncharged battery. The current under this condition is only limited by the ESR of the capacitor, the ON resistance of the FET and diode, and the series resistance of the battery. These values are typically very small, so current in excess of 5 amps can flow for a short time period. In most practical circuits the wait period is not required, but it is good practice to have it in µC controlled systems. The duration of the wait period is determined by the RC time constant of C_O and R_B and can be adjusted by changing these components.

The two Si4463 switches are turned on by connecting their gates to ground. In a short circuit or overdischarged battery condition, the switches could be operated in their linear region. This may result in high power dissipation and excessive die temperature rise. In µC controlled chargers a simple monitor routine can reduce the charge current if the battery voltage is lower than about 2 V. This should not happen under normal circumstances as the Li-Ion cells are not discharged below 2.5 V/cell.

Low Overhead Charging

For applications where the input supply is less than 2 V higher than the final battery voltage, the circuit of Figure 32 can be used. This circuit adds a resistor divider to the input of the current sense amplifier to increase its common-mode input voltage range. The value of this resistor divider should divide down the battery voltage such that the common-mode voltage at CS+ and CS– is at least 2 V less than the chip's VCC. The formula for the ratio is:

$$\frac{R2}{R1+R2} \le \frac{VCC_{MIN}-2\,V}{VBAT_{MAX}}$$

For example, if VCC_{MIN} = 9 V and $VBAT_{MAX}$ = 8.4 V, then the ratio would be 0.833. To provide some headroom for resistor tolerances and line drops, the actual ratio should be lowered to 0.8. The resistors should be reasonably large to keep the current drain low. Values of R1 = 20 kΩ (0.1%) and R2 = 80 kΩ (0.1%) work well. A diode is added between the current sense resistor and the battery to prevent discharging the battery through these resistors.

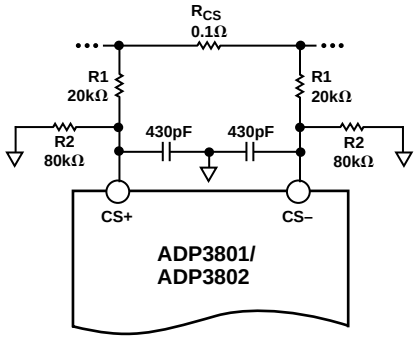


Figure 32. Low Overhead Charging

Because the current sense voltage is divided down by these input resistors, the current sense programming function also changes. Remember to adjust the programming function by the same ratio. In this example, the programming function would become 0.125 V/V. Also, the $\overline{EOC}$ current detection point changes by the same factor.

An alternative to adding the resistor divider is to use a low side current sense. The CS+ and CS– inputs have a common-mode range that extends approximately 300 mV below ground. The circuit in Figure 33 shows how a low side current sense would be configured. The current programming function, $\overline{EOC}$ detection point, and ac performance do not change from the normal configuration.

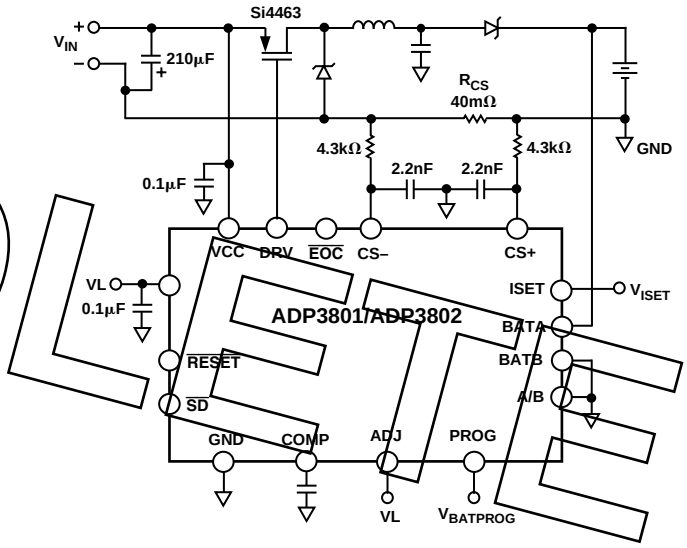


Figure 33. Low Side Current Sensing For Low Overhead Charging

VCC Greater Than 20 V Operation

Some ac/dc adapters have a poorly regulated output voltage that can rise above the 20 V maximum operating voltage of the ADP3801/ADP3802. The circuit in Figure 34 uses a Zener diode and an NPN transistor to extend the ADP3801/ADP3802's maximum input voltage. The Zener should be at least 3 V higher than the final battery voltage to meet the minimum headroom requirements. 3 V is used to account for the V_{BE} drop of the 2N3904 transistor and additional losses in the circuit. If V_{IN} drops below the value of the Zener diode, VCC is no longer regulated and it tracks V_{IN}. If the 2 V of headroom on the current sense pins is not maintained, then the circuits of Figures 32 and 33 can also be used in conjunction with the circuit of Figure 34.

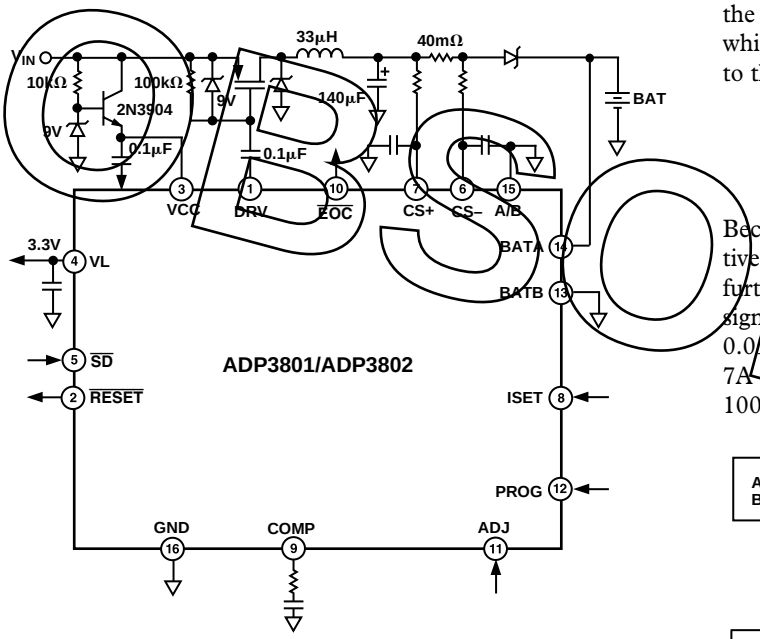


Figure 34. VCC Greater Than 20 V Operation

The gate drive of the PFET is capacitively coupled to the DRV pin with a 0.1 µF capacitor. While the DRV pin is switching, the voltage swing on the DRV pin is coupled to the gate, but the dc voltage is blocked. This allows the gate of the PFET to be at a voltage that is higher than the absolute maximum rating of the DRV pin. The 9 V Zener diode limits the gate drive voltage and the 100 kΩ resistor provides a dc pull-up to turn the PFET off when the DRV pin is not switching.

System Current Sense Reduces Charge Current

In many applications the power required for the system and the battery charger exceeds the total power available from the ac/dc adapter. A design where battery charger current is decreased as the system current increases helps to keep a constant power demand on the brick. Dynamically adjusting the charge current keeps the total power output of the brick constant. The circuit in Figure 35 uses an external low cost amplifier to sense the system current and dynamically control the ADP3801/ADP3802's charge current.

The current setting voltage is produced by R3 and R4 according to the following formula:

$$I_{SET} \approx \frac{1}{10\ R_{CS}} \times \left(\frac{R3}{R3 + R4} \right) VL$$

This equation is approximate because the impedance of R2 and R1 does effect the resistor divider of R3 and R4, but the impact is small. As the system current increases, the voltage across R_{SS} also increases. This voltage is subtracted from V_{ISET} with a gain set by R1 and R2. As the graph in Figure 35 shows, the charge current reduces as the system current increases, and eventually the charge current becomes zero (I_{ZERO}). The system current at which this occurs can be set by selecting R1 and R2 according to the following formula:

$$I_{ZERO} \approx \frac{R1}{R2} \times \left(\frac{10\,R_{CS}}{R_{SS}} \right) \times ISET$$

Because the AD8531 is a single supply amplifier with its negative rail at ground, its output does not go below 0.0 V, so any further increase in system current does not change V_{ISET}. Designing a charger with a maximum charge current of 3A (R_{CS} = 0.05 Ω) which reduces to zero when the system current reaches 7A (R_{SS} = 0.025 Ω) results in the following resistor values: R1 = 100 kΩ, R2 = 820 kΩ, R3 = 8.3 kΩ, R4 = 10 kΩ.

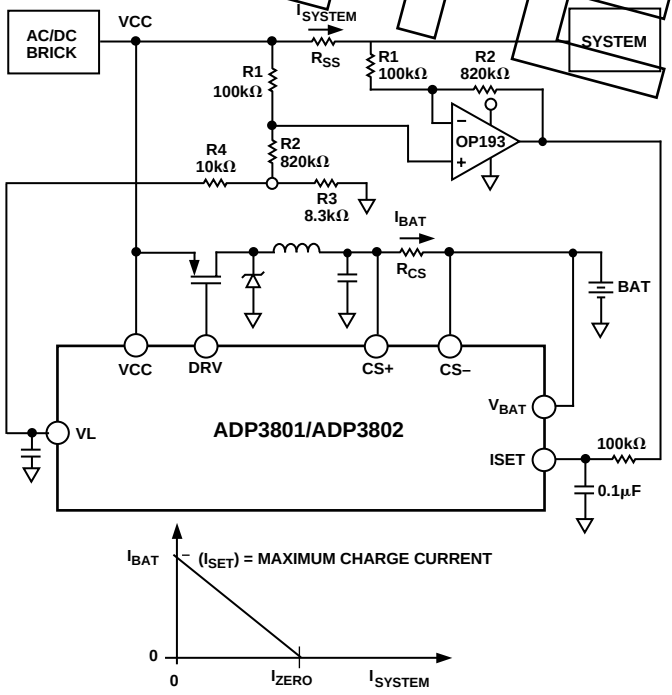


Figure 35. System Current Sense Reduces Charge Current

Board Layout Suggestions

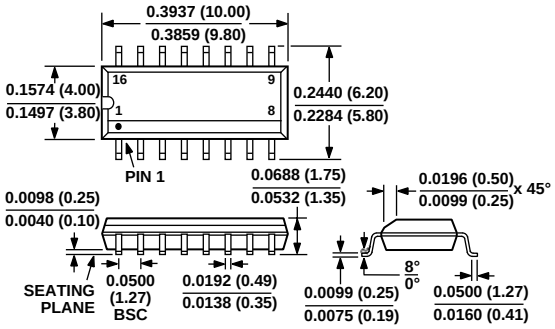
When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the ADP3801 and ADP3802. These items are also illustrated graphically in the layout diagram on the evaluation board application note. Check the following in your layout:

1) The IC ground must return to a) the power and b) the signal grounds with as short of leads as possible. If a double layer PCB board is used and a ground plane is available, connect all grounded parts directly to the ground plane. The ground returns to the anode of the Schottky diode and the minus terminal of C_{IN} should have as short of lead lengths as possible.
2) Connect the IC's current sense pins (CS+ and CS–) to R_{CS} with as short of leads (<0.5 inch) as possible.
3) Route the CS+ and CS– traces together with minimum spacing. The filter capacitors should be close to the IC.
4) Connect the positive side of C_{IN} as close as possible to the source of the P-channel MOSFET (or the emitter of the PNP). This capacitor provides the ac current to the pass transistor.
5) Connect the input decoupling capacitor (0.1 µF) close to the VCC input of the IC. This capacitor carries the DRV peak currents.
6) Connect the 0.1 µF LDO decoupling capacitor as close as possible to the VL pin.
7) The $\overline{\text{RESET}}$ pin has an internal pull-up, and should be pulled low with an external resistor. The $\overline{\text{RESET}}$ pin is high impedance and should not be allowed to float.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Lead Narrow Body (SOIC)
(R-16A)



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