Title	***Engineering Prototype Report for 2.0 W CV Adapter using LinkSwitch™-XT LNK362P***
Specification	85 VAC - 265 VAC Input, 6.2 V, 322 mA Output
Application	Low Cost Adapter
Author	Applications Engineering Department
Document Number	EPR-89
Date	April 26, 2013
Revision	1.1

Summary and Features

- Low cost, low part count solution: requires only 19 components
- Integrated LinkSwitch-XT safety and reliability features:
  - Accurate (± 5%), auto-recovering, hysteretic, thermal shutdown function keeps PCB temperature below safe levels under all conditions
  - Auto-restart protects against output short-circuits and open feedback loops
  - >3.2 mm creepage on IC package enables reliable operation in high humidity and high pollution environments
- *EcoSmart®* – meets all existing and proposed international energy efficiency standards such as China (CECP) / CEC / EPA / AGO / European Commission
  - No-load consumption 110 mW at 265 VAC
  - 61.5 % active-mode efficiency (exceeds CEC requirement of 55.2 %)
- *E-Shield*™ transformer construction and frequency jitter enable this supply to meet EN550022 and CISPR-22 Class B EMI with >10 dBμV of margin
- Meets IEC61000-4-5 Class 3 AC line surge

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Important Note:
Although this board has been designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This engineering report describes a 2.0 W CV, universal input, power supply for applications such as wall adapters. The supply is designed around a LNK362P device, and is intended as a standard evaluation platform for the LinkSwitch-XT family of ICs.

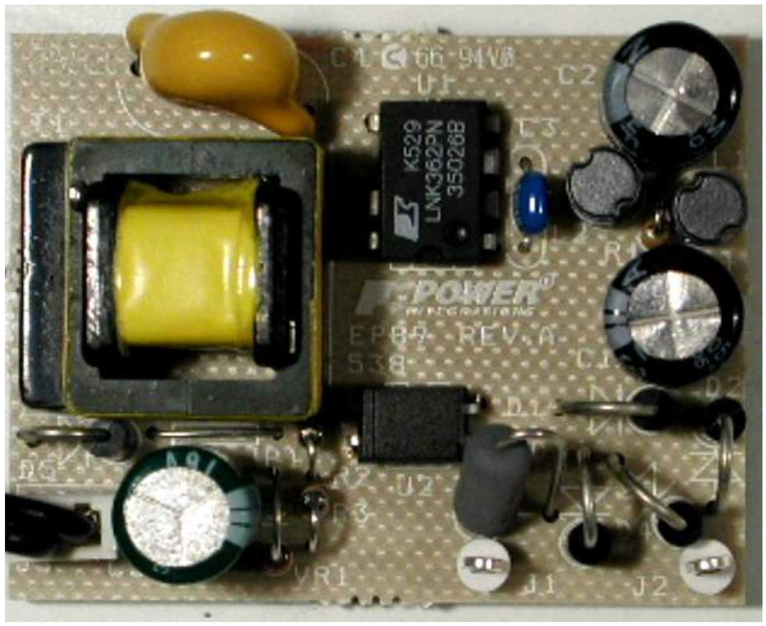

Figure 1 – EP89, LNK362P, 2.0 W, 6.2 V, CV Charger Board Photograph.

The LinkSwitch-XT family has been developed to replace discrete component self-oscillating, ringing choke converters (RCC) and linear regulator-based supplies, in low power adapter applications. The ON/OFF control scheme of the device family achieves very high efficiency over the full load range, as well as very low no-load power consumption. The no-load and active-mode efficiency performance of this supply exceeds all current and proposed energy efficiency standards.

Unlike RCC solutions, the LinkSwitch-XT has intelligent thermal protection built in, eliminating the need for external circuitry. The thermal shutdown has a tight tolerance (142 °C ±5%), a wide hysteresis (75 °C) and recovers automatically once the cause of the over temperature condition is removed. This protects the supply, the load and the user, and typically keeps the average PCB temperature below 100 °C. In contrast, the latching thermal shutdown function typically used in RCC designs usually requires that the AC input power be removed to reset it. Thus, with an RCC, there is fair probability that units may be returned after a thermal latch-off, because the customer is not aware of the reset procedure (unplugging the unit long enough for the input capacitor to discharge). Regardless of the fact that the units being returned are fully functional, this makes the design appear to be less reliable to both the OEM and the end customer, and burdens the power supply manufacturer with the needless handling of perfectly good units through its RMA process.

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On the other hand, an auto-recovering thermal shutdown function eliminates the occurrence of unnecessary returns from the field, since the end customer may never even know that a fault condition existed, because the power supply resumes normal operation once the cause of the fault (a failed battery or blanket inadvertently thrown over top of a working power adapter or battery charger) is removed. Additionally, the thermal shutdown function employed in the LinkSwitch-XT does not have the noise sensitivity associated with discrete latch circuits, which often vary widely with PCB component layout, environmental conditions (such as proximity to external electronic noise sources) and component aging.

The IC package has a wide creepage distance between the high-voltage DRAIN pin and the lower voltage pins (both where the pins exit the package and at the PCB pads). This is important for reliable operation in high humidity and/or high pollution environments. The wide creepage distance reduces the likelihood of arcing, which improves robustness and long-term field reliability.

Another important protection function is auto-restart, which begins operating whenever there is no feedback from the power supply output for more than 40 ms (such as a short circuit on the output or a component that has failed open-circuit in the feedback loop). Auto-restart limits the average output current to about 5 % of the full load rating indefinitely, and resumes normal operation once the fault is removed.

The worst-case, no-load power consumption of this design is about 110 mW at 265 VAC, which is well below the 300 mW European Union standards. It also meets the common target of 150 mW at 230 VAC, that is seen in many particular customer specifications. The amount of heat dissipated within the supply is minimized by the high operating efficiency over all combinations of load and line.

The EE16 transformer bobbin that was used also has a wide creepage spacing, which makes it easy to meet primary-to-secondary safety spacing requirements.

This report contains the complete specification of the power supply, a detailed circuit diagram, the entire bill of materials required to build the supply, extensive documentation of the power transformer, along with test data and oscillographs of the most important electrical waveforms. All of this is intended to document the performance characteristics that should be typical of a power supply designed around the LNK362 device.

2 Power Supply Specification

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power (230 VAC)				0.15	W	
Output						
Output Voltage	V_{OUT}	5.77	6.2	6.63	V	
Output Ripple Voltage	V_{RIPPLE}		60		mV	
Output Current	I_{OUT}		322		mA	
Total Output Power						
Continuous Output Power	P_{OUT}		2.0		W	
Efficiency						
Full Load	η	60			%	Measured at P_{OUT} 115 VAC, 25 °C
Required average active efficiency at 25, 50, 75 and 100 % of P_{OUT}	η_{CEC}	55.2			%	Per California Energy Commission (CEC) / Energy Star requirements
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				>6 dB Margin
Safety		Designed to meet IEC950, UL1950 Class II				
Surge		1.5			kV	1.2/50 µs surge, IEC 1000-4-5, Series Impedance: Differential Mode: 2 Ω Common Mode: 12 Ω
Ambient Temperature	T_{AMB}	0		40	°C	Free convection, sea level

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3 Schematic

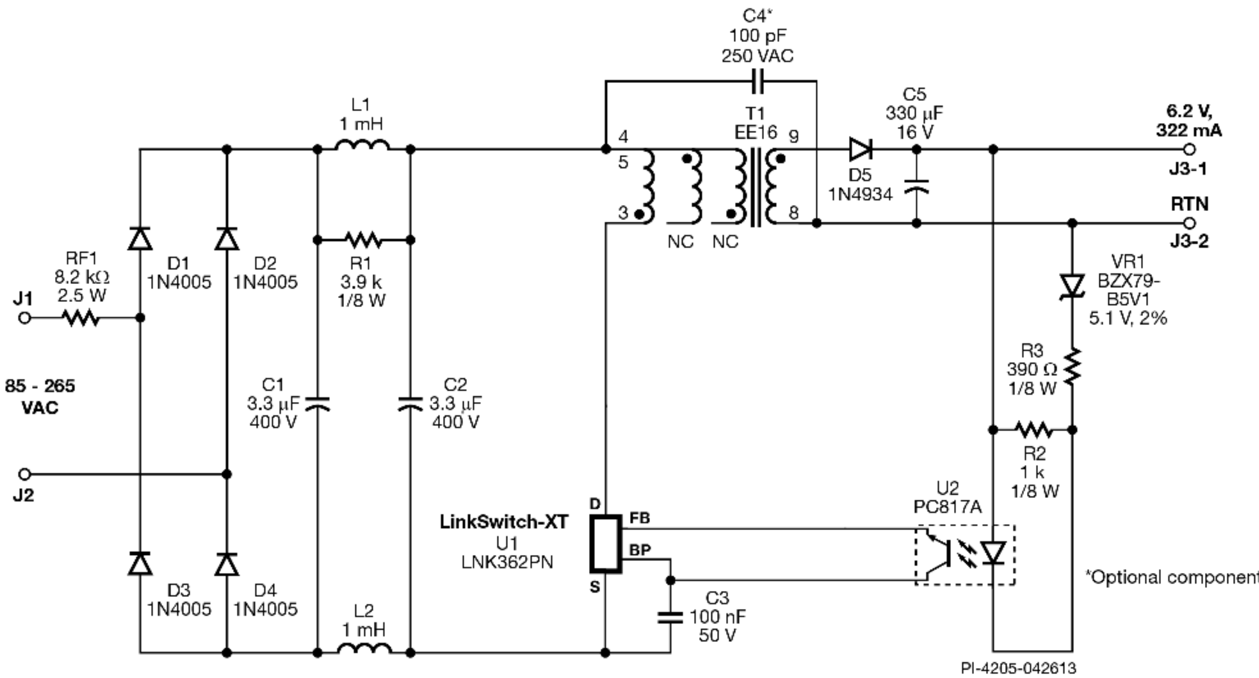

Figure 2 – Schematic.

4 Circuit Description

This converter is configured as a flyback. The output voltage is sensed and compared to a reference (VR1) on the secondary side of the supply, and the results are fed back to U1 (LNK362P) through optocoupler U2 (PC817A). This enables U1 to tightly regulate the output voltage across the entire load range. Past the point of peak power delivery, U1 will go into auto-restart, and the average power delivered to the load will be limited to about 5% of full load. This circuit takes advantage of Power Integrations *Clampless*™ transformer techniques, which use the primary winding capacitance of the transformer to clamp the voltage spike that is induced on the drain-node, by the transformer leakage inductance, each time the integrated MOSFET switch within U1 turns off. Therefore, this converter has no primary clamp components connected to the drain-node.

4.1 Input Filter

Diodes D1 through D4 rectify the AC input. The resulting DC is filtered by bulk storage capacitors C1 and C2. Inductor L1 and capacitors C1 and C2 form a pi (π) filter that attenuates differential-mode conducted EMI noise. Resistor R1 dampens the ringing of the EMI filter. Inductor L2 also attenuates conducted EMI noise in the primary return. This configuration, combined with the LinkSwitch-XT's integrated switching frequency jitter function and Power Integrations E-shield technology used in the construction of the transformer enable this design to meet EN55022 Class-B conducted EMI requirements with good margin. An optional 100 pF Y capacitor (C4) can be used to improve the unit-to-unit repeatability of the EMI measurements. Even with C4 installed, the line frequency leakage current is less than 10 μA.

4.2 LNK362 Primary

The LNK362P (U1) has the following functions integrated onto a monolithic IC: a 700 V power MOSFET, a low-voltage CMOS controller, a high-voltage current source (provides startup and steady-state operational current to the IC), hysteretic thermal shutdown and auto-restart. The excellent switching characteristics of the integrated power MOSFET allows efficient operation up to 132 kHz.

The rectified and filtered input voltage is applied to one side of the primary winding of T1. The other side of the T1 primary winding is connected to the DRAIN pin of U1. As soon as the voltage across the DRAIN and SOURCE pins of U1 exceeds 50 V, the internal high voltage current source (connected to the DRAIN pin of the IC) begins charging the capacitor (C3) connected to the Bypass (BP) pin. Once the voltage across C3 reaches 5.8 V, the controller enables MOSFET switching. MOSFET current is sensed (internally) by the voltage developed across the DRAIN-to-SOURCE resistance ($R_{DS(ON)}$) while it is turned on. When the current reaches the preset (internal) current-limit trip point (I_{LIMIT}), the controller turns the MOSFET off. The controller also has a maximum duty cycle (DC_{MAX}) signal that will turn the MOSFET off if I_{LIMIT} is not reached before the time duration equal to maximum duty cycle has elapsed.

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The controller regulates the output voltage by skipping switching cycles (ON/OFF control) whenever the output voltage is above the reference level. During normal operation, MOSFET switching is disabled whenever the current flowing into the FEEDBACK (FB) pin is greater than 49 μA. If less than 49 μA is flowing into the FB pin when the oscillator's (internal) clock signal occurs, MOSFET switching is enabled for that switching cycle and the MOSFET turns on. That switching cycle terminates when the current through the MOSFET reaches I_{LIMIT}, or the DC_{MAX} signal occurs*. At full load, few switching cycles will be skipped (disabled) resulting in a high effective switching frequency. As the load reduces, more switching cycles are skipped, which reduces the effective switching frequency. At no-load, most switching cycles are skipped, which is what makes the no-load power consumption of supplies designed around the LinkSwitch-XT family so low, since switching losses are the dominant loss mechanism at light loading. Additionally, since the amount of energy per switching cycle is fixed by I_{LIMIT}, the skipping of switching cycles gives the supply a fairly consistent efficiency over most of the load range. [NOTE * Termination of a switching cycle by the maximum duty cycle (DC_{MAX}) signal usually only occurs in an abnormal condition, such as when a high-line-only design (220/240 VAC) is subject to a brown-out condition, where just slightly over 50 V (the minimum drain voltage required for normal operation) is available to the supply, and the current through the MOSFET is not reaching I_{LIMIT} each switching cycle because of the low input voltage.]

4.3 Feedback

The output voltage of the supply is determined by the sum of the voltages developed across VR1, R2 and the (forward bias voltage) LED in optocoupler U2A. As the supply turns on and the output voltage comes into regulation, U2A will become forward biased, which will turn on its photo-transistor (U2B) causing >49 μA to flow into the FB pin, and the next switching cycle to be skipped. Resistor R2 limits the bias current through VR1 to about 1 mA. Resistor R3 can be used to fine-tune the output voltage, and also limits the peak current through U2A during load transients. Since the controller responds to feedback each switching cycle (the decision to enable or disable MOSFET switching is made right before that switching cycle is to occur), the feedback loop requires no frequency compensation components.

5 PCB Layout

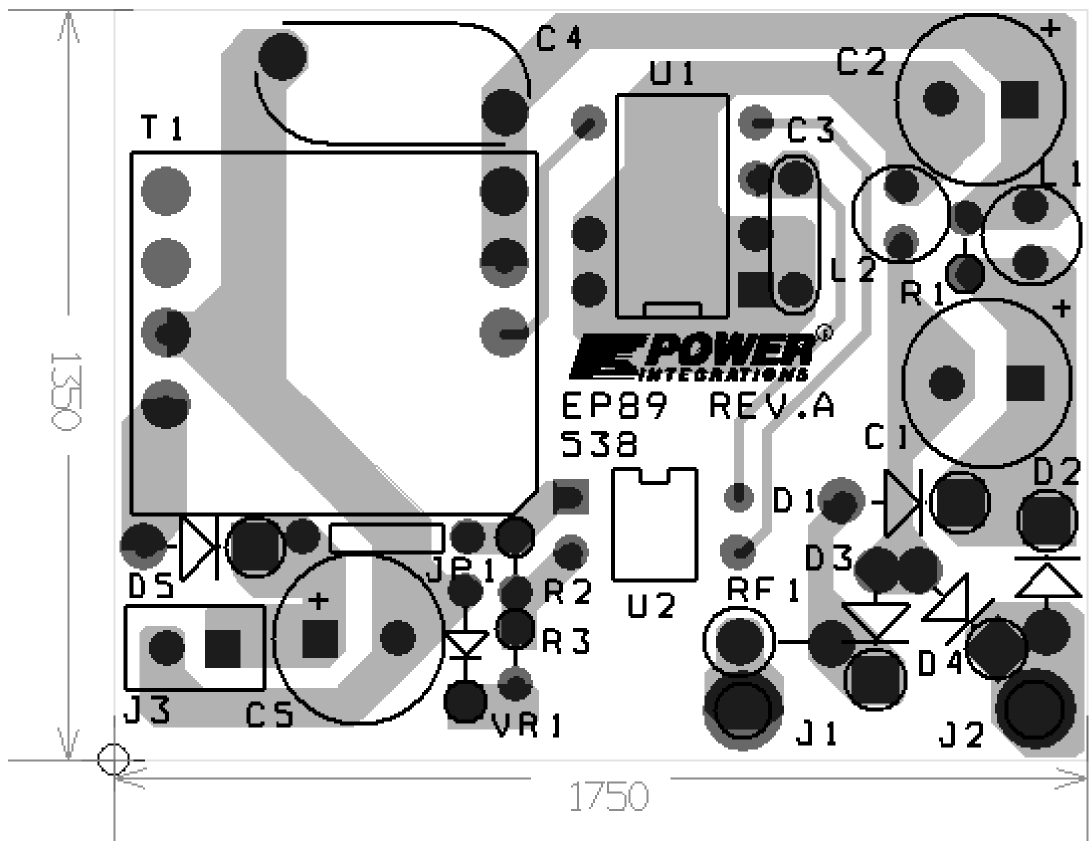

Figure 3 – Printed Circuit Board Layout (dimensions in 0.001”).

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6 Bill of Materials

Item	Ref Des	Qty	Description	Mfg Part Number	Manufacturer
1	C1 C2	2	3.3 μF, 400 V, Electrolytic, (8 x 11.5)	TAQ2G3R3MK0811MLL3	Taicon
2	C3	1	100 nF, 50 V, Ceramic, Z5U, 0.2 Lead Space	C317C104M5U5CA	Kemet
3	C4	1	100 pF, Ceramic, Y1	440LT10	Vishay
4	C5	1	330 μF, 16 V, Electrolytic, Very Low ESR, 72 mΩ, (8 x 11.5)	EKZE160ELL331MHB5D	Nippon Chemi-Con
5	D1 D2 D3 D4	4	600 V, 1 A, Rectifier, DO-41	1N4005	Vishay
6	D5	1	100 V, 1 A, Fast Recovery, 200 ns, DO-41	1N4934	Vishay
7	J1 J2	2	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
8	J3	1	6 ft, #22 AWG, 0.25 Ω, 2.1 mm connector (custom)		
9	JP1	1	Wire Jumper, Non insulated, #22 AWG, 0.3 in	298	Alpha
10	L1 L2	2	1 mH, 0.15 A, Ferrite Core	SBCP-47HY102B	Tokin
11	R1	1	3.9 kΩ, 5%, 1/8 W, Carbon Film	CFR-12JB-3K9	Yageo
12	R2	1	1 kΩ, 5%, 1/8 W, Carbon Film	CFR-12JB-1K0	Yageo
13	R3	1	390 Ω, 5%, 1/8 W, Carbon Film	CFR-12JB-390R	Yageo
14	RF1	1	8.2 Ω, 2.5 W, Fusible/Flame Proof Wire Wound	CRF253-4 5T 8R2	Vitrohm
15	T1	1	Transformer, EE16, Horizontal, 10 pins	SNX-1378 LSLA40343	Santronics Li Shin
16	U1	1	LinkSwitch-XT, DIP-8B	LNK362P	Power Integrations
17	U2	1	Optocoupler, 35 V, CTR 80-160%, 4-DIP	PC817X1	Sharp
18	VR1	1	5.1 V, 500 mW, 2%, DO-35	BZX79-B5V1	Vishay

7 Transformer Specification

7.1 Electrical Diagram

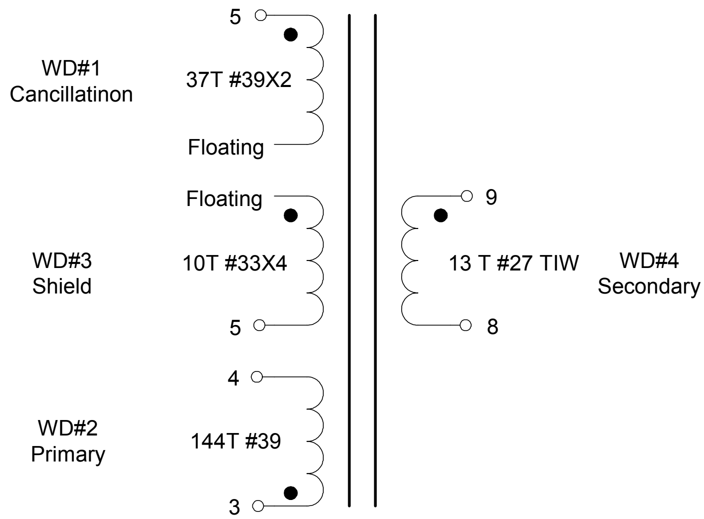

Figure 4 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 3, 4, 5 to pins 8, 9.	3000 VAC
Primary Inductance	Pins 3-4, all other windings open, measured at 100 kHz, 0.4 V_{RMS}.	2.64 mH, ±12%
Resonant Frequency	Pins 3-4, all other windings open.	275 kHz (Min.) 500 kHz (Max)
Primary Leakage Inductance	Pins 3-4, with pins 8-9 shorted, measured at 100 kHz, 0.4 V_{RMS}.	70 μH (Max.)

7.3 Materials

Item	Description
[1]	Core: PC40EE16-Z, TDK or equivalent gapped for AL of 127 nH/t^2
[2]	Bobbin: Horizontal 10 pin
[3]	Magnet Wire: #39 AWG
[4]	Magnet Wire: #33 AWG
[5]	Triple Insulated Wire: #27 AWG
[6]	Tape, 3M 1298 Polyester Film, 2.0 Mils thick, 8.0 mm wide
[7]	Varnish

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7.4 Transformer Build Diagram

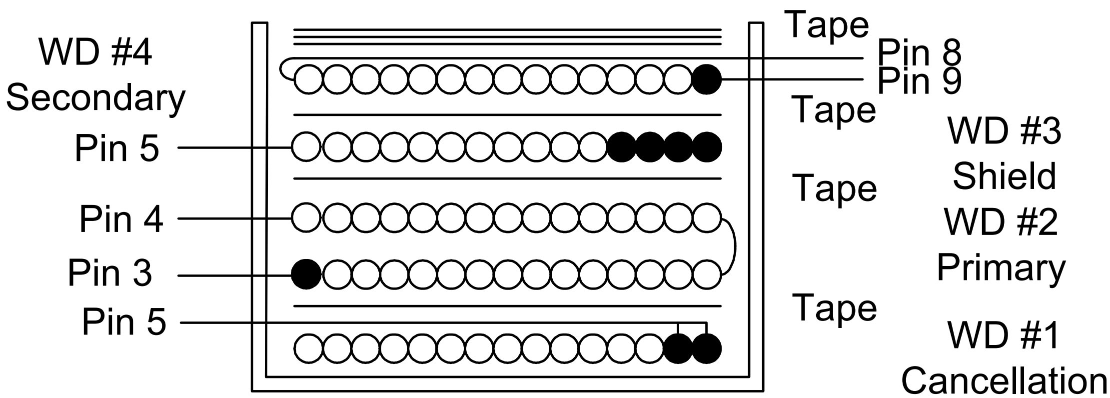

Figure 5 – Transformer Build Diagram.

7.5 Transformer Construction

WD #1 Cancellation Winding	Primary pin side of the bobbin oriented to left hand side. Temporarily start at pin 6. Wind 37 bifilar turns of item [3] from right to left. Wind with tight tension across bobbin evenly. Cut at end. Finish start on pin 5.
Insulation	1 Layer of tape [6] for insulation.
WD #2 Primary Winding	Start at Pin 3. Wind 72 turns of item [3] from left to right. Then wind another 72 turns on the next layer from right to left. Terminate the finish on pin 4. Wind with tight tension across bobbin evenly.
Insulation	Use one layer of tape [6] for basic insulation.
WD #3 Shield Winding	Starting at pin 6 temporarily, wind 10 quadfilar turns of item [4]. Wind from right to left with tight tension across entire bobbin width. Finish on pin 5. Cut at the start lead.
Insulation	Use one layer of tape [6] for basic insulation.
WD #4 Secondary Winding	Start at pin 9, wind 13 turns of item [5] from right to left. Spread turns evenly across bobbin. Finish on Pin 8.
Outer insulation	Wrap windings with 3 layers of tape [6].
Core Assembly	Assemble and secure core halves.
Varnish	Dip varnish assembly with item [7].

8 Transformer Design Spreadsheet

ACDC_LinkSwitch-XT_101205; Rev.1.2; Copyright Power Integrations 2005	INPUT	INFO	OUTPUT	UNIT	ACDC_LinkSwitch-XT_101205_Rev1-2.xls; LinkSwitch-XT Continuous/Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN	85			Volts	Minimum AC Input Voltage
VACMAX	265			Volts	Maximum AC Input Voltage
fL	50			Hertz	AC Mains Frequency
VO	6.20			Volts	Output Voltage (main) (For CC designs enter upper CV tolerance limit)
IO	0.32			Amps	Power Supply Output Current (For CC designs enter upper CC tolerance limit)
CC Threshold Voltage	0.00			Volts	Voltage drop across sense resistor.
Output Cable Voltage Resistance			0.17	Ohms	Enter the resistance of the output cable (if used)
PO			2.00	Watts	Output Power (VO x IO + CC dissipation)
Feedback Type	Opto		Opto		Enter 'BIAS' for Bias winding feedback and 'OPTO' for Optocoupler feedback
Add Bias Winding	No		No		Enter 'YES' to add a Bias winding. Enter 'NO' to continue design without a Bias winding. Addition of Bias winding can lower no load consumption
Clampless design (LNK 362 only)	Yes	***Caution***	Clampless		!!! Caution. For designs above 2 W and no Bias winding, Verify peak Drain Voltage and EMI performance
n	0.63		0.63		Efficiency Estimate at output terminals.
Z	0.50		0.5		Loss Allocation Factor (suggest 0.5 for CC=0 V, 0.75 for CC=1 V)
tC	2.90			mSeconds	Bridge Rectifier Conduction Time Estimate
CIN	6.60			uFarads	Input Capacitance
Input Rectification Type	F		***F***		Choose H for Half Wave Rectifier and F for Full Wave Rectification
ENTER LinkSwitch-XT VARIABLES					
LinkSwitch-XT	**LNK362**		**LNK362**		User selection for LinkSwitch-XT
Chosen Device		*LNK362*			
ILIMITMIN			*0.130*	Amps	Minimum Current Limit
ILIMITMAX			*0.150*	Amps	Maximum Current Limit
fSmin			*124000*	Hertz	Minimum Device Switching Frequency
I^2fmin			2199	A^2Hz	I^2f (product of current limit squared and frequency is trimmed for tighter tolerance)
VOR	77.00		77	Volts	VOR > 90V not recommended for Clampless designs with no Bias windings. Reduce VOR below 90V
VDS			10	Volts	LinkSwitch-XT on-state Drain to Source Voltage
VD	0.75		0.75	Volts	Output Winding Diode Forward Voltage Drop
KP			1.00		Ripple to Peak Current Ratio (0.6 < KP < 6.0)

ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type			**EE16**		Suggested smallest commonly available core
Core		*EE16*		*P/N:*	PC40EE16-Z
Bobbin		*EE16_BOBBIN*		*P/N:*	EE16_BOBBIN
AE			0.192	cm^2	Core Effective Cross Sectional Area
LE			3.5	cm	Core Effective Path Length
AL			1140	nH/T^2	Ungapped Core Effective Inductance
BW			8.6	mm	Bobbin Physical Winding Width

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M			0	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L			2		L > 2 or L < 1 not recommended for Clampless designs with no Bias windings. Enter L = 2
NS			13		Number of Secondary Turns
NB			N/A		Bias winding not used
VB			N/A	Volts	Bias winding not used
PIVB			N/A	Volts	N/A - Bias Winding not in use
DC INPUT VOLTAGE PARAMETERS					
VMIN			87	Volts	Minimum DC Input Voltage
VMAX			375	Volts	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.50		Maximum Duty Cycle
IAVG			0.04	Amps	Average Primary Current
IP			0.13	Amps	Minimum Peak Primary Current
IR			0.12	Amps	Primary Ripple Current
IRMS			0.06	Amps	Primary RMS Current
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			2677	uHenries	Typical Primary Inductance. +/- 12%
LP_TOLERANCE	12.00		12	%	Primary inductance tolerance
NP			144		Primary Winding Number of Turns
ALG			129	nH/T^2	Gapped Core Effective Inductance
BM			1452	Gauss	Maximum Operating Flux Density, BM<1500 is recommended
BAC			553	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1654		Relative Permeability of Ungapped Core
LG			0.17	mm	Gap Length (Lg > 0.1 mm)
BWE			17.2	mm	Effective Bobbin Width
OD			0.12	mm	Maximum Primary Wire Diameter including insulation
INS			0.03	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.09	mm	Bare conductor diameter
AWG			39	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			13	Cmils	Bare conductor effective area in circular mils
CMA			225	Cmils/Amp	Primary Winding Current Capacity (150 < CMA < 500)

TRANSFORMER SECONDARY DESIGN PARAMETERS					
Lumped parameters					
ISP			1.44	Amps	Peak Secondary Current
ISRMS			0.63	Amps	Secondary RMS Current
IRIPPLE			0.54	Amps	Output Capacitor RMS Ripple Current
CMS			125	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			29	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS			0.29	mm	Secondary Minimum Bare Conductor Diameter
ODS			0.66	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
INSS			0.19	mm	Maximum Secondary Insulation Wall Thickness
VOLTAGE STRESS PARAMETERS					
VDRAIN			-	Volts	For Clampless designs, the Peak Drain Voltage is highly dependent on Transformer capacitance and leakage inductance. Please verify this on the bench and ensure that it is below 650 V to allow 50 V margin for transformer variation.
PIVS			40	Volts	Output Rectifier Maximum Peak Inverse Voltage
FEEDBACK COMPONENTS					
Recommended Bias Diode			1N4003 - 1N4007		Recommended diode is 1N4003. Place diode on return leg of bias winding for optimal EMI. See LinkSwitch-XT Design Guide
R1			500 - 1000	ohms	CV bias resistor for CV/CC circuit. See LinkSwitch-XT Design Guide
R2			200 - 820	ohms	Resistor to set CC linearity for CV/CC circuit. See LinkSwitch-XT Design Guide
TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS)					
1st output					
VO1			6.20	Volts	Main Output Voltage (if unused, defaults to single output design)
IO1			0.32	Amps	Output DC Current
PO1			2.00	Watts	Output Power
VD1			0.75	Volts	Output Diode Forward Voltage Drop
NS1			13.00		Output Winding Number of Turns
ISRMS1			0.63	Amps	Output Winding RMS Current
IRIPPLE1			0.54	Amps	Output Capacitor RMS Ripple Current
PIVS1			40.03	Volts	Output Rectifier Maximum Peak Inverse Voltage
Recommended Diodes			UF4001, SB150		Recommended Diodes for this output
Pre-Load Resistor			2	k-Ohms	Recommended value of pre-load resistor
CMS1			126.56	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1			29.00	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1			0.29	mm	Minimum Bare Conductor Diameter
ODS1			0.66	mm	Maximum Outside Diameter for Triple Insulated Wire

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9 Performance Data

All measurements performed at room temperature (25 °C), 60 Hz input frequency.

9.1 Efficiency

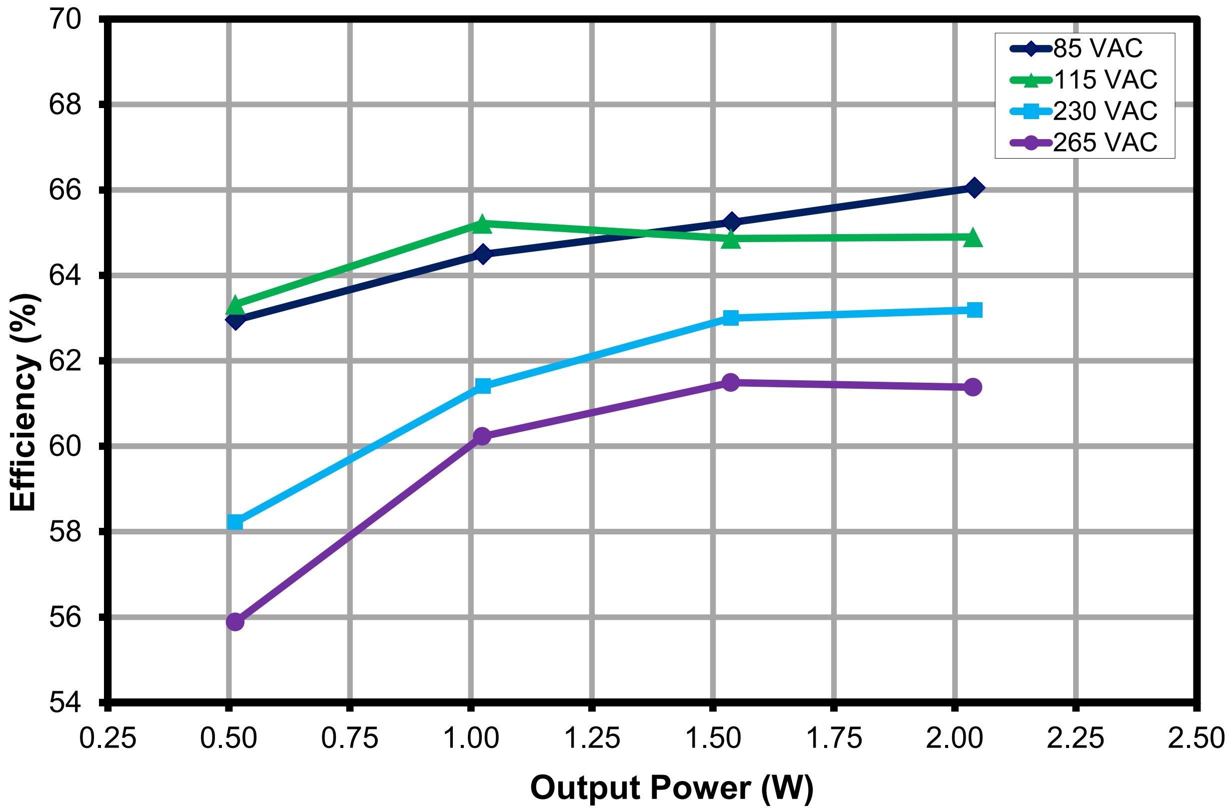

Figure 6 – Efficiency vs. Output Power.

% of Full Load	% Efficiency @ 115 VAC	% Efficiency @ 230 VAC
25	63.3	58.2
50	65.2	61.4
75	64.9	63.0
100	64.9	63.2
Average Efficiency	**64.6**	**61.5**
CEC Requirement	**55.2**	

Figure 7 – Efficiency vs. Input Voltage and Load, Room Temperature, 60 Hz.

9.1.1 Active Mode Efficiency (CEC) Measurement Data

All single output adapters, including those provided with products, for sale in California after July 1st, 2006 must meet the California Energy Commission (CEC) requirement for minimum active mode efficiency and no-load input power consumption. Minimum active mode efficiency is defined as the average efficiency at 25, 50, 75 and 100% of rated output power, based on the nameplate rated output power of the supply.

Nameplate Output (P_O)	Minimum Efficiency in Active Mode of Operation
< 1 W	$0.49 \times P_O$
≥ 1 W to ≤ 49 W	$0.09 \times \ln(P_O) + 0.49$ [ln = natural log]
> 49 W	0.84 W

For adapters that are rated for a single input voltage, the efficiency measurements are made at the input voltage (115 VAC or 230 VAC) specified on the nameplate. For universal input adapters, the measurements are made at both nominal input voltages (115 VAC and 230 VAC).

To comply with the standard, the average of the measured efficiencies must be greater than or equal to the efficiency specified by the CEC/Energy Star standard.

More states within the USA and other countries are adopting this standard, for the latest up to date information on worldwide energy efficiency standards, please visit the PI Green Room at:

http://www.powerint.com/greenroom/regulations.htm

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9.2 No-load Input Power

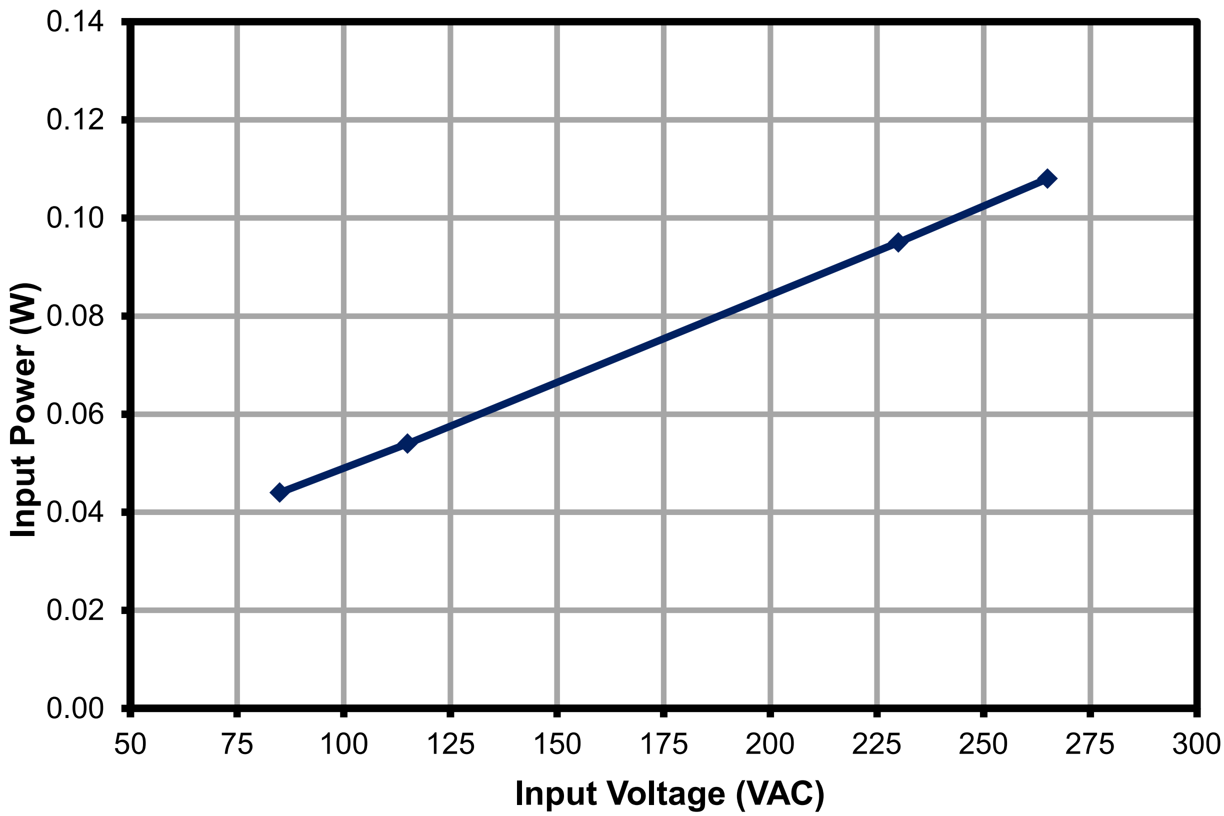

Figure 8 – No-load Input Power vs. Input Line Voltage, Room Temperature, 60 Hz.

9.3 Available Standby Output Power

The graph below shows the available output power vs line voltage when input power is limited to 1 W and 2 W, respectively.

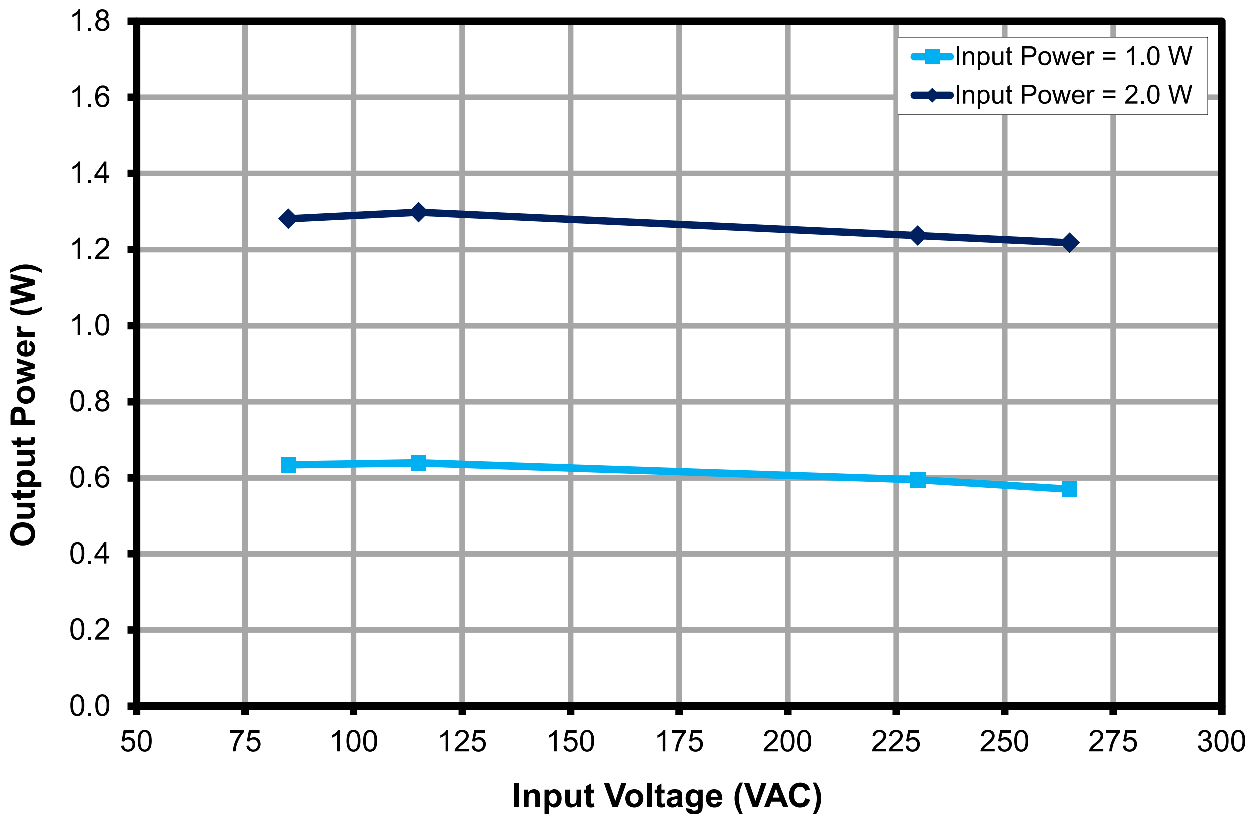

Figure 9 – Available Output Power for Input Power of 1 W and 2 W.

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9.4 Regulation

9.4.1 Load

The output of this supply was characterized by making measurements at the end of a 6 foot long output cable. The DC resistance of the cable is approximately 0.2 Ω.

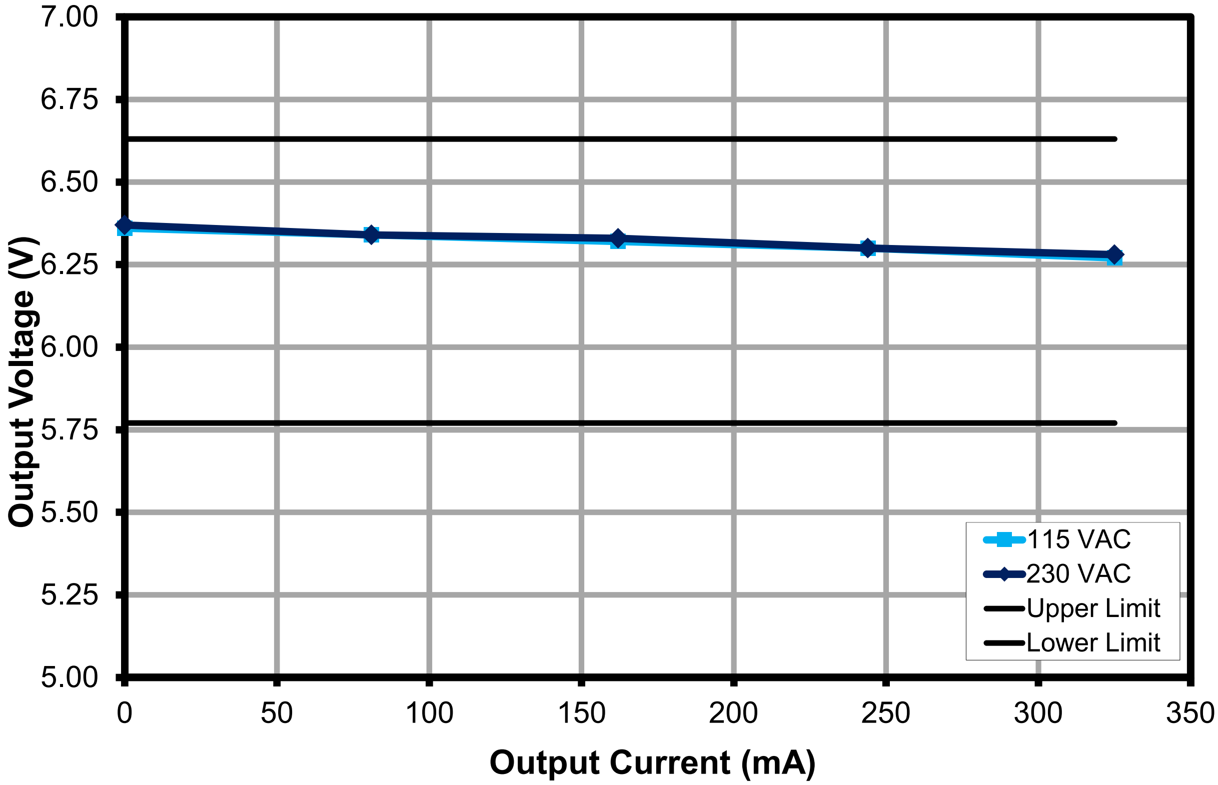

Figure 10 – Load Regulation, Room Temperature.

9.4.2 Line

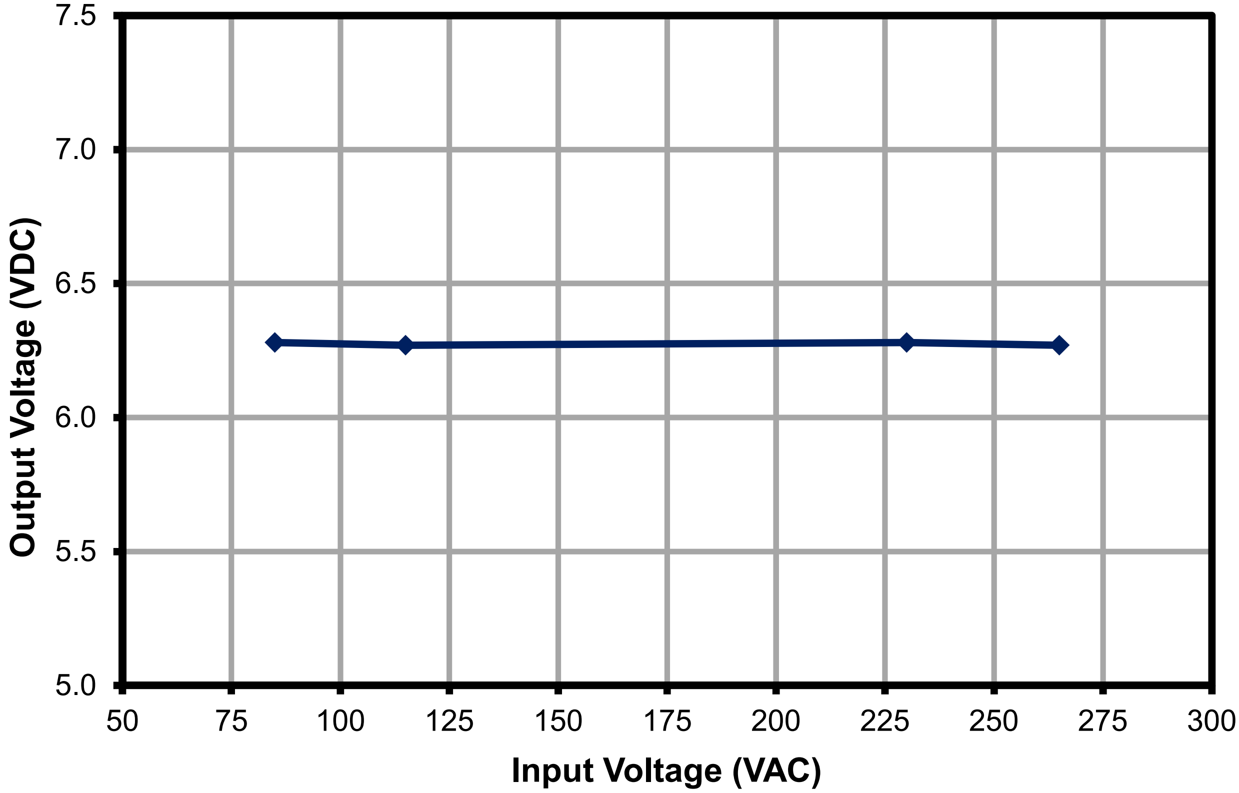

Figure 11 – Line Regulation, Room Temperature, Full Load.

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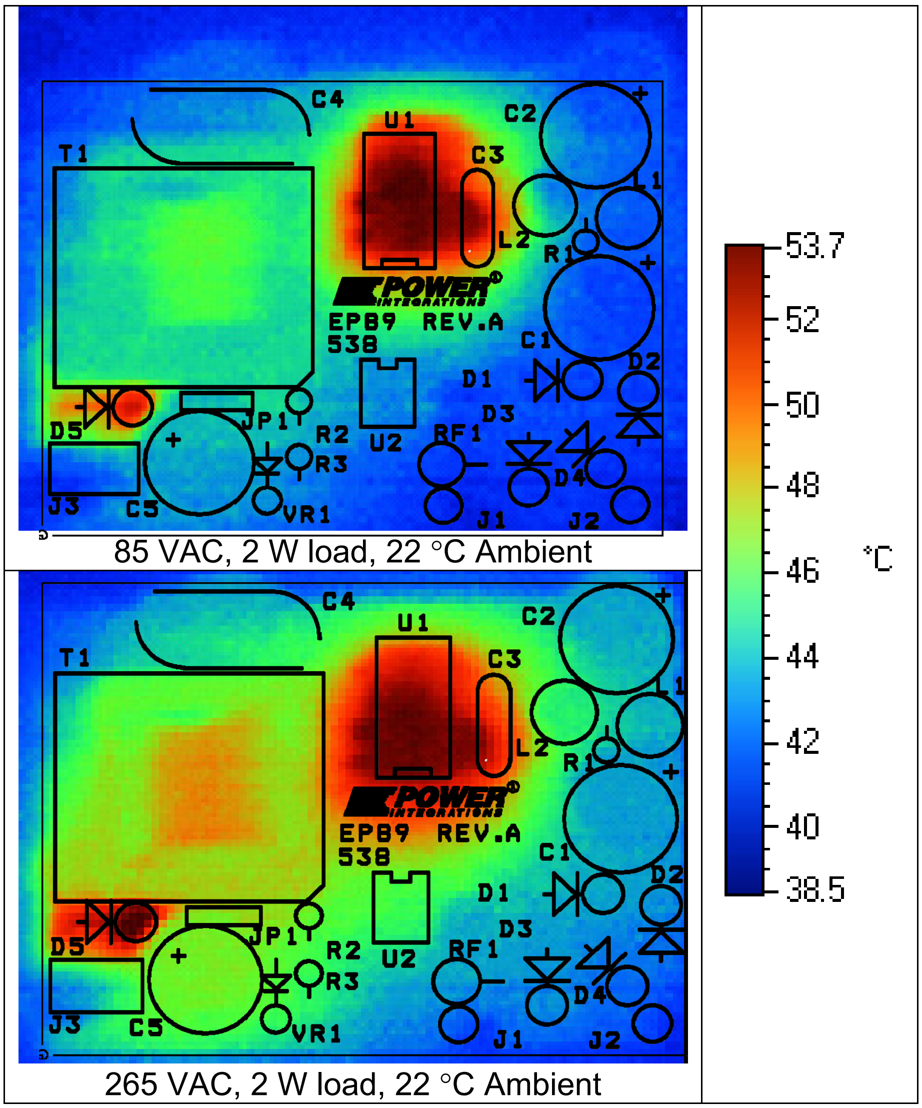
10 Thermal Performance

Thermal performance was measured inside a plastic enclosure, at full load, with no airflow over the power supply components or the housing they were enclosed within.

Item	90 VAC	265 VAC
Ambient	40 °C	40 °C
LNK362P (SOURCE pin)	93.0 °C at 2.0 W output (6.2 V, 322 mA)	111.8 °C at 2.0 W output (6.2 V, 322 mA).



85 VAC, 2 W load, 22 °C Ambient

265 VAC, 2 W load, 22 °C Ambient

Figure 12– Infra-red Thermograph of Operating Unit: Open Frame, 22 °C Ambient.

11 Waveforms

11.1 Drain Voltage and Current, Normal Operation

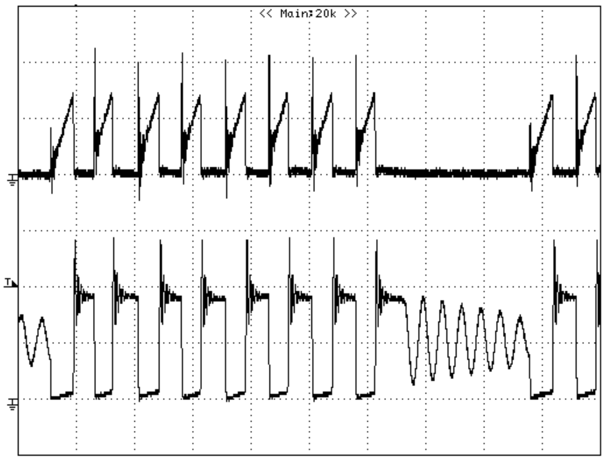


Figure 13 – 85 VAC, Full Load.
Upper: I_{DRAIN}, 0.1 A / div.
Lower: V_{DRAIN}, 100 V / div.

Figure 14 – 265 VAC, Full Load.
Upper: I_{DRAIN}, 0.1 A / div.
Lower: V_{DRAIN}, 200 V / div.

11.2 Output Voltage Start-up Profile

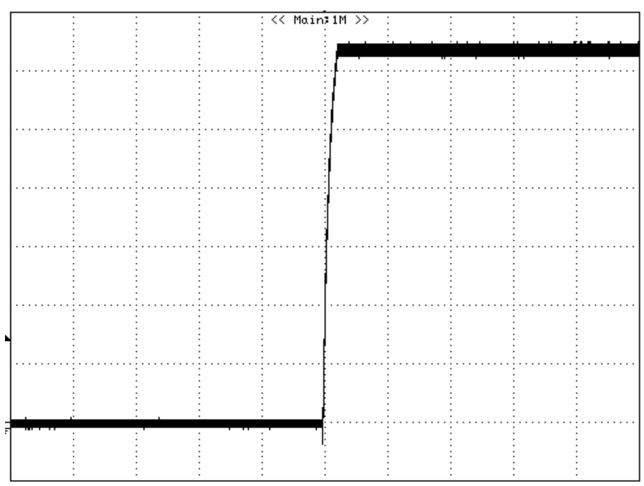


Figure 15 – Start-up Profile, 115 VAC.
1 V, 20 ms / div.

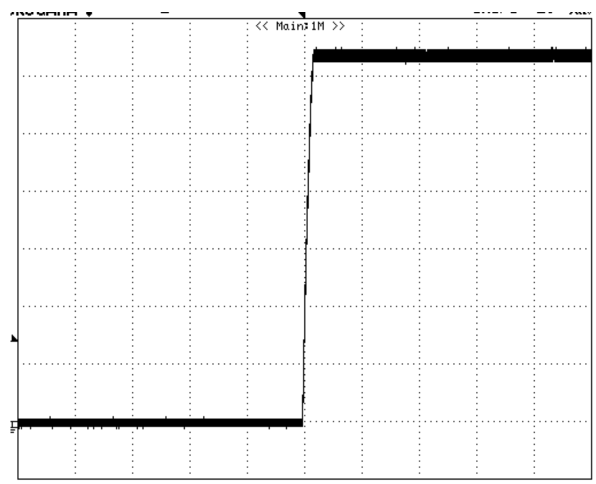


Figure 16 – Start-up Profile, 230 VAC.
1 V, 20 ms / div.

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11.3 Drain Voltage and Current Start-up Profile

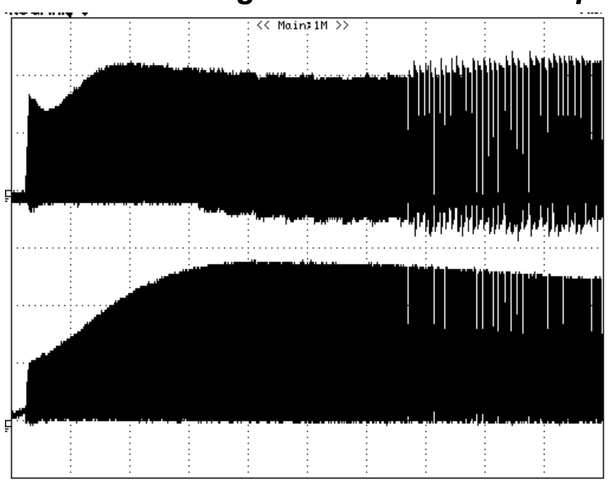

Figure 17 – 85 VAC Input and Maximum Load.
Upper: I_{DRAIN}, 0.1 A / div.
Lower: V_{DRAIN}, 100 V, 1 ms / div.

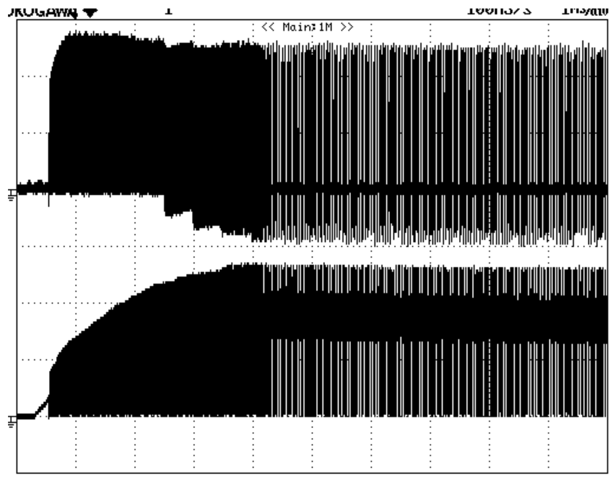

Figure 18 – 265 VAC Input and Maximum Load.
Upper: I_{DRAIN}, 0.1 A / div.
Lower: V_{DRAIN}, 200 V, 1 ms / div.

11.4 Load Transient Response (75% to 100% Load Step)

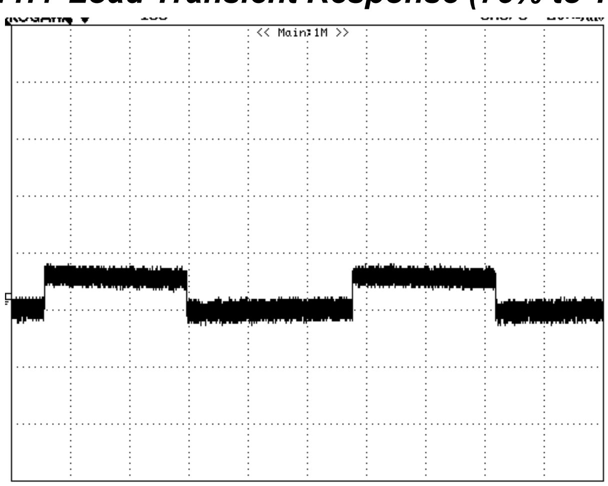

Figure 19 – Transient Response, 115 VAC, 100-75-100% Load Step.
Output Voltage
50 mV, 20 ms / div.

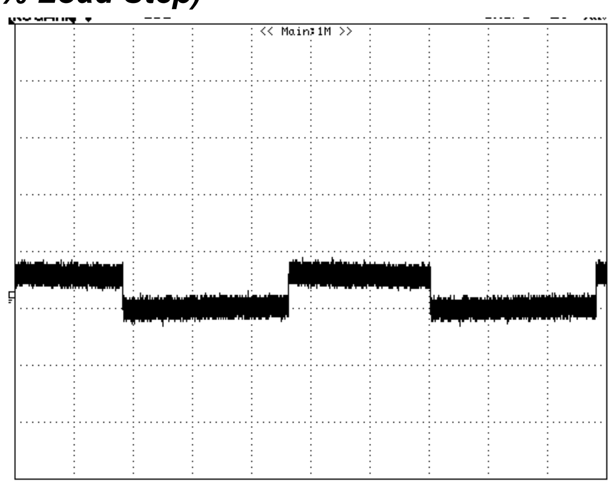

Figure 20 – Transient Response, 230 VAC, 100-75-100% Load Step.
Output Voltage
50 mV, 20 ms / div.

11.5 Output Ripple Measurements

11.5.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pickup. Details of the probe modification are provided in Figure 21 and Figure 22.

The 5125BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 1.0 μF/50 V aluminum electrolytic. ***The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).***

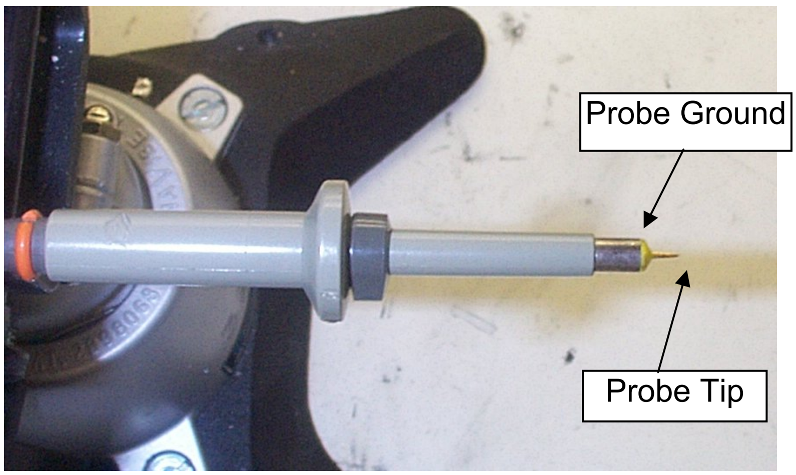

Figure 21 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

Figure 22 – Oscilloscope Probe with Probe Master 5125BA BNC Adapter. (Modified with wires for probe ground for ripple measurement, and two parallel decoupling capacitors added)

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11.5.2 Measurement Results

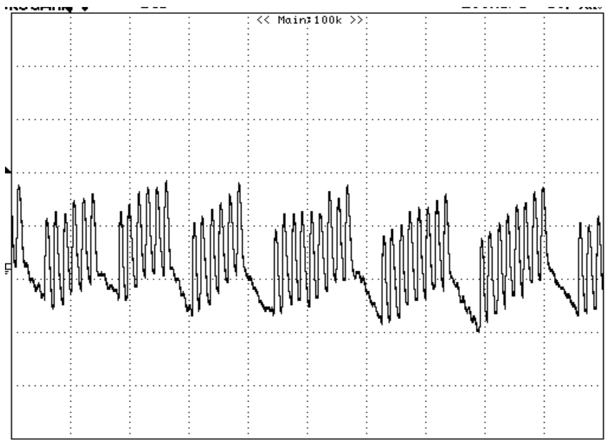

Figure 23 – Ripple, 85 VAC, Full Load.
50 µs, 20 mV / div.

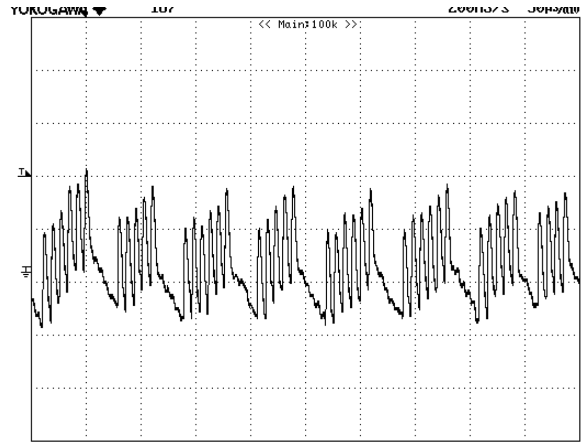

Figure 24 – 5 V Ripple, 115 VAC, Full Load.
50 µs, 20 mV / div.

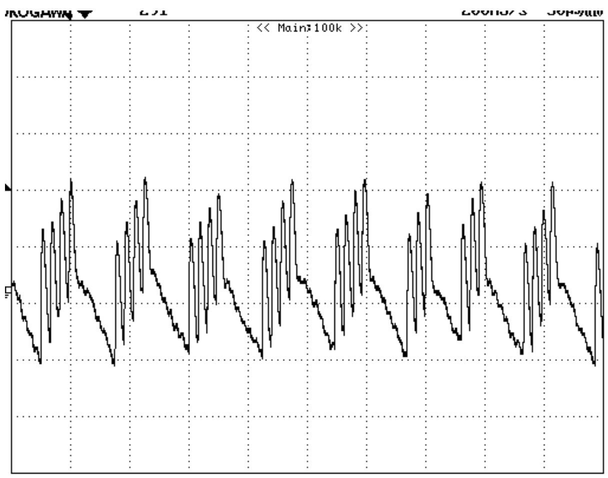

Figure 25 – Ripple, 230 VAC, Full Load.
50 µs, 20 mV / div.

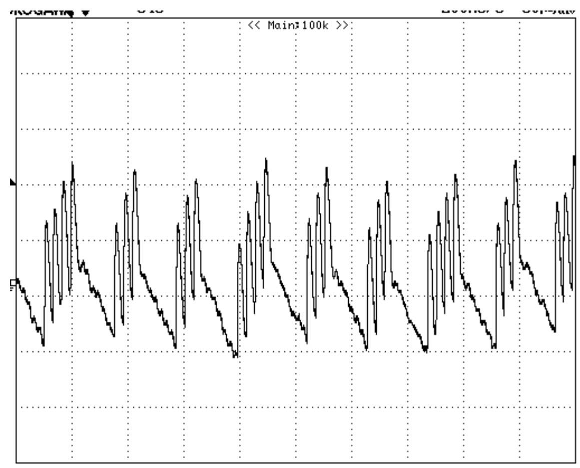

Figure 26 – Ripple, 265 VAC, Full Load.
50 µs, 20 mV / div.

12 Line Surge

Differential input line 1.2/50 µs surge testing was completed on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC / 60 Hz. Output was loaded at full load and operation was verified following each surge event.

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+500	230	L to N	90	Pass
-500	230	L to N	90	Pass
+750	230	L to N	90	Pass
-750	230	L to N	90	Pass
+1000	230	L to N	90	Pass
-1000	230	L to N	90	Pass
+1500	230	L to N	90	Pass
-1500	230	L to N	90	Pass

Unit passes under all test conditions.

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13 Conducted EMI

Figure 27 – Conducted EMI, Maximum Steady State Load, 115 VAC, 60 Hz, Artificial Hand and EN55022 B Limits.

Figure 28 – Conducted EMI, Maximum Steady State Load, 230 VAC, 60 Hz, Artificial Hand and EN55022 B Limits.

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14 Revision History

Date	Author	Revision	Description & changes
08-Nov-05	JAJ	1.0	Formatted for Final Release
26-Apr-13	KM	1.1	Fixed schematic error and re-formatted.

For the latest updates, visit our website: www.powerint.com

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