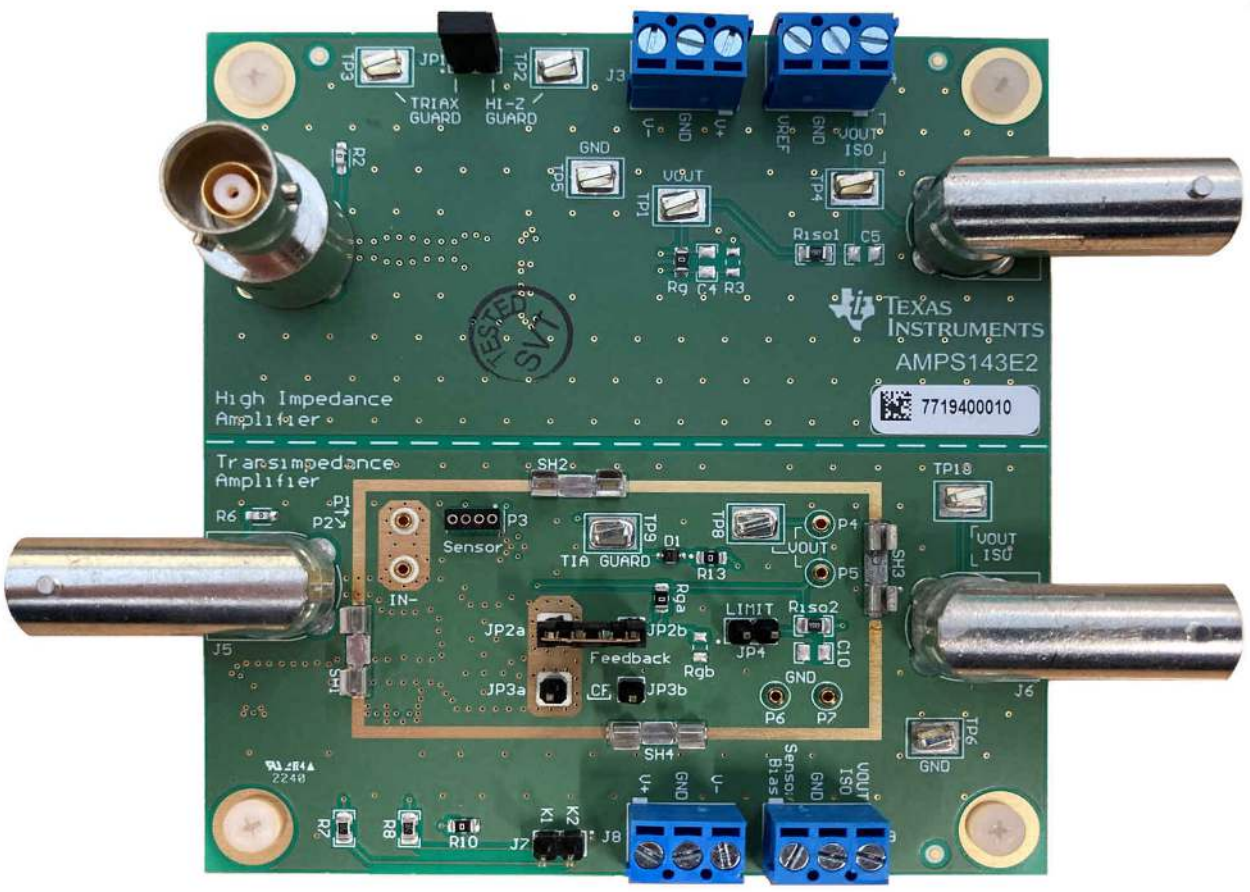
User's Guide

OPA928 Evaluation Module

ABSTRACT



This user's guide describes the operation and use of the OPA928 evaluation module (EVM). The user's guide provides information on how to set up the EVM and describes different circuit configurations that can be used to evaluate the performance of the OPA928 femtoampere, input-bias-current op amp. Throughout this document, the terms *evaluation board, evaluation module,* and *EVM* are synonymous with the OPA928EVM. This document also includes an electrical schematic, simplified schematics of OPA928 applications circuits, a printed circuit board (PCB) layout drawing, and a parts list for the EVM.

Note

For best possible performance, make sure to review the Section 1.1 before handling the EVM board.

Table of Contents

List of Figures

List of Tables

Trademarks

All trademarks are the property of their respective owners.

1 Read This First

1.1 EVM Cleanliness Guidelines

Applications requiring femtoampere-level performance are extremely sensitive to contamination. Contaminants in the form of solder flux, salts, oils, organic acids, and more can form conductive paths over PCB traces that allow small currents to leak into input traces or other sensitive nodes, thus degrading performance. For best possible performance, make sure to keep the OPA928EVM as clean as possible.

The following list of best practices helps prevent the EVM from becoming contaminated:

- Always wear a fresh, clean pair of powder-free gloves or finger cots when handling the OPA928EVM.
- When handling the EVM, always hold the board by the edges.
- Avoid touching the surface of the PCB, especially near sensitive nodes or input traces.
- Be cautious when breathing, speaking, sneezing, and so on, to prevent moisture or saliva from contacting the EVM.
- Do not allow direct airflow from cooling fans or ionizers onto the board. Moving air can blow dust and moisture onto sensitive nodes. Additionally, airflow introduces moving charges that present as a small current at the input.
- When not in use, place the EVM in ESD bag or other enclosure to prevent dust and other contaminants from settling on the board.
- When configuring through-hole components in the TIA feedback path, handle the components by the wire leads only. Avoid touching the component package.

The OPA928EVM undergoes a rigorous cleaning protocol before shipping to customers, providing femtoampere-level performance directly out of the box. Follow the cleaning procedures detailed in Section 5 to maintain best performance. The EVM must be cleaned per these instructions anytime the board is soldered or modified near sensitive nodes, or if these nodes become contaminated by other means.

2 Overview

The OPA928 is a 16-V, femtoampere input-bias-current operational amplifier (op amp) optimized for extremely low current and high-impedance applications. The internally guarded ESD structure and special package pinout isolates the amplifiers inputs from the output and power supply pins. The internal guard buffer is accessible through the guard pin, allowing the guard structure to be extended to the input traces and feedback components.

The OPA928EVM is a four-layer PCB using a hybrid stack-up of Rogers 4350B and FR-4. The EVM uses advanced guarding and shielding techniques to maintain femtoampere-level PCB layout performance. Both high-impedance (Hi-Z) buffer (see Section 4.1) and transimpedance amplifier (TIA, see Section 4.2) configurations are featured to evaluate the OPA928 in common application circuits. These configurations are separated into two independent circuits on the board. By default, 0-Ω resistor Rgnd is populated on the bottom of the board, connecting the analog ground of the two circuits.

The two OPA928 amplifiers, U1 and U2, are located on the bottom side of the EVM and are enclosed within grounded RF shields to protect from contamination, noise, and electromagnetic interference (EMI). The top side of the EVM features a variety of pin sockets, jumpers, and other components that provide easy configuration, while limiting the potential for performance-degrading contamination at sensitive nodes.

2.1 Guarding and Shielding

Every insulator, including PCB material, has a finite resistance that becomes a potential path for current to leak into the high-impedance traces. Copper guard traces are laid out around all the high-impedance input and feedback nodes to protect the signal path from current leaking through the board material. The guard presents a low-impedance path equipotential to the input traces. Any current leaking towards the input prefers the low-impedance guard path over the high-impedance input path. The guard and input are of equal potential; therefore, theoretically, no current flows between these nodes, and the input is protected.

The OPA928EVM PCB layout places the input traces and all sensitive feedback components within a perimeter of guard copper that is then enclosed by a grounded RF shield. The solder mask has been removed from the guard traces to reduce surface charge accumulation. Three-dimensional leakage protection is achieved through guard copper on internal PCB layers and guard-potential via fences surrounding sensitive nodes.

High-impedance, femtoampere-level circuits are highly sensitive to electromagnetic interference (EMI). To help reduce the effects of EMI in the OPA928EVM, three RF shields are connected to the board by surface-mounted shield clips. These shields fully enclose all exposed high-impedance traces and reduce external noise and EMI by shunting the noise to ground. Unless actively configuring or cleaning the EVM, keep these shields installed to reduce EMI and prevent contaminants from entering sensitive nodes. Some user configurations require the top shield to be removed during operation. For best EMI performance, operate the assembly within a shielded enclosure that is connected to ground.

There are three RF shields connected to the board by surface-mounted shield clips. These shields protect from external noise and EMI by shunting the noise to ground. The OPA928EVM is designed to fully enclose all exposed high-impedance traces within grounded RF shields during operation. The Hi-Z circuit has one shield on the bottom side of the EVM. The TIA circuit has two shields, one on the bottom of the EVM and one on the top. Keep these shields installed at all times unless actively configuring or cleaning the EVM.

3 Getting Started

The OPA928EVM is powered from a ±2.25-V to ±8-V dual supply. The high-impedance and transimpedance amplifier circuits have separate power-supply terminals located at terminal blocks J3 and J8, respectively. The TIA circuit has an additional terminal block (J7) requiring two independently-controlled 5-V channels to drive a T-switch that discharges the feedback loop (see Section 4.2.2.1). The EVM can be used without this function, in which case J7 can be ignored.

3.1 Related Documentation From Texas Instruments

Document	Literature Number
OPA928 product data sheet	SBOSA77

3.2 Electrostatic Discharge Caution

CAUTION

Some components on the OPA928EVM are susceptible to damage from electrostatic discharge (ESD). Customers are advised to observe proper ESD handling precautions when unpacking and handling the EVM, including the use of a grounded wrist strap at an approved ESD workstation.

4 EVM Circuit Description

This section describes the circuit configurations and operation of the OPA928EVM.

4.1 High-Impedance Amplifier Circuit

The high-impedance amplifier (Hi-Z) circuit features the OPA928 in a noninverting buffer configuration designed as a front end for high-impedance sensors. The Hi-Z circuit is located on the upper half of the EVM. The sensitive input traces are guarded from leakage currents using the techniques described in Section 2.1.

The input path consists of CBJ70 triaxial (or triax) connector (J1) and 0-Ω series resistor (R1) connected to the noninverting input of the OPA928 (U1). A triax connector is similar to a BNC connector, but includes a guarded enclosure between the center (signal) conductor and the outer shield. The J1 triax connector has three index lugs and is incompatible with standard BNC connectors.

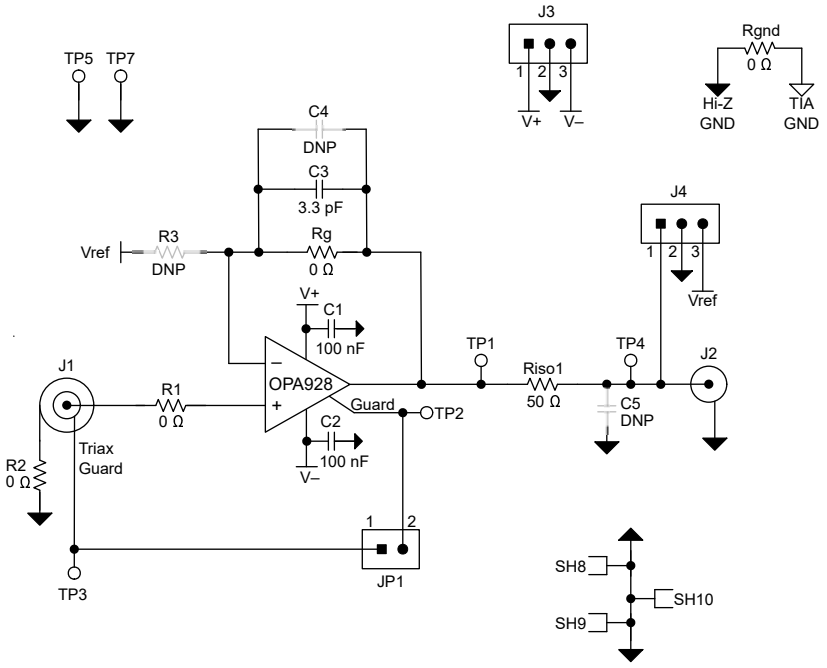


Figure 4-1. HI-Z Circuit Schematic (Simplified)

The high-impedance input traces are surrounded by a copper guard plane driven by the OPA928 internal guard buffer. The guard buffer tracks the potential of the amplifier input as the common-mode input voltage changes. The guard pin of the OPA928 can be connected to the triax cable guard by installing a shunt jumper at JP1. If the guard of the triax connector is not driven by another source, install the jumper at JP1. The amplifier and input traces are located on the bottom of the PCB and are fully enclosed by a grounded RF shield to prevent noise and EMI from coupling into the signal path.

The HI-Z circuit feedback loop is not sensitive to leakage currents or EMI, and has been extended out of the shielded enclosure on the top layer for configurability. If done carefully, the feedback circuitry (Rg, R3, C4) can be soldered and desoldered without requiring a rigorous cleaning protocol (see Section 1.1). The long feedback traces add some parasitics to the loop; therefore, a small feedback capacitor (C3) is installed inside the shielded enclosure to maintain stability.

4.2 Transimpedance Amplifier Circuit

The transimpedance amplifier (TIA) circuit is located on the lower half of the OPA928EVM. This configuration functions as a front end to convert femtoampere-level input currents into voltage outputs. The input path consists of BNC connector (J5) and 0-Ω series resistor (R4) connected to the inverting input of the OPA928 (U2). The inverting input can be accessed directly through pin sockets P1 and P2.

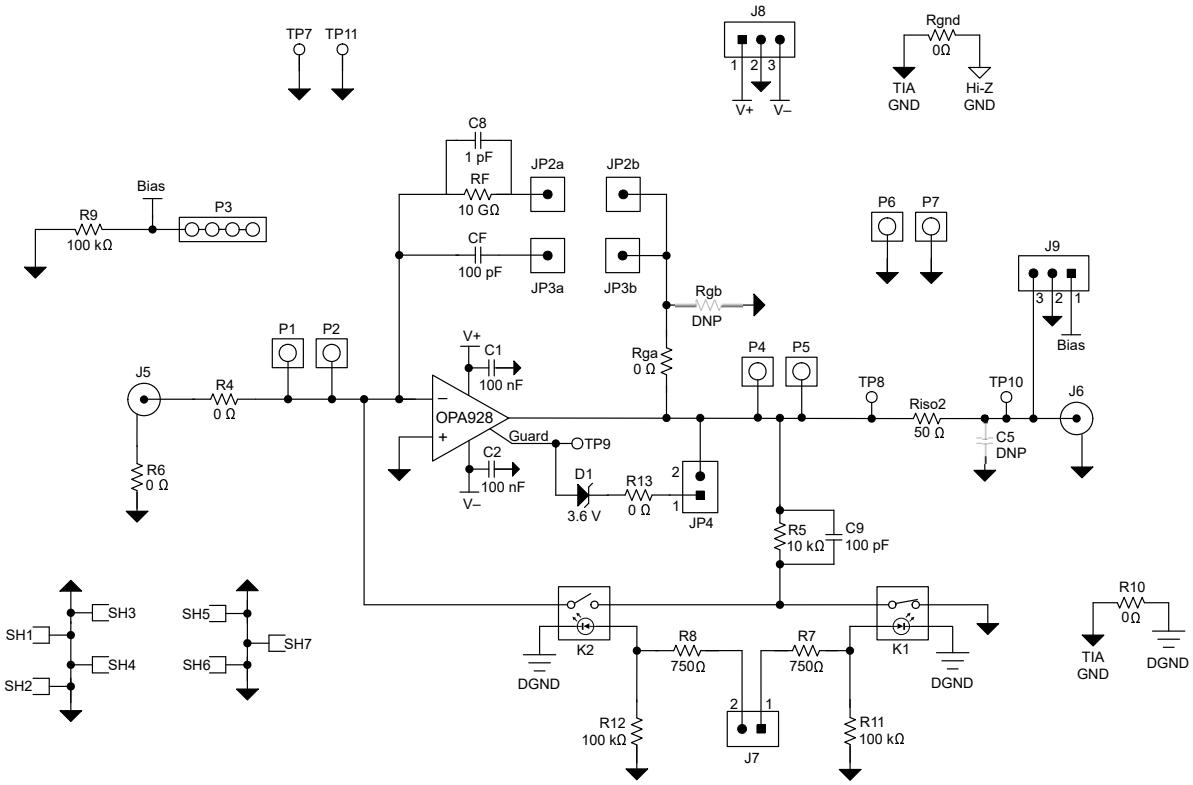


Figure 4-2. TIA Circuit Schematic (Simplified)

The noninverting input of the TIA is tied directly to the analog ground of the TIA circuit. The guard copper surrounding the TIA is grounded as well, which provides very good leakage performance because the offset voltage of a guard driver is not present between the input and guard traces. When using grounded guard traces in a PCB layout, make sure to keep power and digital grounds separate from the guard and prevent ground loops from occurring.

The default feedback path for the TIA consists of a 10-GΩ surface mount resistor (RF) in a resistive transimpedance configuration. The feedback loop can be configured through the pin sockets, or by installing and removing jumpers across certain jumper blocks. Section 4.2.1 describes how to configure the feedback path and other functions of the TIA circuit.

The sensitive input traces and feedback components of the TIA are guarded from leakage currents using the techniques described in Section 2.1. The amplifier, input traces, and SMD feedback components are placed on the bottom of the PCB and are fully enclosed by a grounded RF shield to prevent noise and EMI from coupling into the signal path. For configurability, sensitive input and feedback nodes are also exposed on the top layer at P1, P2, JP2a, and JP3a. The top-side shield encloses these nodes and is sized to accommodate large through-hole components inserted between the TIA pin sockets. If using through-hole components enclosed within the top-side shield, make sure that the component and leads do not come into contact with the shield.

The TIA circuit features two additional functions described in Section 4.2.2. The first function is a low-leakage T-switch that discharges the feedback path to reset measurements in the integrator configuration. The second function uses the OPA928 internal guard buffer in a guarded diode limiter to protect the TIA from overcurrent events. For a detailed description and configuration of these functions, see Section 4.2.2.

4.2.1 Configure the TIA

The TIA is configured through the pin sockets, or by installing and removing jumpers across certain jumper blocks. JP2 and JP3 are separated into single-pin jumper blocks JP2a/JP2b and JP3a/JP3b. Separating these jumper blocks prevents current from leaking through the jumper block material when the jumpers are uninstalled, and allows space for guard copper between the output and any disconnected feedback components. A special length shunt jumper is included in the EVM to connect across JP2 or JP3. The default configuration installs the shunt jumper at JP2, placing the 10-GΩ resistor in the feedback path.

Terminal block J7 and jumper block JP4 control the additional functions described in Section 4.2.2.

Table 4-1 lists the components and connections associated with each jumper block.

Table 4-1. TIA Jumper Block Connections

Designator	Component	Connection With Jumper Shunt Installed
JP2a/JP2b	RF (10 GΩ)	RF in series between IN– and Vout (TIA configuration)
JP3a/JP3b	CF (100 pF)	CF in series between IN– and Vout (integrator configuration)
JP4	D1	D1 in series between Vout and Guard. Limits output voltage. See Section 4.2.2.2
J7	K1, K2	Drives K1, K2 MOS FET relays to discharge feedback. See Section 4.2.2.1

Pin sockets allow easy configuration with through-hole components, such as photodiodes at the input or large value resistors in the feedback path. P3 is a surface-mounted pin socket array that allows through-hole sensors of various sizes to be easily configured at the input. P3 can be driven by the Sensor Bias terminal located at J9.

Table 4-2 lists the nodes associated with each pin socket.

Table 4-2. TIA Pin Socket Configurations

Designator	Node
P1, P2	Inverting Input (U2)
P3	Sensor Bias (J9)
P4, P5	Vout (U2)
P6, P7	Analog Ground (GND)

4.2.2 TIA Functions

The following sections provide a detailed description of the T-switch and guarded diode limiter functions, and how to configure them.

4.2.2.1 T-Switch

The T-switch consists of two MOSFET relays (K1, K2) and one 10-kΩ resistor (R5). To drive the relays, connect two individually controlled 5-V power-supply channels to J7. Figure 4-3 shows the timing diagram for driving K1 and K2 in a break-before-make configuration. From Figure 4-3, t_1, t_2, and t_4 are based on the maximum on and off time of the relays. Follow this timing to prevent the input from being connected directly to ground, which drives the output into the rail. The discharge time (t_3) varies and must be defined by the user.

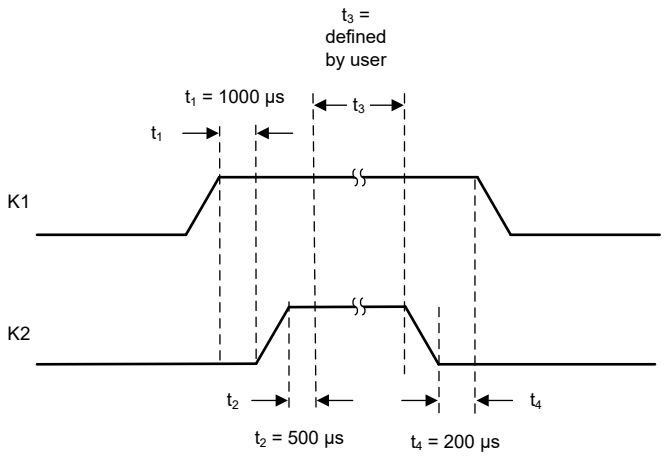


Figure 4-3. T-Switch Timing Diagram

- Logic low (GND) is normal TIA operation
- Logic high (5V) drives the relays, closing the T-switch and discharging the feedback loop

When the pins of J7 are not actively driven, the control logic is pulled to ground by R11 and R12, resulting in a default logic low for normal TIA operation.

Figure 4-4 shows the simplified T-switch circuit in an integrator configuration during normal operation (logic low). The input current source shown is a reverse-biased photodiode. K2 is connected to the input of the integrator and is normally open. K1 is normally closed and connects K2 and R5 to ground. When the T-switch is not active, R5 is a 10-kΩ load to ground at the output of the amplifier. The Omron G3VM-81PR(TR05) MOS FET relay was chosen for K2 for the high insulation resistance and low open-switch capacitance. When K1 is closed and K2 is open, the potential across K2 is nearly 0 V, and the high insulation resistance limits any leakage current to negligible levels. Figure 4-5 shows the functionally equivalent circuit (ignoring switch nonidealities) when the T-switch is logic low.

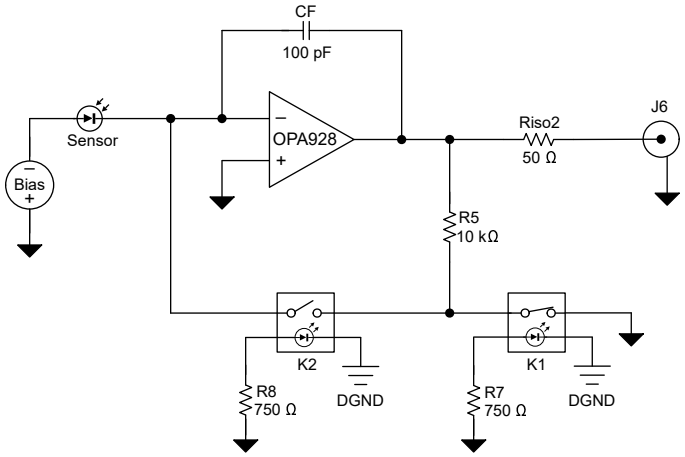


Figure 4-4. T-Switch Logic Low (Normal Operation)

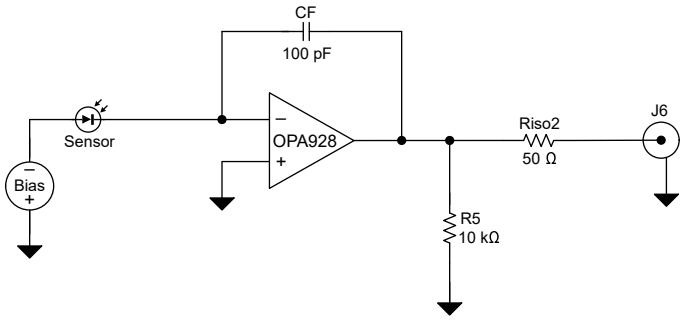


Figure 4-5. T-Switch Logic Low Equivalent Circuit (Normal Operation)

When the T-switch is logic low, the integrating capacitor, CF, accumulates charge that appears as a ramping voltage at the amplifier output. The average current for any measurement period is calculated the following equation.

$$I = C\frac{dV}{dt} \tag{1}$$

where

- I is the average current across the measurement period.
- C is the feedback capacitance.
- dV is the change in voltage across the measurement period.
- dt is the measurement period.

In the case of a unidirectional current source at the input, the integrating capacitor continues to accumulate charge until the amplifier output is driven into the rail and feedback is lost. To prevent the amplifier from railing, drive the T-switch high to discharge the capacitor and reset the measurement.

Figure 4-6 shows the simplified T-switch circuit when the logic is driven high and the feedback is discharged. K1 opens and K2 closes, switching 10-kΩ resistor R5 into the feedback parallel to CF. This 10-kΩ resistor provides

a path for CF to discharge, and the output voltage settles to the level defined by Equation 2. The settling time depends on the output voltage and the RC time constant of the circuit.

$$V = IR \tag{2}$$

where

- V is the output voltage.
- I is the sensor current.
- R is the resistance of the feedback network; in this case, 10 kΩ.

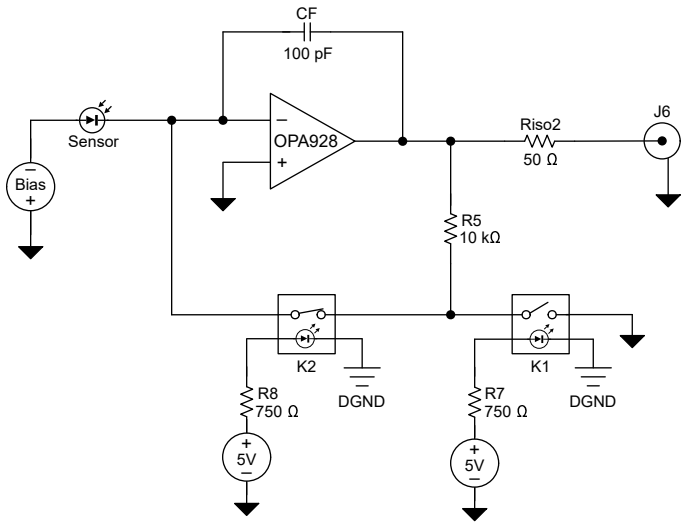


Figure 4-6. T-Switch Logic High (Discharge Feedback)

Figure 4-7 shows the functionally equivalent circuit (ignoring switch nonidealities) when the T-switch is logic high. When K2 is closed and K1 is open, switch K1 presents 100 pF of capacitance at the input of the amplifier. An additional capacitor, C9, is populated in parallel to R5 to maintain stability when the T-switch is active.

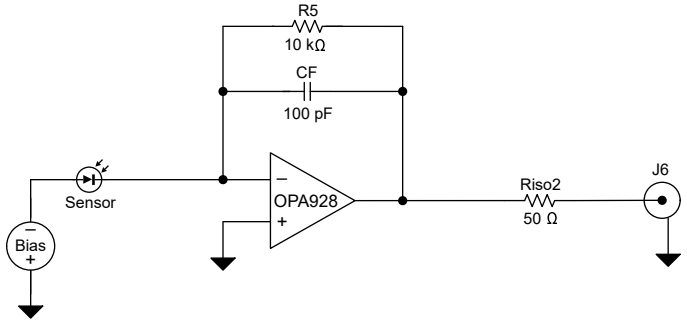


Figure 4-7. T-Switch Logic High Equivalent Circuit (Discharge Feedback)

4.2.2.2 Guarded Diode Limiter

Diode limiter circuits are commonly implemented to prevent the output voltage from exceeding a certain level. These circuits are particularly useful in high-gain applications that are vulnerable to input transients, such as low-level current measurements. On the OPA928EVM, the default TIA configuration is set in a gain of 10,000,000,000 V/A by the 10-GΩ feedback resistor, RF. When using ±5-V supplies, input current spikes greater than 500 pA drive the TIA output into the rail, and feedback is lost.

A typical diode limiter protects a TIA from input overcurrent events by adding a parallel Zener diode in the feedback path. This diode provides an alternate path for large input currents when the output voltage reaches the reverse breakdown voltage of the diode. The reverse breakdown voltage is selected to be less than the maximum output voltage swing of the amplifier, so that the output clips before reaching the rail, and feedback is never lost. The downside of the typical diode limiter circuit is that the Zener diode introduces a leakage path back into the input traces. Instead, the circuit shown in Figure 4-8 takes advantage of the OPA928 internal guard buffer and the internal ESD protection to implement a guarded diode limiter.

The internal guard buffer maintains the input common-mode potential on both sides of the internal ESD diodes. In a fault condition, overcurrent is directed though the ESD diodes and Zener diode, D1, to the output. During normal operation, any leakage current through D1 is directed away from the high-impedance input traces as a load on the guard buffer.

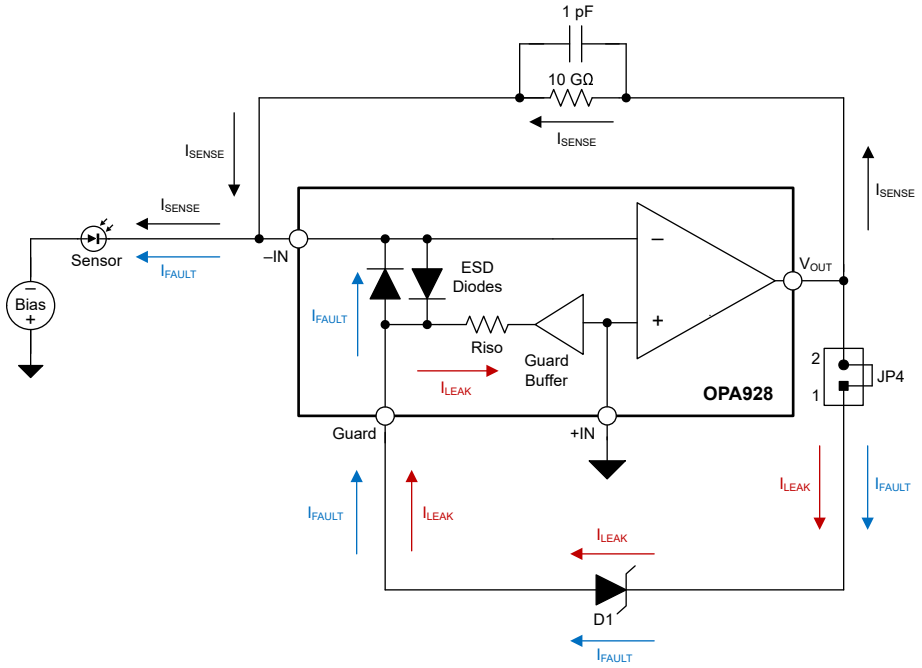


Figure 4-8. Guarded Diode Limiter

To enable this feature on the OPA928EVM, install a shunt jumper at JP4. D1 has a reverse breakdown voltage of 3.6 V. Assuming a maximum voltage of 0.7 V across the internal ESD diodes during the fault condition, and 3.6 V across D1, by Kirchoff's law, the output is limited to a maximum of 4.3 V. To remove the limiter function from the TIA circuit, leave the shunt at JP4 uninstalled, which takes D1 out of the feedback path.

5 Cleaning the EVM

Follow these cleaning instructions whenever the EVM is suspected of contamination within the guard area and performance is degraded.

The recommended cleaning procedure requires access to an ultrasonic bath. If an ultrasonic bath is not available, a manual cleaning procedure is detailed below. The ultrasonic wash produces the best and most consistent outcomes and is preferred over manual cleaning.

Remove all RF shields from the EVM before cleaning and follow the instructions for handling the board as described in the Section 1.1.

5.1 Ultrasonic Wash

1. Place the EVM in the ultrasonic cleaner and fill with fresh deionized (DI) water.
2. Run the ultrasonic cleaner for 30 minutes at 85°C.
3. Remove the EVM from the ultrasonic cleaner and bake for two hours at 100°C

5.2 Manual Cleaning Procedure

1. Flush contaminants from the EVM.
   a. Hold the board by the edges and flush the top and bottom using a combination of fresh isopropyl alcohol (IPA) and fresh DI water. Focus on the input traces, guard copper, and feedback components.
2. Scrub contaminants from top side of the EVM.
   a. Hold the board by the edges with the top layer facing up. Flood sensitive input and feedback areas with fresh IPA.
   b. Use a toothbrush to gently scrub for 30–60 seconds. Focus on the areas surrounding P1, P2, JP2, JP3, SH1, and the area directly right of J1.
   c. Flush the scrubbed areas with fresh DI water, tilting the board to allow runoff to flow away from the input areas.
3. Scrub contaminants from the bottom layer TIA input.
   a. Hold the board by the edges with the bottom layer facing up. Flood sensitive input and feedback areas with fresh IPA.
   b. Use a toothbrush to gently scrub for 30–60 seconds. Focus on areas surrounding U2, R4, Rf, Cf, K2, K1, U1, R1, and all input and guard traces.
   c. Flush the scrubbed areas with fresh DI water, tilting the board to allow runoff to flow away from the input areas.
4. Remove moisture from the PCB.
   a. Bake the EVM for two hours at 100°C.

6 Schematic, PCB Layout, and Bill of Materials

This section provides the OPA928EVM hardware schematics, PCB layout and bill of materials.

6.1 EVM Schematic

Figure 6-1 shows the OPA928EVM Hi-Z schematic.

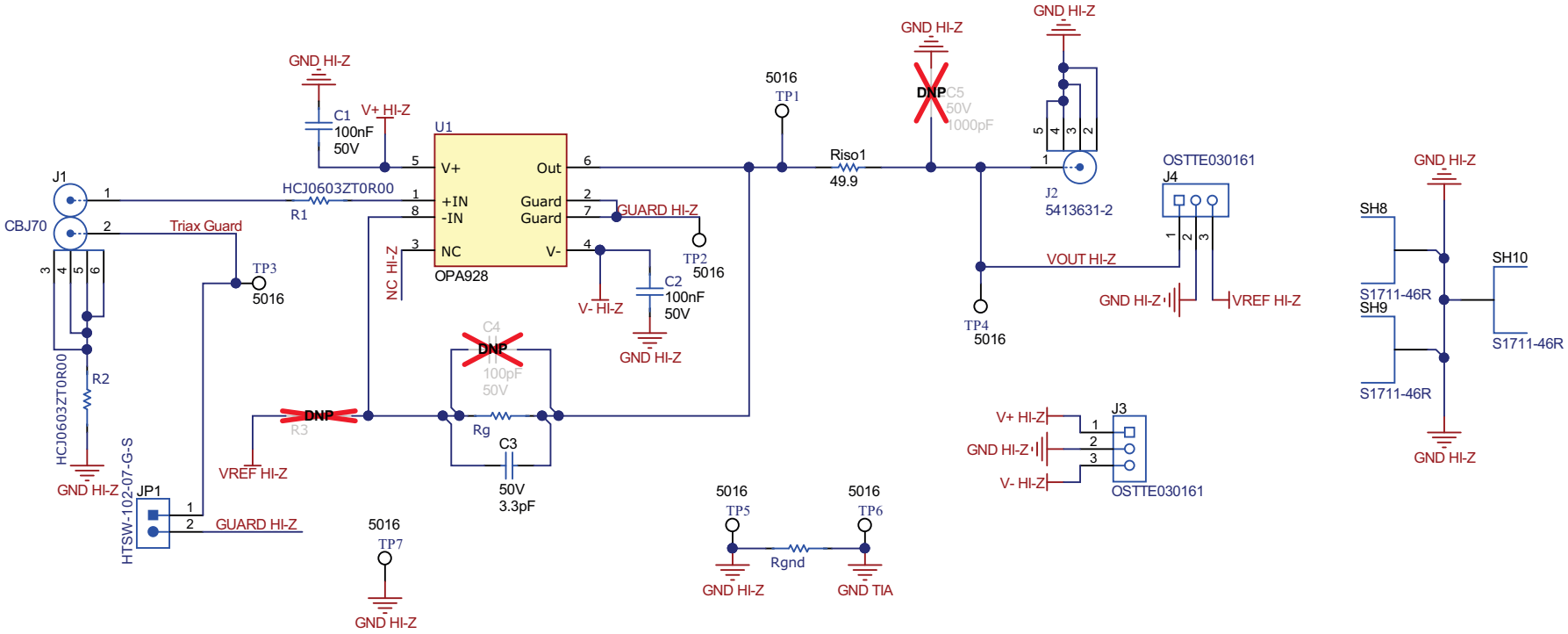


Figure 6-1. OPA928EVM Hi-Z Schematic

Figure 6-2 shows the OPA928EVM TIA schematic.

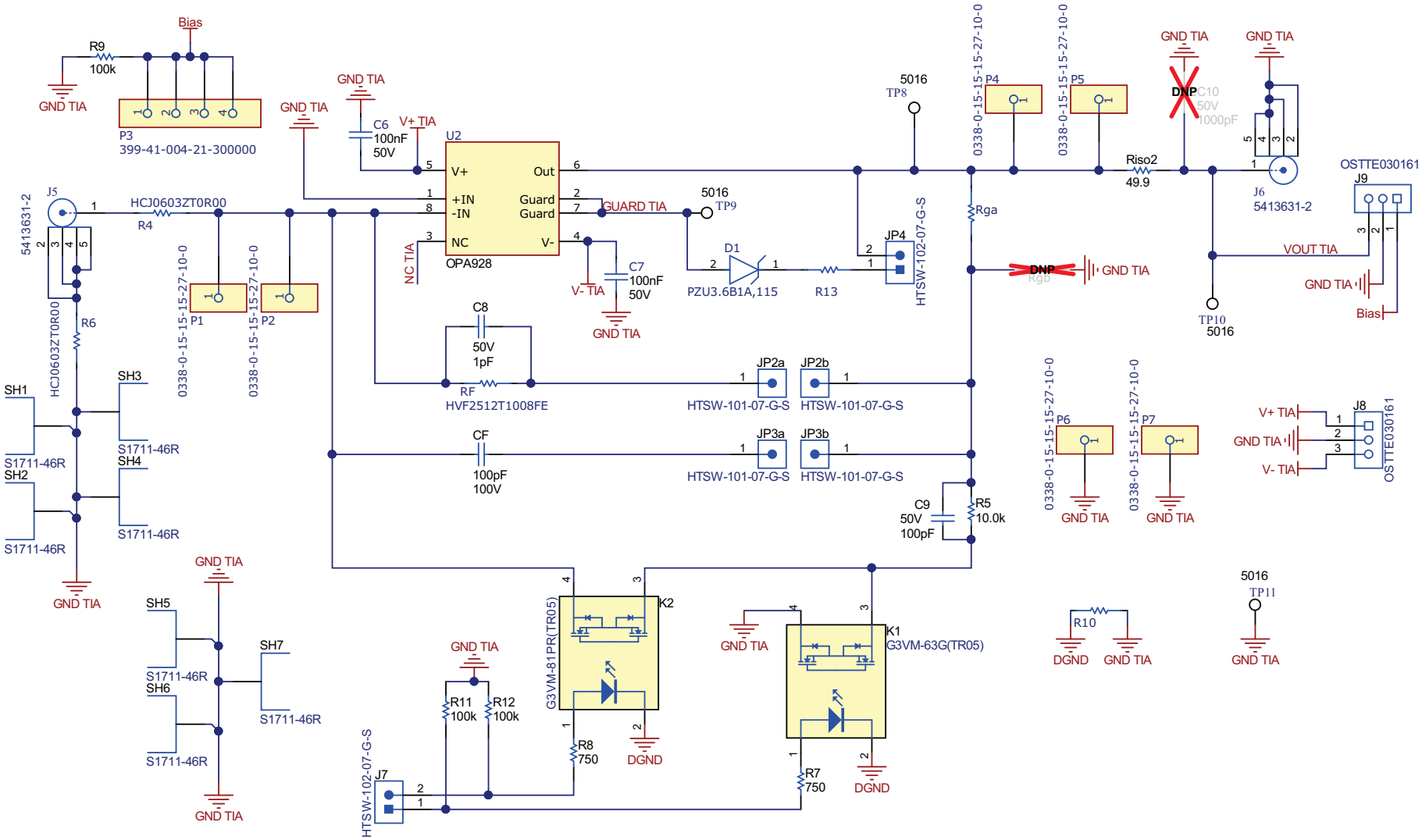


Figure 6-2. OPA928EVM TIA Schematic

6.2 PCB Layout

The OPA928EVM is a four-layer PCB. Figure 6-3 to Figure 6-10 show the PCB layer illustrations. The top layer consists of the configuration circuitry and output signal traces and is poured with a solid ground plane. The second layer routes the power supply connections. The third layer provides an additional layer of guard copper directly above all guard copper on the bottom layer for three-dimensional guarding. The bottom layer consists of the sensitive input traces, sensitive feedback circuitry, and guard traces and is poured with a solid ground plane. The top and bottom solder mask layers are included to show where the solder mask was removed from guard copper and RF shield mount areas.

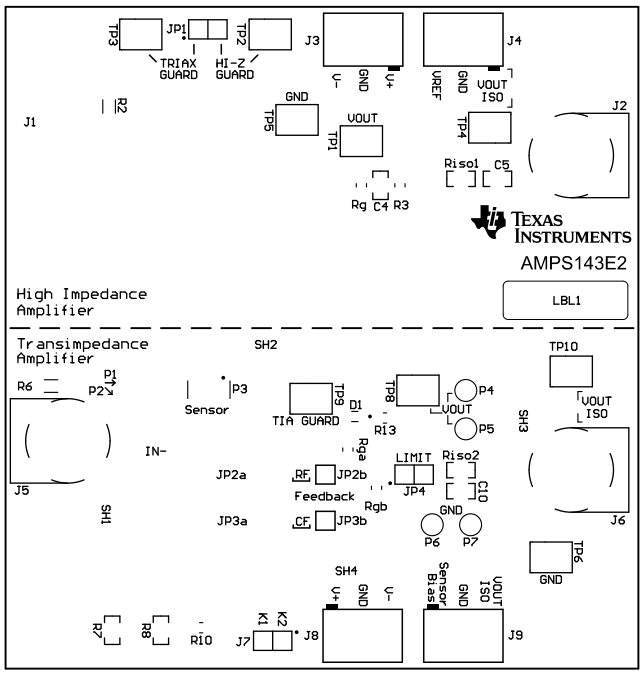


Figure 6-3. Top Overlay

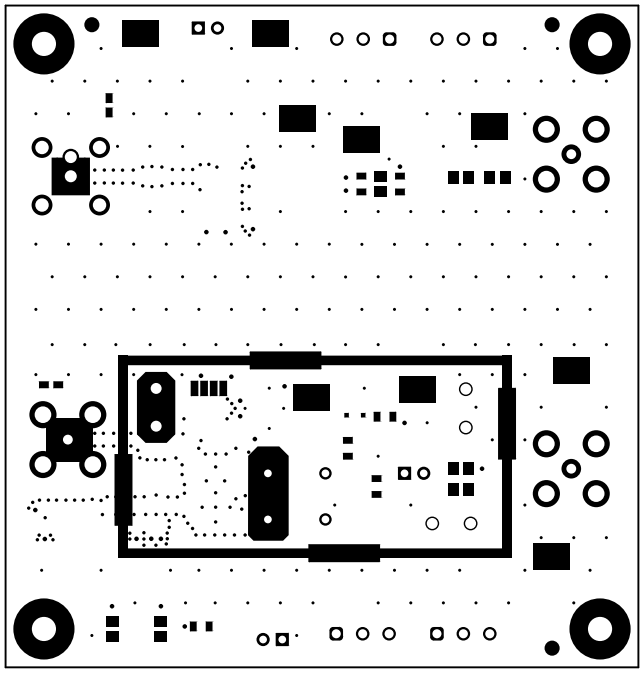


Figure 6-4. Top Solder Mask

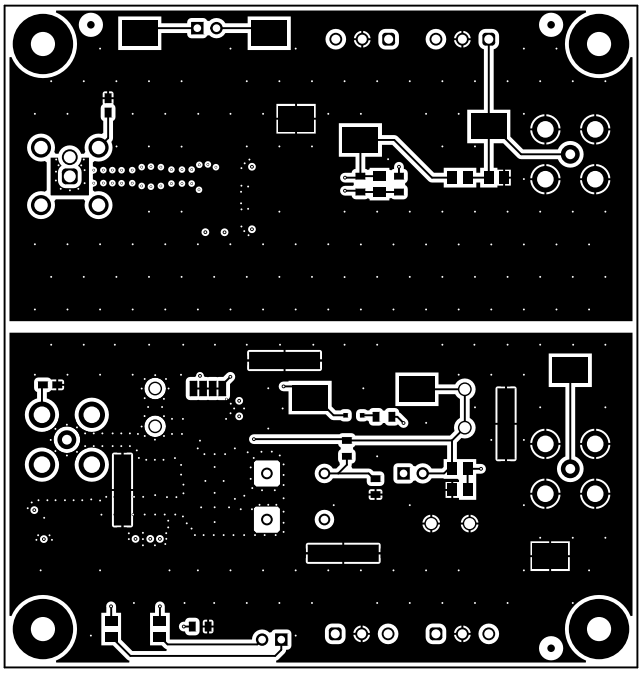


Figure 6-5. Top Layer PCB Layout

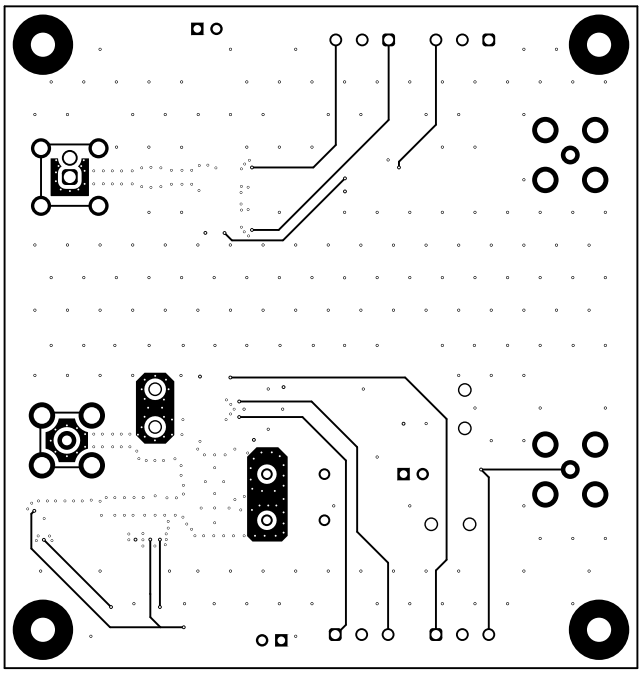


Figure 6-6. Internal Power Layer PCB Layout

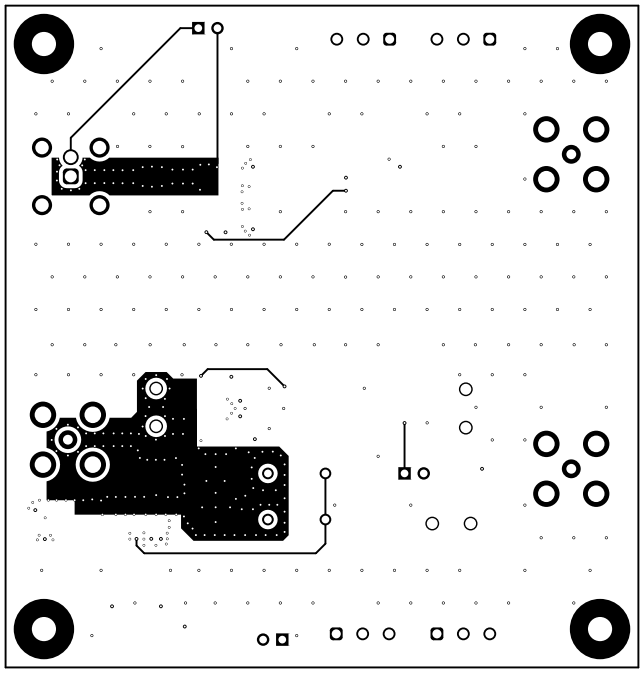


Figure 6-7. Internal Guard Layer PCB Layout

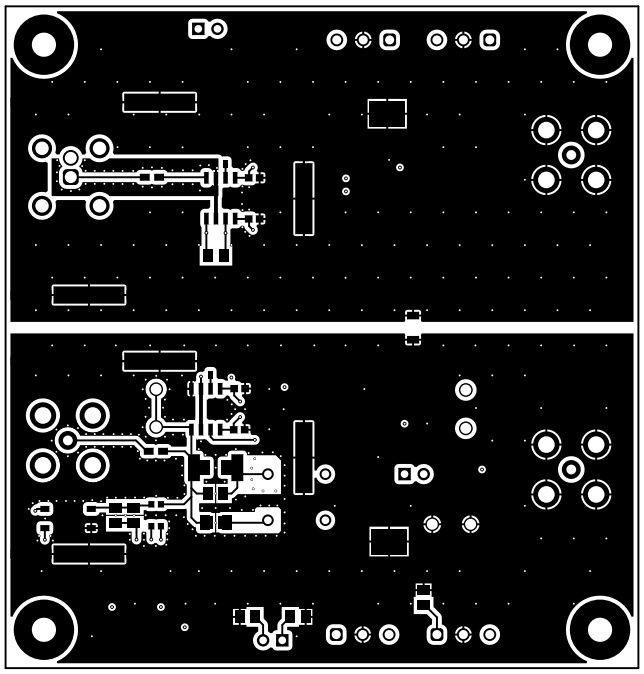


Figure 6-8. Bottom Layer PCB Layout

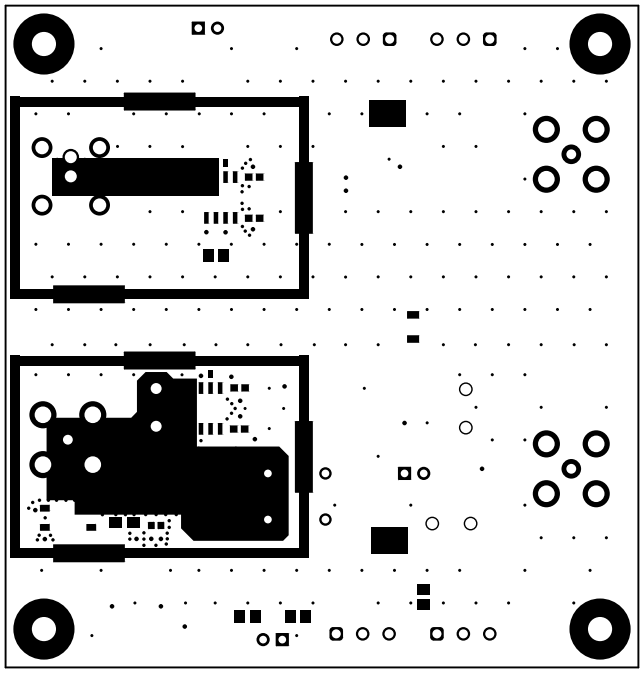


Figure 6-9. Bottom Solder Mask

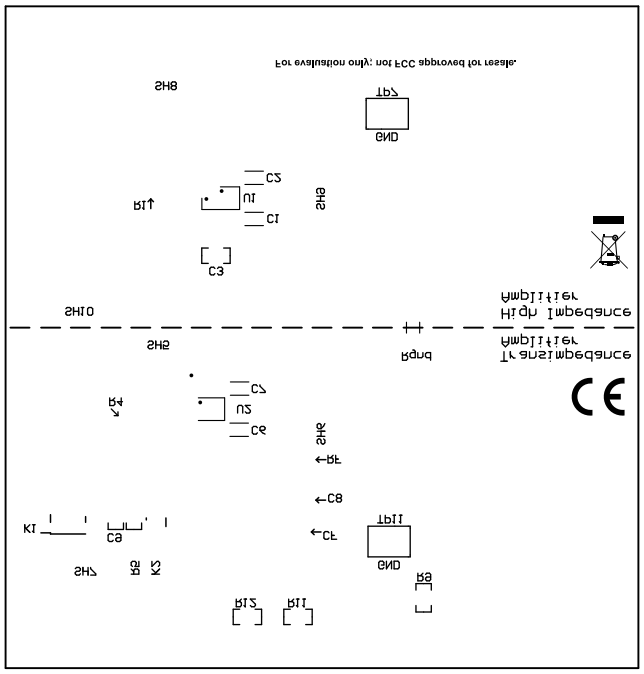


Figure 6-10. Bottom Overlay

6.3 Bill of Materials

Table 6-1 lists the bill of materials (BOM) used for the OPA928EVM.

Table 6-1. OPA928EVM Bill of Materials

Designator	Quantity	Value	Description	Package Reference	PartNumber	Manufacturer
C1, C2, C6, C7	4	100 nF	0.1 µF ±10% 50V Ceramic Capacitor X7R 0603 (1608 Metric)	0603	C0603C104K5RAC7081	KEMET
C3	1	3.3 pF	CAP, CERM, 3.3 pF, 50 V, +/- 8%, C0G/NP0, 0805	0805	08055A3R3CAT2A	AVX
C8	1	1 pF	CAP, CERM, 1 pF, 50 V, +/- 25%, C0G/NP0, 0805	0805	08055A1R0CAT2A	AVX
C9	1	100 pF	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0805	0805	CL21C101JBANNNC	Samsung Electro-Mechanics
CF	1	100 pF	CAP, CERM, 100 pF, 100 V, +/- 1%, C0G/NP0, 0805	0805	08051A101FAT2A	AVX
D1	1		Zener Diode 3.6 V 320 mW ±2% Surface Mount SOD-323	SOD-323	PZU3.6B1A,115	Nexperia
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B&F Fastener Supply
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone
J1	1		Connector Jack, TH	Connector Jack, TH	CBJ70	Cinch Connectivity
J2, J5, J6	3		Connector, TH, BNC Right angle, 50 ohm gold	5413631-2	5413631-1	AMP
J3, J4, J8, J9	4		Terminal Block, 3.5mm, 3x1, Tin, R/A, TH	Terminal Block, 3.5mm, 3x1, TH	OSTTE030161	On-Shore Technology
J7, JP1, JP4	3		Header, 100mil, 2x1, Gold, TH	Header, 100mil, 2x1, TH	HTSW-102-07-G-S	Samtec
JP2a, JP2b, JP3a, JP3b	4		Header, 2.54mm, 1x1, Gold, TH	Header, 2.54mm, 1x1, TH	HTSW-101-07-G-S	Samtec
K1	1		Relay, SPST-NC (1 Form B), 0.5 A, SMD	SMD, 4.4x2.1x3.9mm	G3VM-63G(TR05)	Omron Electronic Components
K2	1		Relay, SPST-NO (1 Form A), 0.12 A, SMD	SMD, 2.85x2.2mm	G3VM-81PR(TR05)	Omron Electronic Components
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady
MP1	1		Standard RF Shield 1.0 x 2.0 x 0.75	RF_SHIELD	1.0 x 2.0 x 0.75	Fotofab
MP2, MP3	2		Standard RF Shield 1.0 x 1.5 x 0.25	RF_SHIELD	1.0 x 1.5 x 0.25	Fotofab

Table 6-1. OPA928EVM Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	PartNumber	Manufacturer
P1, P2, P4, P5, P6, P7	6		Pin Receptacle Connector 0.020" - 0.032" (0.51mm - 0.81mm) No Tail Solder	PTH	0338-0-15-15-15-27-10-0	Mill-Max
P3	1		4 Position Socket Connector 0.050" (1.27mm) Surface Mount Gold	CONN_SCKT4	399-41-004-21-300000	Mill-Max
R1, R2, R4, R6	4	0 Ω	RES 0 OHM JUMPER 1/4W 0603	0603	HCJ0603ZT0R00	Stackpole Electronics
R5	1	10.0 kΩ	10 kOhms ±1% 0.25W, 1/4W Chip Resistor 0805 (2012 Metric) Anti-Sulfur Thin Film	0805	RNCP0805FTD10K0	Stackpole Electronics
R7, R8	2	750 Ω	RES, 750, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	CRCW0805750RFKEA	Vishay-Dale
R9, R11, R12	3	100 kΩ	RES, 100 k, 1%, 0.2 W, 0805	0805	RMCF0805FT100K	Stackpole Electronics
R10, R13, Rg, Rga	4		0 Ohms Jumper 0.125W, 1/8W Chip Resistor 0805 (2012 Metric) Automotive AEC-Q200 Thick Film	0805	RMCF0805ZT0R00	Stackpole Electronics
RF	1	10 GΩ	10 GOhms ±10% 0.25W, 1/4W Chip Resistor 1206 (3216 Metric) High Voltage Thick Film	1206	HVC1206Z1008KET	Ohmite
Rgnd	1	0 Ω	0Ω ±0 0.25W 1206 Thick Film Chip Resistor AEC-Q200 compliant	1206	RMCF1206ZT0R00	Stackpole Electronics
Riso1, Riso2	2	49.9 Ω	RES, 49.9, 1%, 0.25 W, AEC-Q200 Grade 0, 0805	0805	RNCP0805FTD49R9	Stackpole Electronics Inc
SH1, SH2, SH3, SH4, SH5, SH6, SH7, SH8, SH9, SH10	10		RFI SHIELD CLIP TIN SMD	RFI SHIELD CLIP	S1711-46R	Harwin
SH-J1	1	1x2	Shunt, 100mil, Flash Gold, Black	Closed Top 100mil Shunt	SPC02SYAN	Sullins Connector Solutions
SH-J2	1		4 (1 x 4) Position Shunt Connector Black Open Top 0.100" (2.54mm) Gold or Gold, GXT™	JUMPER	69144-204LF	Amphenol ICC

Table 6-1. OPA928EVM Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	PartNumber	Manufacturer
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11	11		Test Point, Compact, SMT	Testpoint_Keystone_Compact	5016	Keystone
U1, U2	2		16-V, fA Input Bias, Precision, CMOS, Rail-to-Rail Input/Output Operational Amplifier, SOIC8	SOIC8	OPA928	Texas Instruments
C4	0	DNP	CAP	0805	N/A	Any
C5, C10	0	DNP	CAP	0805	N/A	Any
FID1, FID2, FID3	0	DNP	Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
R3, Rgb	0	DNP	RES	0805	N/A	Any

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社

東京都新宿区西新宿 6 丁目 2 4 番 1 号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265