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DS50002707B

dsPIC33CH128MP508 Plug-In Module (PIM) Information Sheet

Overview

The dsPIC33CH128MP508 General Purpose Explorer 16/32 PIM (MA330040) is designed to demonstrate the capabilities of the dsPIC33CH128MP508 family using the Explorer 16 or Explorer 16/32 Development Board. Refer to Table 1 and Table 2 for the mapping of the physical pins on the dsPIC33CH128MP508 to the 100 pins on the PIM connector.

Not all predefined PIM signals found on the Explorer 16/32 are connected due to the limited amount of I/O pins available.

The dsPIC33CH128MP508 is a dual core device. The Master core, as well the Slave, can be debugged and programed using this PIM. Since there are two cores available in the dsPIC33CH128MP508 device, there are multiple ways to program and debug the Master and the Slave. The four scenarios are:

1. Master = Release, Slave = Release
2. Master = Debug, Slave = Release
3. Master = Release, Slave = Debug
4. Master = Debug, Slave = Debug (e.g., "Dual Debug" mode)

In scenarios 1, 2 and 3, only a single programmer/debugger tool is needed, and it should be connected to the PIM via the Explorer 16 (or Explorer 16/32) In-Circuit Serial Programming™ (ICSP™) interface.

In scenario 4 only ("Dual Debug" of both cores simultaneously), two debugger tools are required. In this scenario, the debugger connected via the Explorer 16 (or Explorer 16/32) ICSP interface is used to debug the Master core, while the second debugger is intended to be connected directly to the PIM via the 6-pin in-line ICSP interface J2 on the PIM. When using the Explorer 16/32, the PICkit™-On-Board (PKOB) circuit would typically be used to debug the Master core (thus requiring only one additional debugger tool in this scenario). The pins of J2 are slightly staggered to provide some retention friction, for temporary use, without requiring solder.

Demo Overview

This demo project provides a basic demonstration of how to use both the Master and Slave cores within the dsPIC33CH128MP508, and how to use the Master/Slave core interface for sending data between the cores.

The `master.X` includes/uses the `slave.X` project. Therefore, attempting to build and program the `master.X` project should have the effect of simultaneously building and programming both the Master and Slave core program code into the device.

During execution, the demo performs the following operations:

1. Periodically takes ADC measurements on the potentiometer on the Explorer 16/32 and prints the results to the LCD screen.
2. Periodically computes the value of "pi" and prints the results to the LCD screen.
3. Blinks an LED (D10 on the Explorer 16/32).
4. Samples the S3 and S6 push buttons (used for "mode" switching).

The demo has two primary operating modes:

Mode 1: Uses only the Master core to perform all application tasks, or

Mode 2: Uses the Master core to perform user interface related tasks (ex: LCD printing, LED blinking, ADC measurements), while the Slave core is used to perform mathematical computations (computes "pi").

While operating in Mode 1, both the pi computations and other tasks are all performed on the Master core only, and since the pi computation is written as blocking code, it temporarily blocks the operation of the other application tasks (ex: ADC POT measurements, LED blinking and LCD screen updates are temporary halted while the pi computation is in progress).

While operating in Mode 2, the pi computations do not interrupt/interfere with the other application operations (such as ADC POT measurements and LCD printing), since the tasks are being performed on separate cores. In Mode 2, when a pi computation is complete, the value is sent to the Master core through the Master/Slave interface mailboxes, and the master core is responsible for printing the pi result to the LCD screen (along with the POT value data).

To operate the application in Mode 1 (Master only), press the "S3" push button on the Explorer 16/32 Development Board when prompted to do so on the LCD screen. Alternatively, to operate in Mode 2 (Master + Slave), press the "S6" push button.

To appreciate the difference between the two operating modes, it is suggested to continuously adjust the POT while the demo is running (and to compare the difference in LCD updating behavior between the modes).

Table 1: dsPIC33CH128MP508 PIM Mapping

PIM Pin #	Device Pin # (80-Pin TQFP)	dsPIC33CH128MP508 I/Os	Function	Explorer 16/32 Net Name
1	—	—	—	P1_VBUS
2	12, 25, 31, 51, 71	VDD + AVDD	VDD	VDD_PIM
3	64	ASDA2/RE13/S1RE13	LCD D5	P3_LCDD5
4	77	RE14/S1RE14	LCD D6	P4_LCDD6
5	79	RE15/S1RE15	LCD D7	P5_LCDD7
6	16	AN0/CMP1A/RA0/S1RA0	General Purpose I/O	P6
7(1)	—	—	—	P7
8(1)	—	—	—	P8
9(1)	—	—	—	P9
10	29	AN14/ISRC1/RP50/RC2/S1ANA0/S1RP50/S1RC2	mikroBUS™ A SPI SCK	P10_SCKA
11	53	RP70/RD6/S1RP70/S1PWM6H/S1RD6	mikroBUS A SPI MISO	P11_MISOA
12	33	CMP1B/RP51/RC3/S1AN8/S1CMP3B/S1RP51/S1RC3	mikroBUS A SPI MOSI	P12_MOSIA
13	9	$\overline{\text{MCLR}}$	$\overline{\text{MCLR}}$ Reset	P13_$\overline{\text{MCLR}}$
14	69	RP67/RD3/S1RP67/S1PWM3L/S1RD3	mikroBUS A Chip Select	P14_CSA
15	11, 26, 32, 50, 70	VSS + AVSS	VSS	VSS
16	12, 25, 31, 51, 71	VDD + AVDD	VDD	VDD_PIM
17	2	RE0/S1RE0	LED D3	P17_LED3
18	80	RP45/PWM2L/RB13/S1RP45/S1RB13	mikroBUS B Interrupt	P18_INTB
19	30	RP54/RC6/S1AN11/S1CMP1B/S1RP54/S1RC6	mikroBUS B Reset	P19_RSTB
20	21	AN3/IBIAS0/RA3/S1AN0/S1CMP1A/S1PGA1P1/S1RA3	10k Potentiometer	P20_POT
21	18	AN1/RA1/S1AN15/S1RA1	TC1047A Temp. Sensor	P21_TEMP
22	28	AN13/ISRC0/RP49/RC1/S1ANA1/S1RP49/S1RC1	General Purpose I/O	P22
23	58	TDO/AN9/RP39/RB7/S1MCLR1/S1AN6/S1RP39/ S1PWM5H/S1RB7	mikroBUS B Chip Select	P23_CSB
24	41	DACOUT/AN7/CMP1D/RP34/INT0/RB2/$\overline{\text{S1MCLR2}}$/ S1AN3/S1ANC0/S1ANC1/S1CMP1D/S1CMP2D/ S1CMP3D/S1RP34/S1INT0/S1RB2	mikroBUS B Analog	P24_ANB
25	40	AN15/ISRC2/RP55/RC7/S1AN12/S1RP55/S1RC7	mikroBUS A Analog	P25_ANA_USBOC
26	45	PGC2/RP36/RB4/S1PGC2/S1AN9/S1RP36/S1PWM5L/ S1RB4	ICSP™ Prog/Debug PGC2	P26_PGC
27	43	PGD2/AN8/RP35/RB3/S1PGD2/S1AN18/S1CMP3A/ S1PGA3P1/S1RP35/S1RB3	ICSP Prog/Debug PGD2	P27_PGD
28	36	RD11/S1AN17/S1PGA1P2/S1RD11	General Purpose I/O	P28
29	27	RD12/S1AN14/S1PGA2P2/S1RD12	General Purpose I/O	P29
30	12, 25, 31, 51, 71	VDD + AVDD	VDD	VDD_PIM
31	11, 26, 32, 50, 70	VSS + AVSS	VSS	VSS
32	20	AN2/RA2/S1AN16/S1RA2	General Purpose I/O	P32_CC2
33	15	AN12/IBIAS3/RP48/RC0/S1AN10/S1RP48/S1RC0	General Purpose I/O	P33_CC1
34	—	—	—	P34
35	—	—	—	P35
36	11, 26, 32, 50, 70	VSS + AVSS	VSS	VSS
37	12, 25, 31, 51, 71	VDD + AVDD	VDD	VDD_PIM
38	4	RE1/S1RE1	LED D4	P38_LED4
39	75	TMS/RP42/PWM3H/RB10/S1RP42/S1RB10	General Purpose I/O	P39
40	76	TCK/RP43/PWM3L/RB11/S1RP43/S1RB11	General Purpose I/O	P40
41	—	—	—	P41
42	—	—	—	P42
43	—	—	—	P43
44	59	RE11/S1RE11	LCD Register Select	P44_LCDRS
45	11, 26, 32, 50, 70	VSS + AVSS	VSS	VSS
46	12, 25, 31, 51, 71	VDD + AVDD	VDD	VDD_PIM
47	7	RP62/RC14/S1RP62/S1PWM7H/S1RC14	General Purpose I/O	P47
48	8	RP63/RC15/S1RP63/S1PWM7L/S1RC15	General Purpose I/O	P48
49	66	RP58/RC10/S1RP58/S1PWM1H/S1RC10	MCP2221A/mikroBUS B RX	P48
50	67	RP59/RC11/S1RP59/S1PWM1L/S1RC11	MCP2221A/mikroBUS B TX	P49_RXB

Note 1: These pins can optionally be connected to the microcontroller if jumper resistors R1, R2 and R3 are populated.

Table 1: dsPIC33CH128MP508 PIM Mapping (Continued)

PIM Pin #	Device Pin # (80-Pin TQFP)	dsPIC33CH128MP508 I/Os	Function	Explorer 16/32 Net Name
51	73	RP65/RD1/S1RP65/S1PWM4H/S1RD1	mikroBUS™ A TX	P51_TXA
52	74	RP64/RD0/S1RP64/S1PWM4L/S1RD0	mikroBUS A RX	P52_RXA
53	49	SDO2/PCI19/RD8/S1SDO1/S1PCI19/S1RD8	mikroBUS B MOSI	P53_MOSIB
54	47	RP57/ASCL1/SDI2/RC9/S1RP57/S1ASCL1/S1SDI1/ S1RC9	mikroBUS B MISO	P54_MISOB
55	46	RP56/ASDA1/SCK2/RC8/S1RP56/S1ASDA1/ S1SCK1/S1RC8	mikroBUS B SPI SCK	P55_SCKB
56	61	PGC1/AN11/RP41/SDA1/RB9/S1PGC1/S1RP41/ S1SDA1/S1RB9	Shared I2C SDA	P56_SDA
57	60	PGD1/AN10/RP40/SCL1/RB8/S1PGD1/S1AN7/ S1RP40/S1SCL1/S1RB8	Shared I2C SCL	P57_SCL
58	17	RE2/S1RE2	LED D5	P58_LED5
59	19	RE3/S1RE3	LED D6	P59_LED6
60	22	RE4/S1RE4	LED D7	P60_LED7
61	24	RE5/S1RE5	LED D8	P61_LED8
62	12, 25, 31, 51, 71	VDD + AVDD	VDD	VDD_PIM
63	34	OSCI/CLKI/AN5/RP32/RB0/S1AN5/S1RP32/S1RB0	Primary Oscillator In	P63_OSCI
64	35	OSCO/CLKO/AN6/IBIAS2/RP33/RB1/ S1AN4/ S1RP33/S1RB1	Primary Oscillator Out	P64_OSCO
65	11, 26, 32, 50, 70	VSS + AVSS	VSS	VSS
66	78	TDI/RP44/PWM2H/RB12/S1RP44/S1RB12	General Purpose I/O	P66
67	72	RP66/RD2/S1RP66/S1PWM8L/S1RD2	mikroBUS A Interrupt	P67_INTA
68	14	RD13/S1ANN0/S1PGA1N2/S1RD13	General Purpose I/O	P68
69	65	RP53/RC5/S1RP53/S1PWM2L/S1RC5	General Purpose I/O	P69
70	13	PCI21/RD14/S1ANN1/S1PGA2N2/S1PCI21/S1RD14	General Purpose I/O	P70
71	—	—	—	P71
72	3	RP47/PWM1L/RB15/S1RP47/S1RB15	mikroBUS A PWM	P72_PWMA
73	—	—	—	P73_SOSCI
74	—	—	—	P74_SOSCO
75	11, 26, 32, 50, 70	VSS + AVSS	VSS	VSS
76	38	ISRC3/RD10/S1AN13/S1CMP2B/S1RD10	General Purpose I/O	P76
77	—	—	—	P77
78	63	RP52/RC4/S1RP52/S1PWM2H/S1RC4	mikroBUS B PWM	P78_PWMB
79	10	PCI22/RD15/S1PCI22/S1RD15	EEPROM Chip Select	P79_EECS
80	44	RE9/S1RE9	Button S4	P80_S4
81	57	RE10/S1RE10	LCD E	P81_LCDE
82	—	—	LCD R/nW (pulled low by R4)	P82_LCDRW
83	1	RP46/PWM1H/RB14/S1RP46/S1RB14	Button S3	P83_S3
84	42	RE8/S1RE8	Button S6	P84_S6
85	—	—	—	P85_VDDCORE
86	—	—	—	P86_ENVREG
87	5	RP60/PWM4H/RC12/S1RP60/S1RC12	General Purpose I/O	P87
88	6	RP61/PWM4L/RC13/S1RP61/S1RC13	General Purpose I/O	P88
89	52	RP71/RD7/S1RP71/S1PWM8H/S1RD7	General Purpose I/O	P89_USBDN
90	54	RP69/RD5/S1RP69/S1PWM6L/S1RD5	General Purpose I/O	P90_USBDP
91	37	RE6/S1PGA3N2/S1RE6	LED D9	P91_LED9
92	39	RE7/S1RE7	Button S5, LED D10	P92_S5_LED10
93	—	—	—	P93_LCDD0
94	—	—	—	P94_LCDD1
95	68	RP68/RD4/S1RP68/S1PWM3H/S1RD4	mikroBUS A Reset Pin	P95_RSTA
96	48	PCI20/RD9/S1PCI20/S1RD9	General Purpose I/O	P96_VBUSON
97	—	—	—	P97
98	—	—	—	P98_LCDD2
99	—	—	—	P99_LCDD3
100	62	ASCL2/RE12/S1RE12	LCD D4	P100_LCDD4

Note 1: These pins can optionally be connected to the microcontroller if jumper resistors R1, R2 and R3 are populated.

Table 2: dsPIC33CH128MP508 PIC® MCU Mapping

Device Pin # (80-Pin TQFP)	PIM Pin #	dsPIC33CH128MP508 I/Os	Function	Explorer 16/32 Net Name
1	83	RP46/PWM1H/RB14/S1RP46/S1RB14	Button S3	P83_S3
2	17	RE0/S1RE0	LED D3	P17_LED3
3	72	RP47/PWM1L/RB15/S1RP47/S1RB15	mikroBUS™ A PWM	P72_PWMA
4	38	RE1/S1RE1	LED D4	P38_LED4
5	87	RP60/PWM4H/RC12/S1RP60/S1RC12	General Purpose I/O	P87
6	88	RP61/PWM4L/RC13/S1RP61/S1RC13	General Purpose I/O	P88
7	47	RP62/RC14/S1RP62/S1PWM7H/S1RC14	General Purpose I/O	P47
8	48	RP63/RC15/S1RP63/S1PWM7L/S1RC15	General Purpose I/O	P48
9	13	$\overline{\text{MCLR}}$	$\overline{\text{MCLR}}$ Reset	P13_MCLR
10	79	PCI22/RD15/S1PCI22/S1RD15	EEPROM Chip Select	P79_EECS
11, 26, 32, 50,70	15	VSS + AVSS	VSS	VSS
12, 25, 31, 51, 71	16	VDD + AVDD	VDD	VDD_PIM
13	70	PCI21/RD14/S1ANN1/S1PGA2N2/S1PCI21/S1RD14	General Purpose I/O	P70
14	68	RD13/S1ANN0/S1PGA1N2/S1RD13	General Purpose I/O	P68
15	33	AN12/IBIAS3/RP48/RC0/S1AN10/S1RP48/S1RC0	General Purpose I/O	P33_CC1
16	6	AN0/CMP1A/RA0/S1RA0	General Purpose I/O	P6
17	58	RE2/S1RE2	LED D5	P58_LED5
18	21	AN1/RA1/S1AN15/S1RA1	TC1047A Temp. Sensor	P21_TEMP
19	59	RE3/S1RE3	LED D6	P59_LED6
20	32	AN2/RA2 /S1AN16/S1RA2	General Purpose I/O	P32_CC2
21	20	AN3/IBIAS0/RA3/S1AN0/S1CMP1A/S1PGA1P1/S1RA3	10K Potentiometer	P20_POT
22	60	RE4/S1RE4	LED D7	P60_LED7
23[1]	NC	$\overline{\text{SMCLR3}}$/AN4/S1AN1/ S1CMP2A/S1PGA2P1/ S1PGA3P2/IBIAS1/ RA4/S1RA4	—	—
24	61	RE5/S1RE5	LED D8	P61_LED8
12, 25, 31, 51, 71	62	VDD + AVDD	VDD	VDD_PIM
11, 26, 32, 50, 70	65	VSS + AVSS	VSS	VSS
27	29	RD12/S1AN14/S1PGA2P2/S1RD12	General Purpose I/O	P29
28	22	AN13/ISRC0/RP49/RC1/S1ANA1/S1RP49/S1RC1	General Purpose I/O	P22
29	10	AN14/ISRC1/RP50/RC2/S1ANA0/S1RP50/S1RC2	mikroBUS A SPI SCK	P10_SCKA
30	19	RP54/RC6/S1AN11/S1CMP1B/S1RP54/S1RC6	mikroBUS B Reset	P19_RSTB
12, 25, 31, 51, 71	16	VDD + AVDD	VDD	VDD_PIM
11, 26, 32, 50, 70	15	VSS + AVSS	VSS	VSS
33	12	CMP1B/RP51/RC3/S1AN8/S1CMP3B/S1RP51/S1RC3	mikroBUS A SPI MOSI	P12_MOSIA
34	63	OSCI/CLKI/AN5/RP32/RB0/S1AN5/S1RP32/S1RB0	Primary Oscillator In	P63_OSCI
35	64	OSCO/CLKO/AN6/IBIAS2/RP33/RB1/S1AN4/S1RP33/ S1RB1	Primary Oscillator Out	P64_OSCO
36	28	RD11/S1AN17/S1PGA1P2/S1RD11	General Purpose I/O	P28
37	91	RE6/S1PGA3N2/S1RE6	LED D9	P91_LED9
38	76	ISRC3/RD10/S1AN13/S1CMP2B/S1RD10	General Purpose I/O	P76
39	92	RE7/S1RE7	Button S5/LED D10	P92_S5_LED10
40	25	AN15/ISRC2/RP55/RC7/S1AN12/S1RP55/S1RC7	mikroBUS A Analog	P25_ANA_USBOC
40	50	RC12/U1TX	MCP2221A and mikroBUS B TX	P50_TXB

Note 1: These pins are connected to "Dual Debug" header J2. They can optionally be connected to the Explorer 16/32 if R1, R2 and R3 are populated with jumper resistors.

Table 2: dsPIC33CH128MP508 PIC® MCU Mapping (Continued)

Device Pin # (80-Pin TQFP)	PIM Pin #	dsPIC33CH128MP508 I/Os	Function	Explorer 16/32 Net Name
41	24	DACOUT/AN7/CMP1D/RP34/INT0/RB2/$\overline{\text{S1MCLR2}}$/S1AN3/ S1ANC0/S1ANC1/S1CMP1D/S1CMP2D/S1CMP3D/S1RP34/ S1INT0/S1RB2	mikroBUS B Analog	P24_ANB
42	84	RE8/S1RE8	Button S6	P84_S6
43	27	PGD2/AN8/RP35/RB3/S1PGD2/S1AN18/S1CMP3A/ S1PGA3P1/S1RP35/S1RB3	ICSP™ Prog/Debug PGD2	P27_PGD
44	80	RE9/S1RE9	Button S4	P80_S4
45	26	PGC2/RP36/RB4/S1PGC2/S1AN9/S1RP36/S1PWM5L/S1RB4	ICSP™ Prog/Debug PGC2	P26_PGC
46	55	RP56/ASDA1/SCK2/RC8/S1RP56/S1ASDA1/S1SCK1/S1RC8	mikroBUS™ B SPI SCK	P55_SCKB
47	54	RP57/ASCL1/SDI2/RC9/S1RP57/S1ASCL1/S1SDI1/S1RC9	mikroBUS B SPI MISO	P54_MISOB
48	96	PCI20/RD9/S1PCI20/S1RD9	General Purpose I/O	P96_VBUSON
49	53	SDO2/PCI19/RD8/S1SDO1/S1PCI19/S1RD8	mikroBUS B SPI MOSI	P53_MOSIB
11, 26, 32, 50, 70	65	VSS + AVSS	VSS	VSS
12, 25, 31, 51, 71	62	VDD + AVDD	VDD	VDD_PIM
52	89	RP71/RD7/S1RP71/S1PWM8H/S1RD7	General Purpose I/O	P89_USBDN
53	11	RP70/RD6/S1RP70/S1PWM6H/S1RD6	mikroBUS A SPI MISO	P11_MISOA
54	90	RP69/RD5/S1RP69/S1PWM6L/S1RD5	General Purpose I/O	P90_USBDP
55[1]	NC	S1PGC3/RPIN38/RPO6/S1RPIN38/S1RPO6/SCL2/RB6/ S1RB6	—	—
56[1]	NC	S1PGD3/RPIN37/RPO5/S1RPIN37/S1RPO5/SDA2/RB5/ S1RB5	—	—
57	81	RE10/S1RE10	LCD E	P81_LCDE
58	23	TDO/AN9/RP39/RB7/$\overline{\text{S1MCLR1}}$/S1AN6/S1RP39/S1PWM5H/ S1RB7	mikroBUS B Chip Select	P23_CSB
59	44	RE11/S1RE11	LCD Register Select	P44_LCDRS
60	57	PGD1/AN10/RP40/SCL1/RB8/S1PGD1/S1AN7/S1RP40/ S1SCL1/S1RB8	Shared I^2C SCL	P57_SCL
61	56	PGC1/AN11/RP41/SDA1/RB9/S1PGC1/S1RP41/S1SDA1/ S1RB9	Shared I^2C SDA	P56_SDA
62	100	ASCL2/RE12/ S1RE12	LCD D4	P100_LCDD4
63	78	RP52/RC4/S1RP52/S1PWM2H/S1RC4	mikroBUS B PWM	P78_PWMB
64	3	ASDA2/RE13/S1RE13	LCD D5	P3_LCDD5
65	69	RP53/RC5/S1RP53/S1PWM2L/S1RC5	General Purpose I/O	P69
66	49	RP58/RC10/S1RP58/S1PWM1H/S1RC10	MCP2221A and mikroBUS B RX	P49_RXB
67	50	RP59/RC11/S1RP59/S1PWM1L/S1RC11	MCP2221A and mikroBUS B TX	P50_TXB
68	95	RP68/RD4/S1RP68/S1PWM3H/S1RD4	mikroBUS A Reset Pin	P95_RSTA
69	14	RP67/RD3/S1RP67/S1PWM3L/S1RD3	mikroBUS A Reset Pin	P14_CSA
11, 26, 32, 50, 70	65	VSS + AVSS	VSS	VSS
12, 25, 31, 51, 71	62	VDD + AVDD	VDD	VDD_PIM
72	67	RP66/RD2/S1RP66/S1PWM8L/S1RD2	mikroBUS A Interrupt	P67_INTA
73	51	RP65/RD1/S1RP65/S1PWM4H/S1RD1	mikroBUS A TX	P51_TXA
74	52	RP64/RD0/S1RP64/S1PWM4L/S1RD0	mikroBUS A RX	P52_RXA
75	39	TMS/RP42/PWM3H/RB10/S1RP42/S1RB10	General Purpose I/O	P39
76	40	TCK/RP43/PWM3L/RB11/S1RP43/S1RB11	General Purpose I/O	P40
77	4	RE14/S1RE14	LCD D6	P4_LCDD6
78	66	TDI/RP44/PWM2H/RB12/S1RP44/S1RB12	General Purpose I/O	P66
79	5	RE15/S1RE15	LCD D7	P5_LCDD7
80	18	RP45/PWM2L/RB13/S1RP45/S1RB13	mikroBUS B Interrupt	P18_INTB

Note 1: These pins are connected to "Dual Debug" header J2. They can optionally be connected to the Explorer 16/32 if R1, R2 and R3 are populated with jumper resistors.

Schematic Revision 1.0