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User's Guide

SNVA136A–June 2006–Revised April 2013

AN-1420 LM3208 Evaluation Board

1 Introduction

The LM3208 evaluation board is a working demonstration of a step down DC-DC converter. This document contains information about the evaluation board and board layout considerations. For further information on buck converter topology, device electrical characteristics, and component selection, see the device-specific data sheet.

2 General Description

The LM3208 is a DC-DC converter optimized for powering RF power amplifiers (PAs) from a single Lithium-Ion cell, however they may be used in many other applications. It steps down an input voltage from 2.7V to 5.5V to a variable output voltage from 0.8V(typ.) to 3.6V(typ.). Output voltage is set using a V_{CON} analog input for controlling power levels and efficiency of the RF PA.

The LM3208 offers superior performance for mobile phones and similar RF PA applications. Fixed-frequency PWM operation minimizes RF interference. Shutdown function turns the device off and reduces battery consumption to 0.01 µA (typ.).

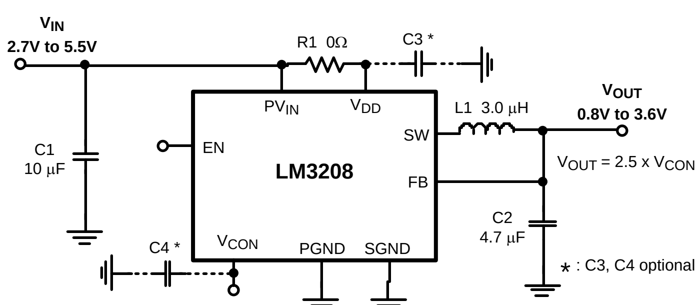
The LM3208 is available in a 8-pin lead free DSBGA package. A high switching frequency (2 MHz) allows use of tiny surface-mount components. Only three small external surface-mount components, an inductor and two ceramic capacitors are required.

3 Operating Conditions

The board will operate under the following conditions:

- V_{IN} range: 2.7V ≤ V_{IN} ≤ 5.5V
- V_{CON} range: 0.32V ≤ V_{CON} ≤ 1.44V
- V_{OUT} equation: V_{OUT} = 2.5 x V_{CON}
- I_{OUT} range: 0 mA≤ I_{OUT} ≤ 650 mA

4 Typical Application



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5 Evaluation Board Layout

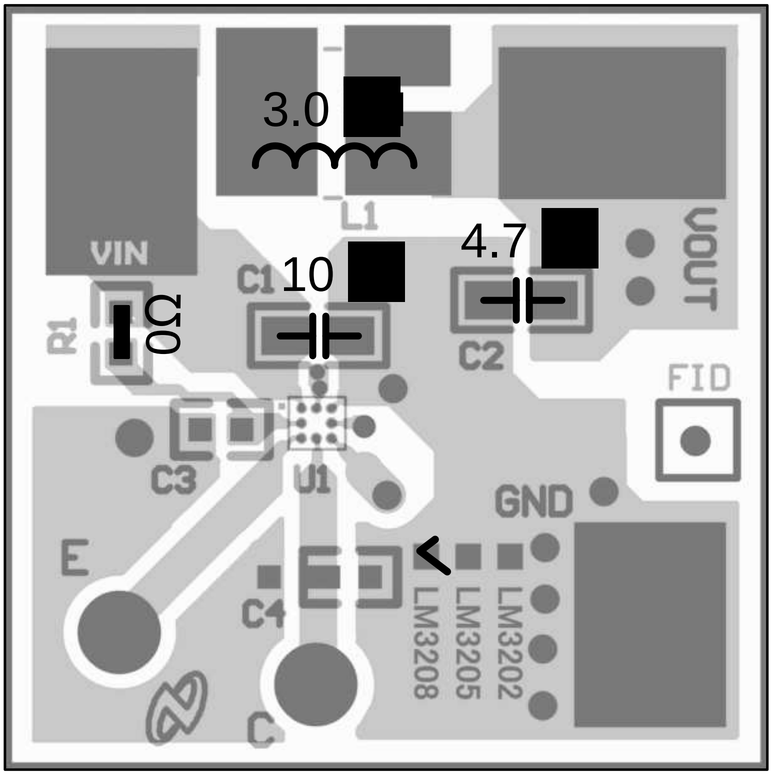

Figure 1. Top Layer

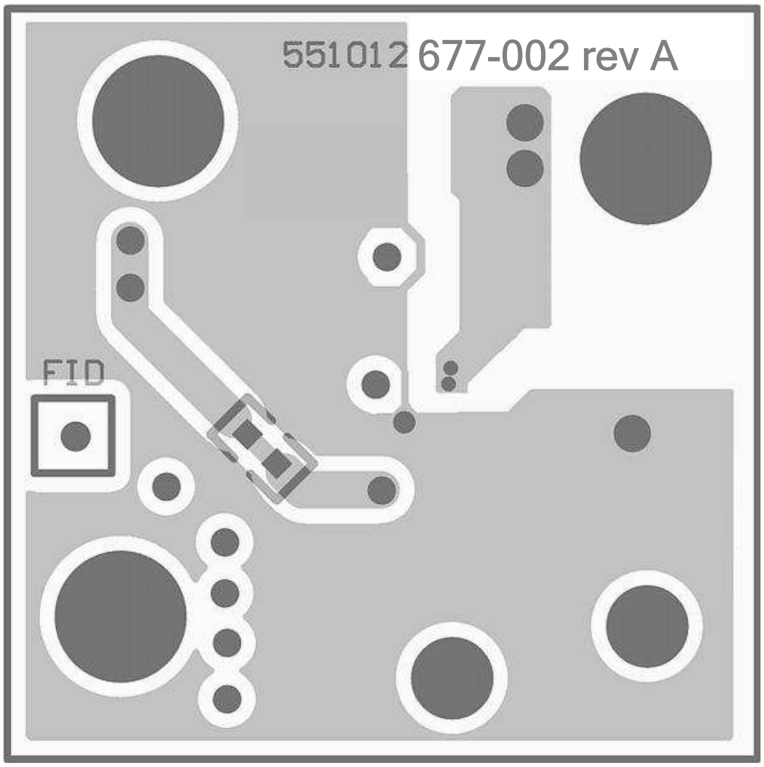

Figure 2. Bottom Layer

6 Connection Diagram and Package Mark Information

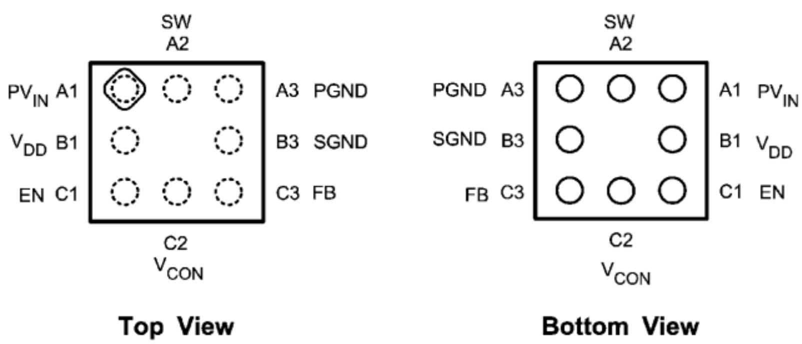

Figure 3. 8-Bump Thin DSBGA Package, Large Bump

Table 1. Pin Descriptions

Pin No	Name	Description
A1	PV_{IN}	Power Supply Voltage Input to the internal PFET switch.
B1	V_{DD}	Analog Supply Input.
C1	EN	Enable Input. Set this digital input high for normal operation. For shutdown, set low.
C2	V_{CON}	Voltage Control Analog input. V_{CON} controls V_{OUT} in PWM mode.
C3	FB	Feedback Analog Input. Connect to the output at the output filter capacitor.
B3	SGND	Analog and Control Ground
A3	PGND	Power Ground
A2	SW	Switch node connection to the internal PFET switch and NFET synchronous rectifier. Connect to an inductor with a saturation current rating that exceeds the maximum Switch Peak Current Limit specification of the LM3208.

7 Bill of Materials (BOM) for Common Configurations

	Manufacture	Manufacture No	Description
C1 (input C)	TDK	C2012X5R0J106M	10 µF, 6.3V, 20%, 0805 (2012)
C2 (output C)	TDK	C1608X5R0J475M	4.7 µF, 6.3V, 20%, 0603 (1608)
C3 (optional, input C)			0.1 µF, 25V , 0402 (1005) (1)
C4 (optional, filter for V_{CON})			10 - 100 pF, 25V, 0402 (1005) (1)
L1 (inductor)	FDK	MIPW3226D3R0M	3.0 µH, Idc = 1000mA, Rdc = 0.12Ω, 3.2×2.6×1.0 mm
R1 (jumper PV_{IN} to V_{DD})	Vishay	CRCW04020R00F	0Ω, 0402 (1005)
V_{IN} banana jack - red	Johnson Components	108-0902-001	Connector, insulated banana jack (red)
V_{out} banana jack - yellow	Johnson Components	108-0907-001	Connector, insulated banana jack (yellow)
GND banana jack - black	Johnson Components	108-0903-001	Connector, insulated banana jack (black)

(1) C3 and C4 are recommended for a better noise performance.

8 Board Layout Considerations

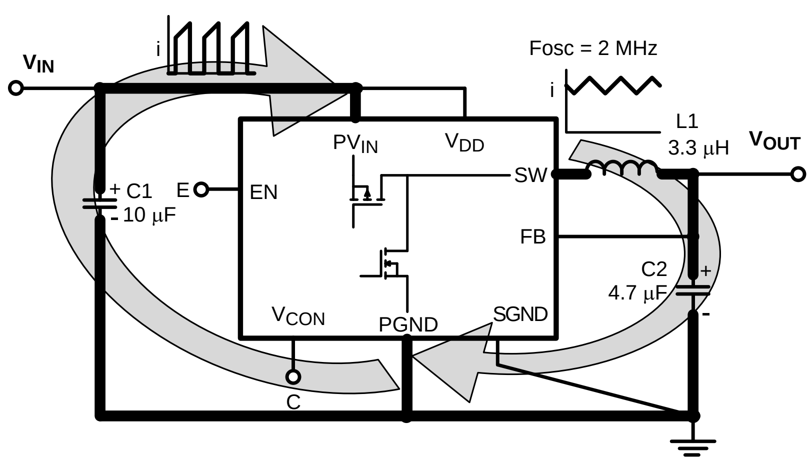

Figure 4. Current Loop

The LM3208 converts higher input voltage to lower output voltage with high efficiency. This is achieved with an inductor-based switching topology. During the first half of the switching cycle, the internal PMOS switch turns on, the input voltage is applied to the inductor, and the current flows from PV_{IN} line to the output capacitor (C2) and the load through the inductor. During the second half cycle, the PMOS turns off and the internal NMOS turns on. The inductor current continues to flow via the inductor from the device PGND line to the output capacitor (C2) and the load .

Referring to Figure 4, a pulse current flows in the left hand side loop, and a ripple current flows in the right hand side loop. Board layout and circuit pattern design of these two loops are the key factors for reducing noise radiation and stable operation. In other lines, such as from battery to C1 and C2 to the load, the current is mostly DC current. Theresore, it is not necessary to take so much care. Only pattern width (current capability) and DCR drop considerations are needed.

8.1 Board Layout Flow

1. Minimize C1, PV_{IN}, and PGND loop. These traces should be as wide and short as possible. This is the highest priority.
2. Minimize L1, C2, SW and PGND loop. These traces also should be wide and short. This is the second priority.
3. The above layout patterns should be placed on the component side of the PCB to minimize parasitic inductance and resistance due to via-holes. It may be a good idea that the SW to L1 path is routed between C1(+) and C1(-) land patterns. If vias are used in these large current paths, multiple via-holes should be used if possible.
4. Connect C1(-), C2(-) and PGND with wide GND pattern. This pattern should be short, so C1(-), C2(-), and PGND should be as close as possible. Then connect to a PCB common GND pattern with as many via-holes as possible.
5. SGND should not connect directly to PGND. Connecting these pins under the device should be avoided. (If possible, connect SGND to the common port of C1(-), C2(-) and PGND.)
6. V_{DD} should not be connected directly to PV_{IN}. Connecting these pins under the device should be avoided. It is good idea to connect V_{DD} to C1(+) to avoid switching noise injection to the V_{DD} line.
7. The FB line should be protected from noise. It is a good idea to use an inner GND layer (if available) as a shield.

NOTE: The evaluation board shown in Figure 1 and Figure 2 for the LM3208 was designed with these considerations, and it shows good performance. However some aspects have not been optimized because of limitations due to evaluation-specific requirements. The board can be used as a reference, but it is not the ideal. For more information, contact a TI representative.

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