UNITRODE

DV2003S2

Fast Charge Development System

Control of On-Board N-FET Switch-Mode Regulator

Features

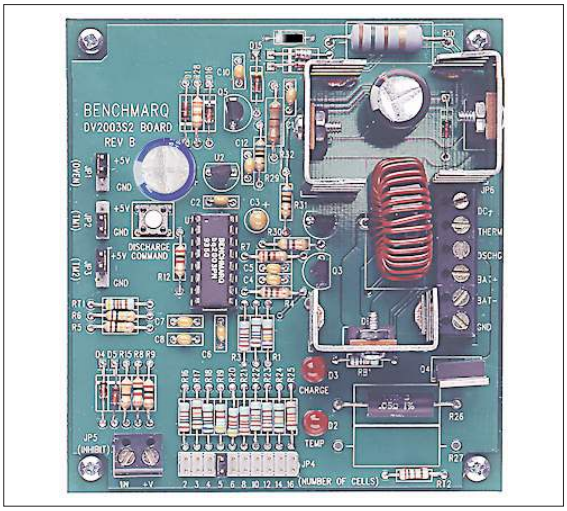
- bq2003 fast charge control evaluation and bq2003 fast-charge control evaluation and development
- Charge current sourced from an on-board switch-mode regulator (up to 6.0 A)
- Fast charge of 2 to 16 NiCd or NiMH cells
- Fast-charge termination by delta temperature/delta time (ΔT/Δt), negative delta voltage (-ΔV), maximum temperature, maximum time, and maximum voltage
- -ΔV enable, hold-off, top-off, maximum time, and number of cells are jumper-configurable
- Charging status displayed on charge and temperature LEDs
- Discharge-before-charge control with push-button switch
- Inhibit fast charge by external logic-level input

General Description

The DV2003S2 Development System provides a development environment for the bq2003 Fast-Charge IC. The DV2003S2 incorporates a bq2003 and an N-FET buck-type switch-mode regulator to provide fast charge control for 2 to 16 NiCd or NiMH cells. The primary difference between the DV2003S2 and the DV2003S1 is in the switching FET Q1. The DV2003S1 uses a P-FET for battery charge currents of 3.0A or less, whereas the DV2003S2 uses an n-FET to support charge currents up to 6.0A.

Review the bq2003 data sheet and the application note, "Using the bq2003 to Control Fast Charge," before using the DV2003S2 board. Also review the application note, "Step-Down Switching Current Regulation Using the bq2003," for information concerning trade-offs between using P-FET and N-FET transistors for Q1.

The fast charge is terminated by any of the following: ΔT/Δt, -ΔV, maximum temperature, maximum time, maximum voltage, or an external inhibit command. Jumper settings select the -ΔV enabled state, and the hold-off, top-off, and maximum time limits.



The user provides a power supply and batteries. The user configures the DV2003S2 for the number of cells, -ΔV charge termination, and maximum charge time (with or without top-off), and commands the discharge-before-charge option with the push-button switch S1.

Connection Descriptions

JP6

DC+	DC input from charger supply
THERM	Thermistor connection
DSCHG	Low side of discharge load
BAT+	Positive battery terminal and high side of discharge load
BAT–	Negative battery terminal and thermistor connection
GND	Ground from charger supply

JP5

+V	Voltage source for inhibit input
IN	Inhibit input to prevent bq2003 activity

JP1 DVEN Negative voltage termination enable

JP2 TM1 TM1 setting

JP3 TM2 TM2 setting

JP4 NOC Select number of cells

Fixed Configuration

The DV2003S2 board has the following fixed characteristics :

V_{CC} (4.75–5.25V) is regulated on-board from the supply at connector JP6 DC+.

LEDs indicate charge status and temperature fault status.

Pin CCMD is grounded, providing charge initiation on the later application of the battery or DC+, which provides V_{CC} to the bq2003.

Pin DCMD is pulled to ground through R12. A toggle of switch S1 momentarily pulls DCMD high and initiates a discharge-before-charge. The bq2003 output activates FET Q4, allowing current to flow through an external current-limiting load between BAT+ and DSCHG on connector JP6.

Trickle current is limited by a 150Ω/2W resistor R10 between DC+ and BAT+ (maximum potential across R10 = 17.3V). Note that too large a voltage between DC+ and BAT+ may exceed the wattage rating of resistor R10.

As shipped from Benchmarq, the DV2003S1 buck-type switch-mode regulator is configured to a charging current of 2.35A. This current level is controlled by the value of sense resistor R26 by the relationship:

$$I_{CHG} = \frac{0.235V}{R26}$$

The value of R26 at shipment is 0.100Ω. This resistor can be changed depending on the application.

The suggested maximum I_{CHG} for the DV2003S2 board is 3A. A location for a second sense resistor (R27) is provided on the DV2003S2 board. R27 is electrically in parallel with R26, which assists in user modification of I_{CHG}, if needed.

Charge current can be halted at any time via external stimulus. Connector JP5 provides a +5V DC source (+V) and an inhibit input (IN) node for this function. To inhibit charge current, the JP5 inhibit input (IN) is driven by +5V DC. To re-initiate charge, remove the voltage source from the inhibit input.

The maximum cell voltage (MCV) setting is 1.8V.

With the provided NTC thermistor connected between THERM and BAT–, values are: LTF = 10°C, HTF = 45°C, and TCO = 50°C. The $\Delta T/\Delta t$ settings at 30°C ($T_{\Delta T}$) are: minimum = 0.82°C/minute, typical = 1.10°C/minute.

The thermistor is identified by the serial number suffix as follows:

Identifier	Thermistor
K1	Keystone RL0703-5744-103-S1
(blank)	Philips 2322-640-63103
F1	Fenwal Type 16, 197-103LA6-A01
O1	Ozhumi 150-108-00(4)
S1	Semetic 103AT-2

Jumper-Selectable Configuration

The DV2003S1 must be configured as described below.

DVEN (JP1): Enables/disables -ΔV termination (see bq2003 data sheet).

Jumper Setting	Pin State
[1 2] 3	Enabled (high)
1 [2 3]	Disabled (low)

TM1 and TM2 (JP2 and JP3): Select fast charge safety time/hold-off/top-off (see bq2003 data sheet).

Jumper Setting	Pin State
[1 2] 3	High
1 [2 3]	Low
1 2 3	Float

Number of Cells (JP4): A resistor-divider network is provided to select 2 to 16 cells (the resulting resistor value equals N – 1 cells). RB1 is a 200KΩ resistor, and RB2 (R16–R25) is jumper-selected.

Temperature Disable: Connecting a 10KΩ resistor between THERM and BAT– disables temperature control.

Closed Jumper	Number of Cells
R25	16
R24	14
R23	12
R22	10
R21	8
R20	6
R19	5
R18	4
R17	3
R16	2

Setup Procedure

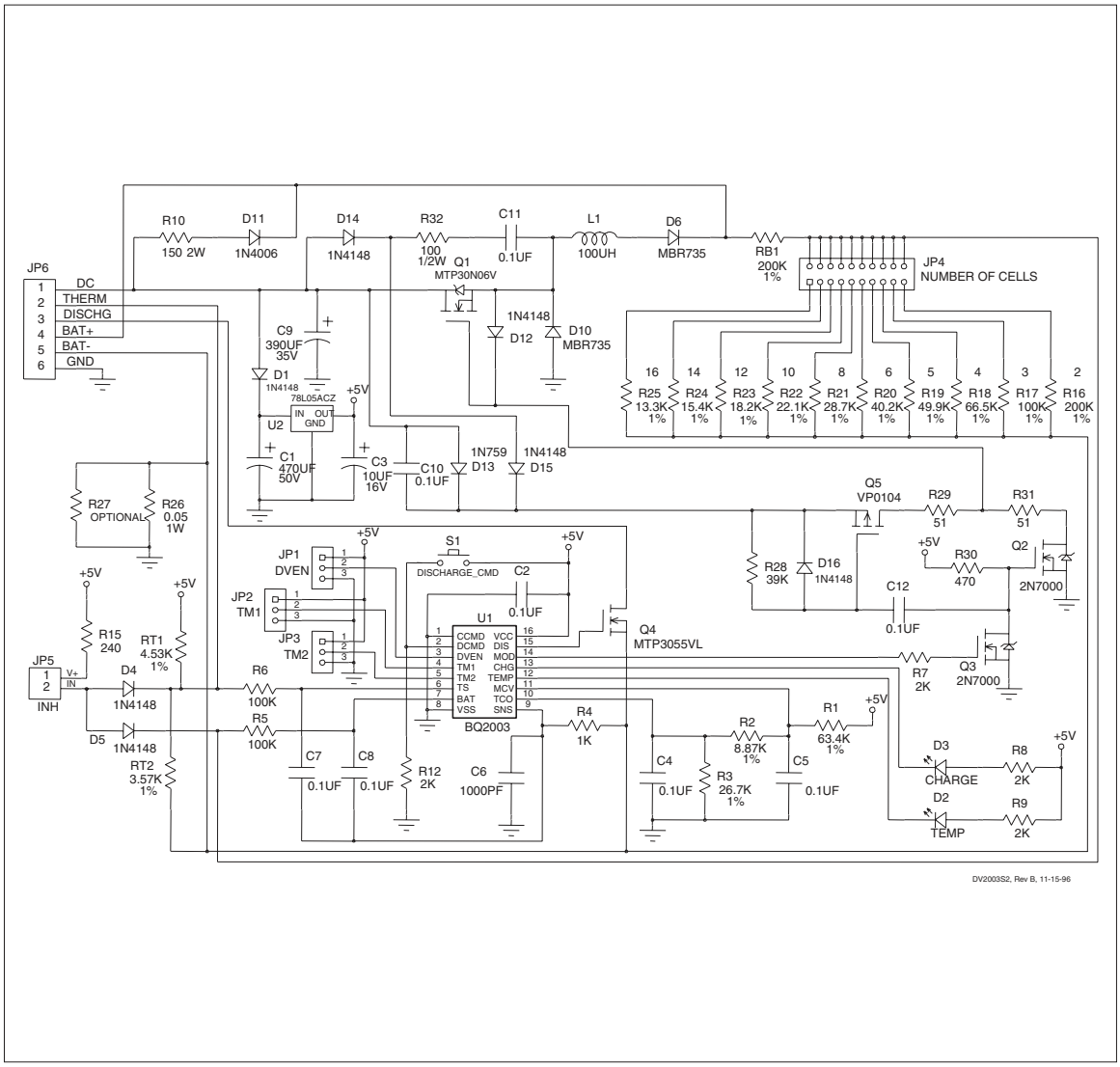
1. Configure DVEN, TM1, TM2, and number-of-cells (NOC) jumpers.
2. Connect the provided thermistor or a 10KΩ resistor between THERM and BAT–.

   Note: RT1 and RT2 match the thermistor provided and must be changed if a different thermistor type is used (see Appendix A in the application note, "Using the bq2003 to Control Fast Charge").
3. If using the discharge-before-charge option, connect a current-limiting discharge load between BAT+ and DSCHG.
4. If using the INHIBIT function, connect a switch across JP5 (IN to +V) or connect IN to the controlling signal source (3–5V).
5. Attach the battery pack to BAT+ and BAT–. For temperature control, the thermistor must contact the cells.
6. Attach DC current source to DC+ (+) and GND (–) connections in JP6.

Recommended DC Operating Conditions

Symbol	Description	Minimum	Typical	Maximum	Unit	Notes
I_{DC+}	Maximum input current	-	-	6.0	A	
V_{DC+}	Maximum input voltage	2.0 + V_{BAT+} or 8.0	-	30	V	
V_{BAT+}	BAT+ input voltage	-	-	30	V	
V_{THERM}	THERM input voltage	0	-	5	V	
V_{IN}	Inhibit input signal	0	-	5	V	
I_{DSCHG}	Discharge load current	-	-	2	A	

DV2003S2 Board Schematic



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