CBTD3306

Dual bus switch with level shifting

Rev. 8 — 1 May 2012 Product data sheet

1. General description

The CBTD3306 dual FET bus switch features independent line switches. Each switch is disabled when the associated output enable ($n\overline{OE}$) input is HIGH.

The CBTD3306 is characterized for operation from −40 °C to +85 °C.

2. Features and benefits

- Designed to be used in 5 V to 3.3 V level shifting applications with internal diode
- 5 Ω switch connection between two ports
- TTL-compatible input levels
- Multiple package options
- Latch-up protection exceeds 100 mA per JESD78B
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - CDM JESD22-C101E exceeds 1000 V

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
CBTD3306D	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
CBTD3306PW	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 4.4 mm	SOT530-1
CBTD3306GT	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	SOT833-1
CBTD3306GM	XQFN8	plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.6 × 1.6 × 0.5 mm	SOT902-2

4. Marking

Table 2. Marking codes

Type number	Marking code
CBTD3306D	CBD3306
CBTD3306PW	D306
CBTD3306GT	W06
CBTD3306GM	W06

5. Functional diagram

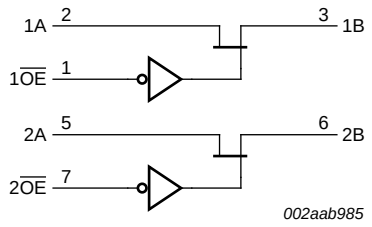


Fig 1. Logic diagram

6. Pinning information

6.1 Pinning

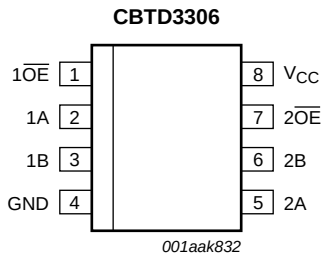


Fig 2. Pin configuration for SO8 (SOT96-1)

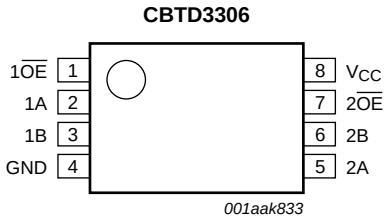


Fig 3. Pin configuration for TSSOP8 (SOT530-1)

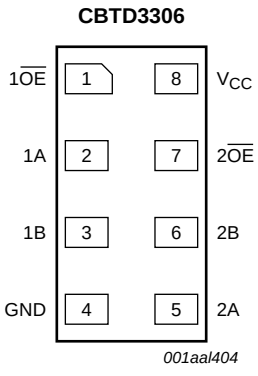


Fig 4. Pin configuration SOT833-1 (XSON8)

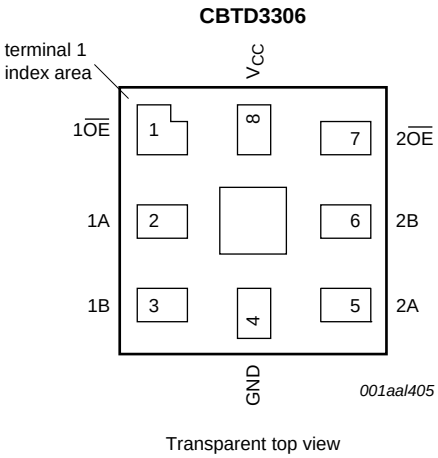


Fig 5. Pin configuration SOT902-2 (XQFN8)

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
$1\overline{OE}$, $2\overline{OE}$	1, 7	output enable input
1A, 2A	2, 5	data input/output (A port)
1B, 2B	3, 6	data input/output (B port)
GND	4	ground (0 V)
V_{CC}	8	positive supply voltage

7. Functional description

Table 4. Function selection[1]

Input	Input/output
$n\overline{OE}$	nA, nB
L	nA = nB
H	Z

[1] H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			−0.5	+7.0	V
V_I	input voltage		[2]	−0.5	+7.0	V
I_{SW}	switch current			-	128	mA
I_{IK}	input clamping current	$V_{I/O}$ = 0 V		−50	-	mA
T_{stg}	storage temperature			−65	+150	°C

[1] Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Section 9. is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

9. Recommended operating conditions

Table 6. Operating conditions

All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
T_{amb}	ambient temperature	operating in free air	−40	-	+85	°C

10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

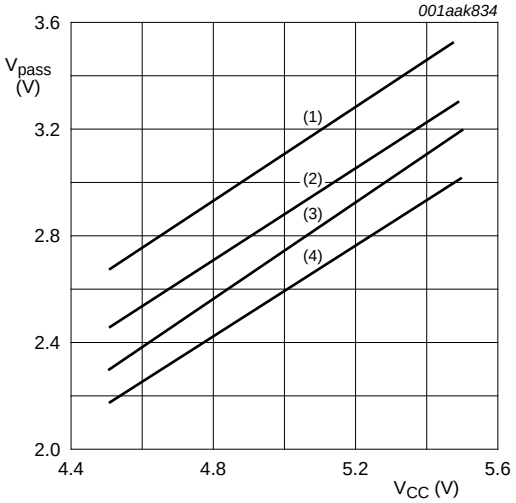
Symbol	Parameter	Conditions		T_{amb} = –40 °C to +85 °C			Unit
				Min	Typ[1]	Max	
V_{IK}	input clamping voltage	V_{CC} = 4.5 V; I_I = –18 mA		-	-	–1.2	V
I_I	input leakage current	V_{CC} = 5.5 V; V_I = GND or 5.5 V		-	-	±1	μA
I_{CC}	supply current	V_{CC} = 5.5 V; I_{SW} = 0 mA; V_I = V_{CC} or GND		-	-	1.5	mA
V_{pass}	pass voltage	see Figure 6 to Figure 10		-	-	-	V
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 5.5 V; one input at 3.4 V, other inputs at V_{CC} or GND	[2]	-	-	2.5	mA
C_I	input capacitance	control pin; V_I = 3 V or 0 V		-	3.2	-	pF
$C_{io(off)}$	off-state input/output capacitance	port off; V_I = 3 V or 0 V; $n\overline{OE}$ = V_{CC}		-	6.5	-	pF
R_{ON}	ON resistance	V_{CC} = 4.5 V; V_I = 0 V; I_I = 64 mA	[3]	-	3.6	5	Ω
		V_{CC} = 4.5 V; V_I = 0 V; I_I = 30 mA	[3]	-	3.6	5	Ω
		V_{CC} = 4.5 V; V_I = 2.4 V; I_I = 15 mA	[3]	-	17	35	Ω

[1] All typical values are at V_{CC} = 5 V, T_{amb} = 25 °C.

[2] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

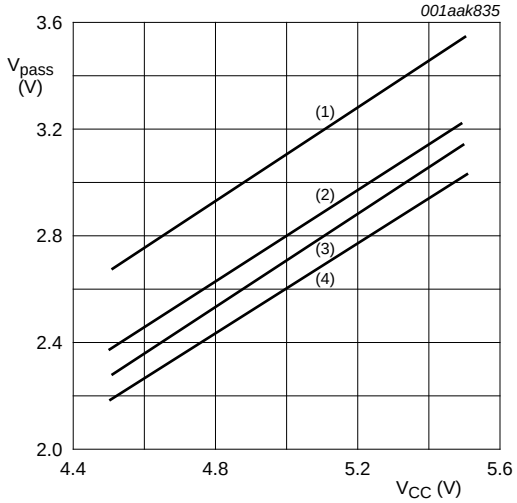
[3] Measured by the voltage drop between the nA and the nB terminals at the indicated current through the switch. ON resistance is determined by the lowest voltage of the two (nA or nB) terminals.

10.1 Typical pass voltage graphs



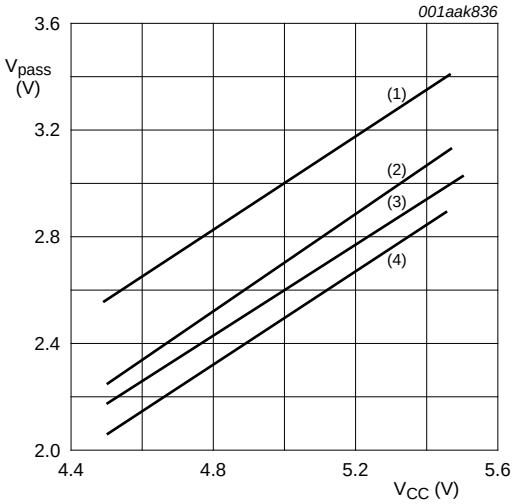
(1) I_{SW} = 100 µA
(2) I_{SW} = 6 mA
(3) I_{SW} =12 mA
(4) I_{SW} = 24 mA

Fig 6. Pass voltage versus supply voltage; T_{amb} = 85 °C (typical)



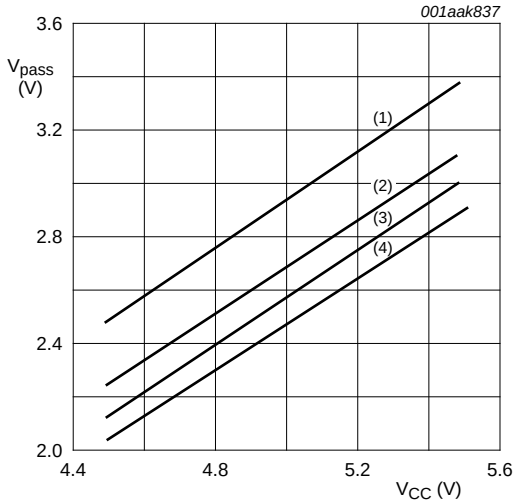
(1) I_{SW} = 100 µA
(2) I_{SW} = 6 mA
(3) I_{SW} =12 mA
(4) I_{SW} = 24 mA

Fig 7. Pass voltage versus supply voltage; T_{amb} = 70 °C (typical)



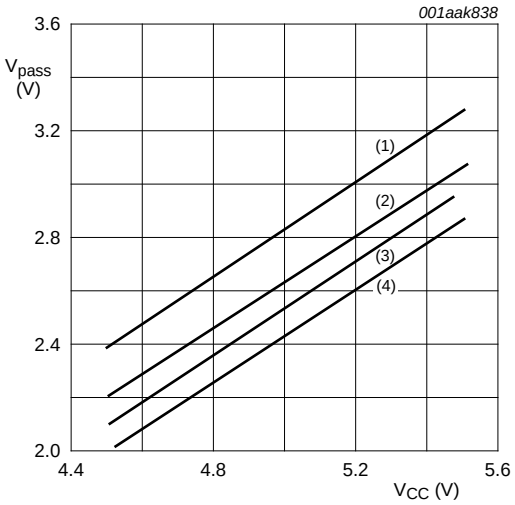
(1) I_{SW} = 100 µA
(2) I_{SW} = 6 mA
(3) I_{SW} =12 mA
(4) I_{SW} = 24 mA

Fig 8. Pass voltage versus supply voltage; T_{amb} = 25 °C (typical)



(1) I_{SW} = 100 µA
(2) I_{SW} = 6 mA
(3) I_{SW} =12 mA
(4) I_{SW} = 24 mA

Fig 9. Pass voltage versus supply voltage; T_{amb} = 0 °C (typical)



(1) I_{SW} = 100 μA

(2) I_{SW} = 6 mA

(3) I_{SW} =12 mA

(4) I_{SW} = 24 mA

Fig 10. Pass voltage versus supply voltage; T_{amb} = –40 °C (typical)

11. Dynamic characteristics

Table 8. Dynamic characteristics

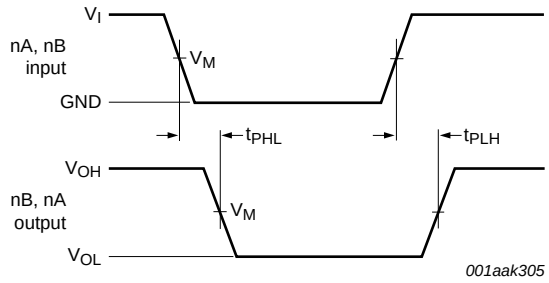
Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 13.

Symbol	Parameter	Conditions		T_{amb} = –40 °C to +85 °C			Unit
				Min	Typ	Max	
t_{pd}	propagation delay	nA, nB to nB, nA; see Figure 11	[1][2]	-	-	0.25	ns
		V_{CC} = 5.0 V ± 0.5 V					
t_{en}	enable time	$\overline{nOE}$ to nA or nB; see Figure 12	[2]	1.0	-	5.4	ns
		V_{CC} = 5.0 V ± 0.5 V					
t_{dis}	disable time	$\overline{nOE}$ to nA or nB; see Figure 12	[2]	1.0	-	4.9	ns
		V_{CC} = 5.0 V ± 0.5 V					

[1] The propagation delay is the calculated RC time constant of the typical ON resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

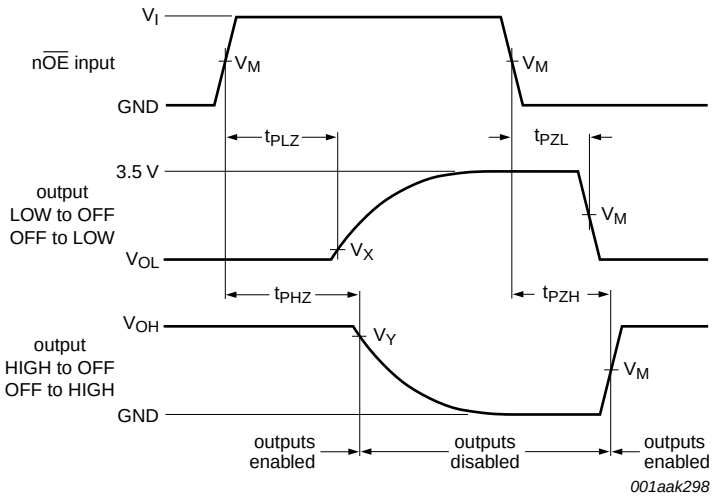
12. Waveforms



Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 11. The data input (nA, nB) to output (nB, nA) propagation delay times



Measurement points are given in Table 9.

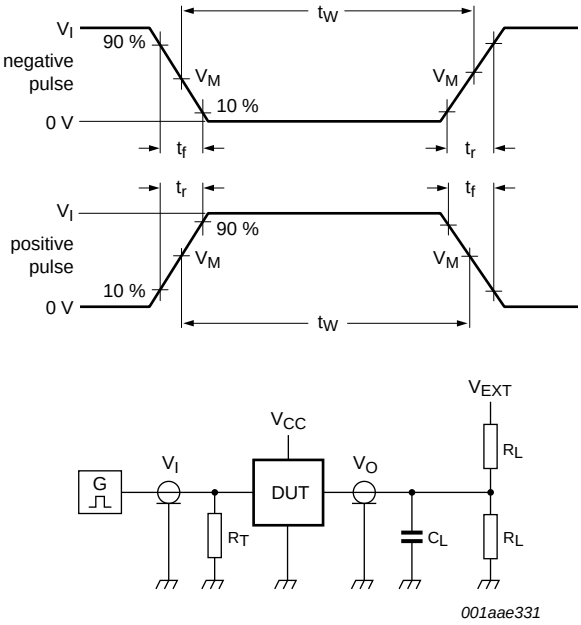
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 12. Enable and disable times

Table 9. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
V_{CC} = 5.0 V ± 0.5 V	GND to 3.0 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} − 0.3 V

13. Test information



Test data is given in Table 10.

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω.

The outputs are measured one at a time with one transition per measurement.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

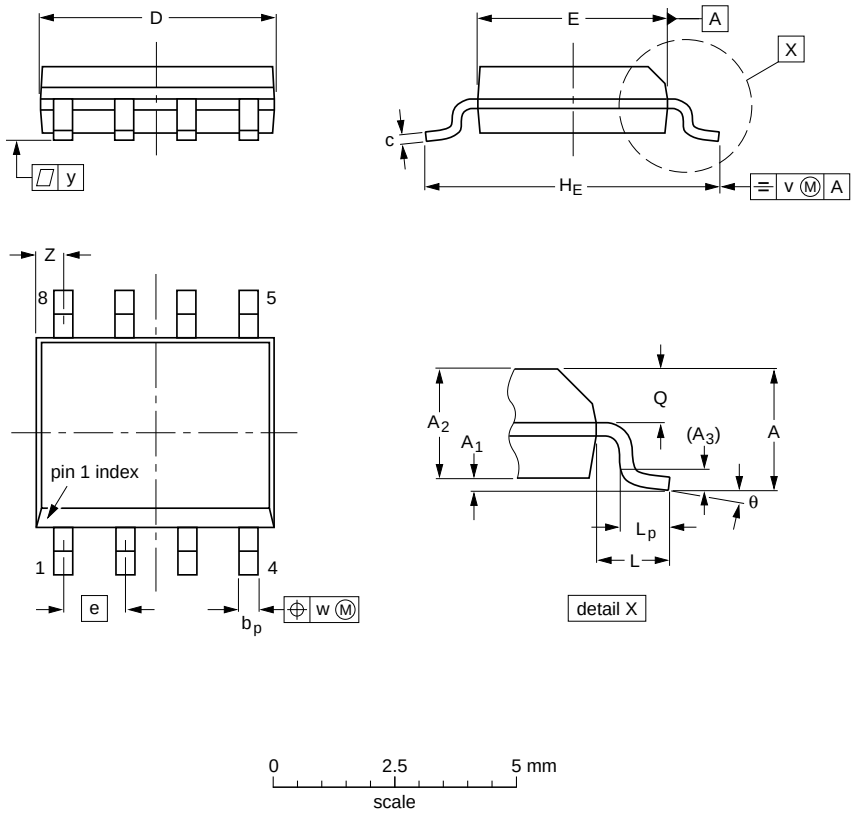
Fig 13. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
V_{CC} = 5.0 V ± 0.5 V	GND to 3.0 V	≤ 2.5 ns	50 pF	500 Ω	open	7.0 V	open

14. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

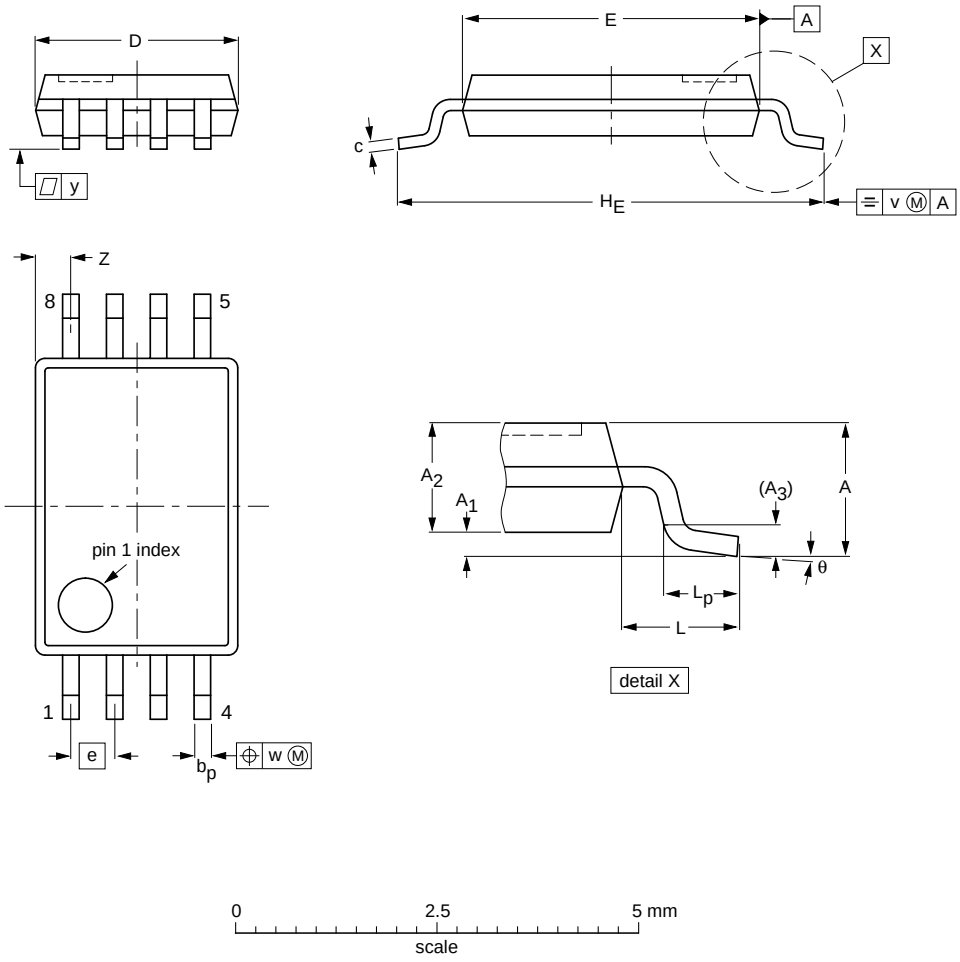
Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 14. Package outline SOT96-1 (SO8)

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 4.4 mm **SOT530-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.85	0.25	0.30 0.19	0.20 0.13	3.1 2.9	4.5 4.3	0.65	6.5 6.3	0.94	0.7 0.5	0.1	0.1	0.1	0.70 0.35	8° 0°

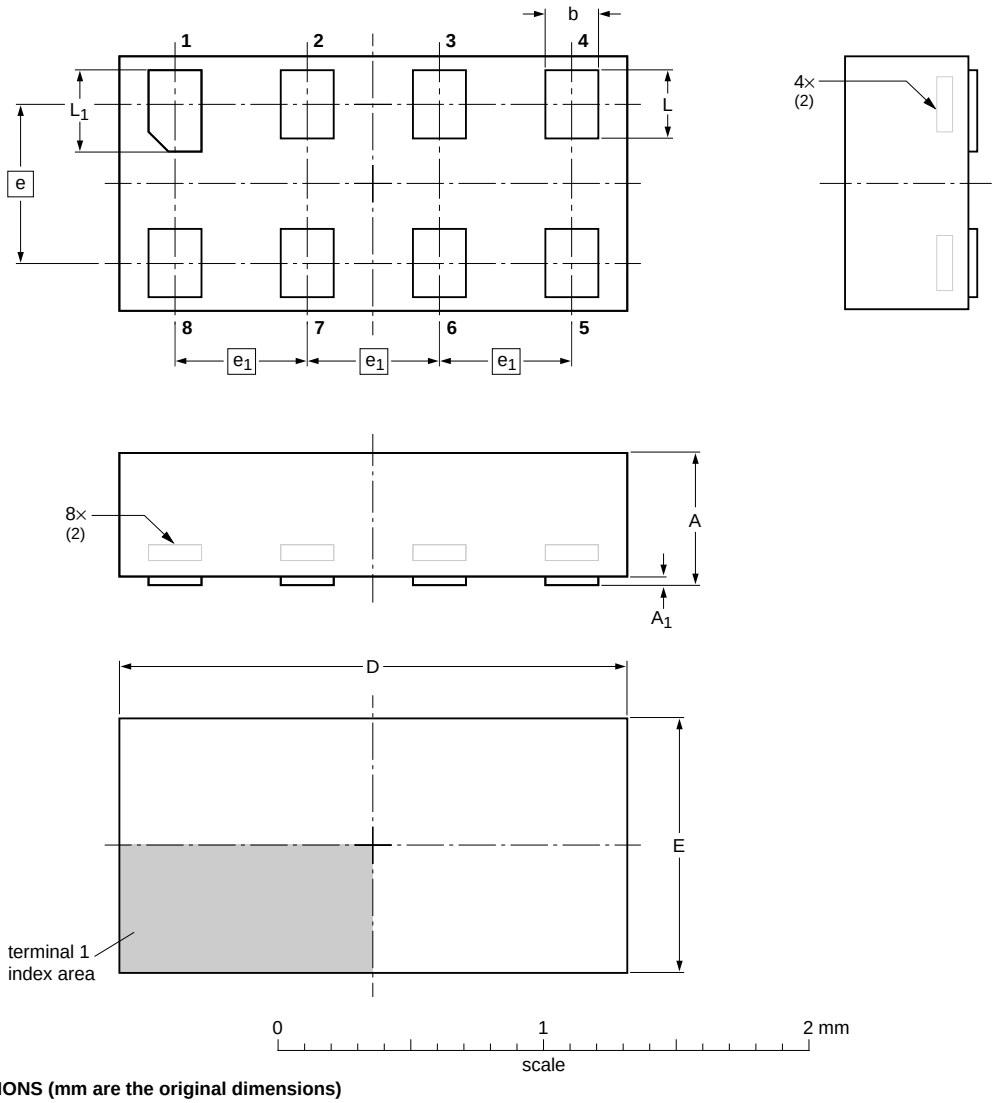
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT530-1		MO-153				~~00-02-24~~ 03-02-18

Fig 15. Package outline SOT530-1 (TSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm **SOT833-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max	A1 max	b	D	E	e	e1	L	L1
mm	0.5	0.04	0.25 0.17	2.0 1.9	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

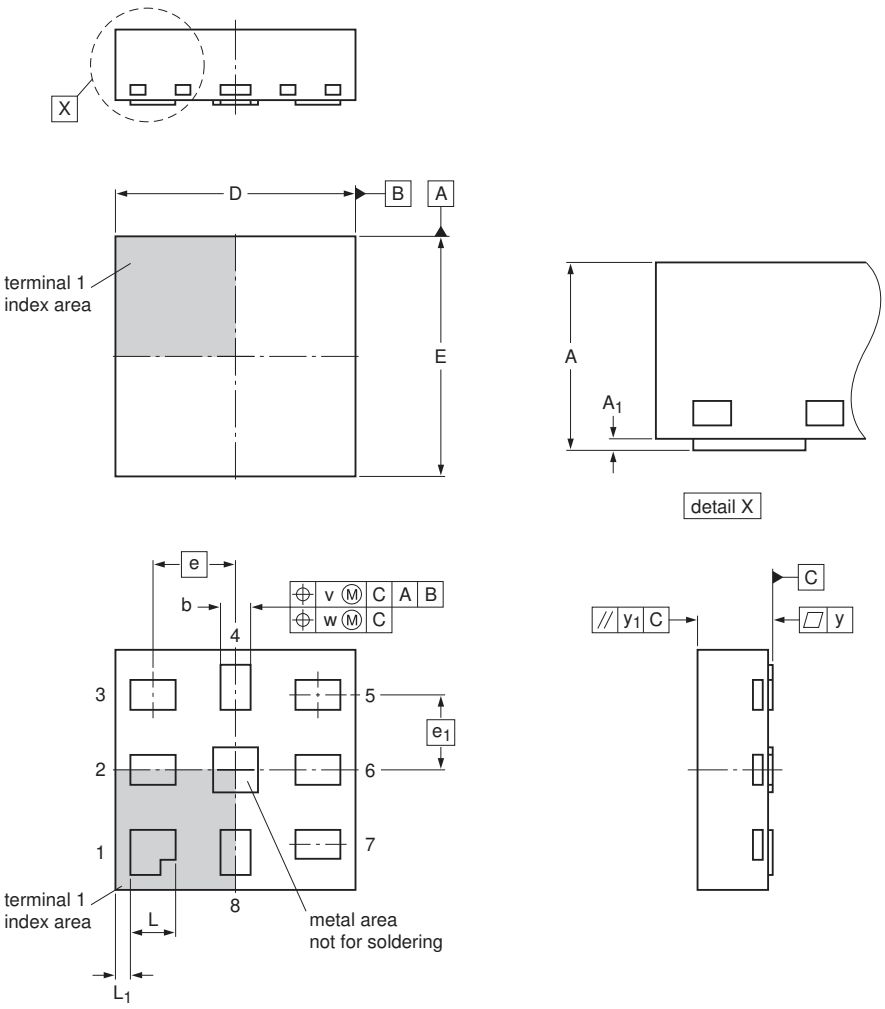
Notes

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT833-1	- - -	MO-252	- - -			~~07-11-14~~ 07-12-07

Fig 16. Package outline SOT833-1 (XSON8)

XQFN8: plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.6 x 1.6 x 0.5 mm **SOT902-2**



Dimensions

Unit(1)		A	A_1	b	D	E	e	e_1	L	L_1	v	w	y	y_1
mm	max	0.5	0.05	0.25	1.65	1.65	0.55	0.5	0.35	0.15	0.1	0.05	0.05	0.05
	nom			0.20	1.60	1.60			0.30	0.10				
	min		0.00	0.15	1.55	1.55			0.25	0.05				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot902-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT902-2	- - -	MO-255	- - -			~~10-11-02~~ 11-03-31

Fig 17. Package outline SOT902-2 (XQFN8)

15. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
FET	Field Effect Transistor
HBM	Human Body Model
PRR	Pulse Rate Repetition
TTL	Transistor-Transistor Logic

16. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBTD3306 v.8	20120501	Product data sheet	-	CBTD3306 v.7
Modifications:	• For type number CBTD3306GM the SOT code has changed to SOT902-2.			
CBTD3306 v.7	20120103	Product data sheet	-	CBTD3306 v.6
Modifications:	• Marking code for type number CBTD3306D changed.			
CBTD3306 v.6	20111121	Product data sheet	-	CBTD3306 v.5
Modifications:	• Legal pages updated.			
CBTD3306 v.5	20110428	Product data sheet	-	CBTD3306 v.4
CBTD3306 v.4	20100325	Product data sheet	-	CBTD3306 v.3
CBTD3306 v.3	20100223	Product data sheet	-	CBTD3306 v.2
CBTD3306 v.2	20091015	Product data sheet	-	CBTD3306 v.1
CBTD3306 v.1	20011108	Product data	-	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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18. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

19. Contents

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