ACS781xLR

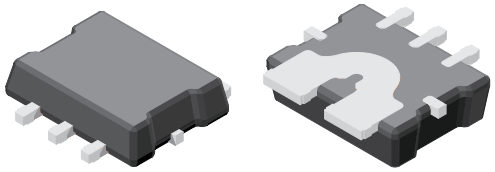
High-Precision Linear Hall-Effect-Based Current Sensor IC with 200 µΩ Current Conductor

FEATURES AND BENEFITS

- Core-less, micro-sized, 100 A continuous current package
- Ultra-low power loss: 200 µΩ internal conductor resistance
- Immunity to common-mode field interference
- Greatly improved total output error through digitally programmed and compensated gain and offset over the full operating temperature range
- Industry-leading noise performance through proprietary amplifier and filter design techniques
- Integrated shield greatly reduces capacitive coupling from current conductor to die due to high dV/dt signals, and prevents offset drift in high-side, high-voltage applications
- Monolithic Hall IC for high reliability
- 3 to 3.6 V, single supply operation
- 120 kHz typical bandwidth
- 3.6 µs output rise time in response to step input current
- Output voltage proportional to AC or DC currents
- Factory-trimmed for accuracy
- Extremely stable quiescent output voltage
- AEC-Q100 automotive qualification

PACKAGE:

7-pin PSOF package (suffix LR)



Not to scale

DESCRIPTION

The Allegro ACS781xLR is a fully integrated current sensor linear IC in a new core-less package designed to sense AC and DC currents up to 100 A. This automotive-grade, low-profile (1.5 mm thick) sensor IC package has a very small footprint. The Hall sensor technology also incorporates common-mode field rejection to optimize performance in the presence of interfering magnetic fields generated by nearby current carrying conductors.

The device consists of a precision, low-offset linear Hall circuit with a copper conduction path located near the die. Applied current flowing through this copper conduction path generates a magnetic field which the Hall IC converts into a proportional voltage. Device accuracy is optimized through the proximity of the primary conductor to the Hall transducer and factory programming of the sensitivity and quiescent output voltage at the Allegro factory.

Chopper-stabilized signal path and digital temperature compensation technology also contribute to the stability of the device across the operating temperature range.

High-level immunity to current conductor dV/dt and stray electric fields, offered by Allegro proprietary integrated shield technology for low-output voltage ripple and low-offset drift in high-side, high-voltage applications.

The output of the device has a positive slope ($>V_{CC}/2$) when an increasing current flows through the primary copper conduction

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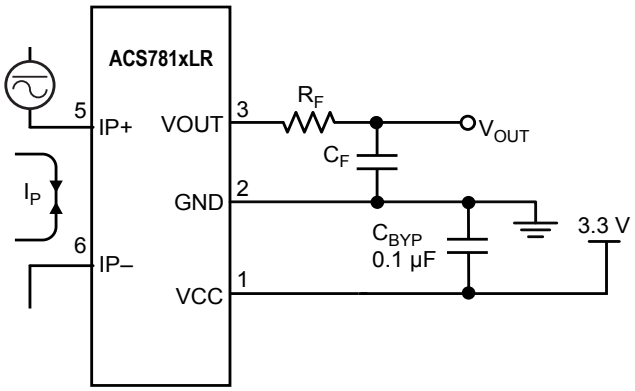

Typical Application

Application 1: The ACS781xLR outputs an analog signal, V_{OUT}, that varies linearly with the bidirectional AC or DC primary current, I_P, within the range specified. C_F is for optimal noise management, with values that depend on the application.

DESCRIPTION (CONTINUED)

path (from terminal 5 to terminal 6), which is the path used for current sampling. The internal resistance of this conductive path is 200 µΩ typical, providing low power loss.

The thickness of the copper conductor allows survival of the device at high overcurrent conditions. The terminals of the conductive path are electrically isolated from the signal leads (pins 1 through 4, and 7), and allows the device to operate safely with voltages up to 100 V peak on the primary conductor.

The device is fully calibrated prior to shipment from the factory. The ACS781xLR family is lead (Pb) free. All leads are plated with 100% matte tin, and there is no Pb inside the package. The heavy gauge leadframe is made of oxygen-free copper.

SELECTION GUIDE

Part Number	Sensed Current Direction	Primary Sampled Current, I_P (A)	Sensitivity Sens (Typ.) (mV/A)	T_{OP} (°C)	Packing [1]
ACS781LLRTR-050B-T	Bidirectional	±50	26.4	–40 to 150	Tape and reel
ACS781LLRTR-050U-T	Unidirectional	0 to 50	39.6		
ACS781LLRTR-100B-T	Bidirectional	±100	13.2		
ACS781LLRTR-100U-T	Unidirectional	0 to 100	26.4		
ACS781KLRTR-150B-T	Bidirectional	±150 transient ±100 continuous	8.8	–40 to 125	
ACS781KLRTR-150U-T	Unidirectional	0 to 150 transient 0 to 100 continuous	17.6		

[1] Contact Allegro for additional packing options.

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}		6	V
Reverse Supply Voltage	V_{RCC}		–0.5	V
Forward Output Voltage	V_{OUT}		25	V
Reverse Output Voltage	V_{RIOUT}		–0.5	V
Output Source Current	$I_{OUT(Source)}$	VOUT to GND	2.8	mA
Output Sink Current	$I_{OUT(Sink)}$	Minimum pull-up resistor of 500 Ω	10	mA
Nominal Operating Ambient Temperature	T_{OP}	Range K	–40 to 125	°C
		Range L	–40 to 150	°C
Maximum Junction	T_J(max)		165	°C
Storage Temperature	T_{stg}		–65 to 165	°C

THERMAL CHARACTERISTICS: May require derating at maximum conditions

Characteristic	Symbol	Test Conditions [1]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	Mounted on the Allegro evaluation board ASEK781 85-0807-001 with FR4 substrate and 8 layers of 2 oz. copper (with an area of 1530 mm^2 per layer) connected to the primary leadframe and with thermal vias connecting the copper layers. Performance is based on current flowing through the primary leadframe and includes the power consumed by the PCB.	18	°C/W

[1] Additional thermal information available on the Allegro website

TYPICAL OVERCURRENT CAPABILITIES [2][3]

Characteristic	Symbol	Notes	Rating	Unit
Overcurrent	I_{POC}	T_A = 25°C, 1 s on time, 60 s off time	285	A
		T_A = 85°C, 1 s on time, 35 s off time	225	A
		T_A = 125°C, 1 s on time, 30 s off time	170	A
		T_A = 150°C, 1 s on time, 10 s off time	95	A

[2] Test was done with Allegro evaluation board (85-0807-001). The maximum allowed current is limited by T_J(max) only.

[3] For more overcurrent profiles, please see FAQ on the Allegro website, www.allegromicro.com.

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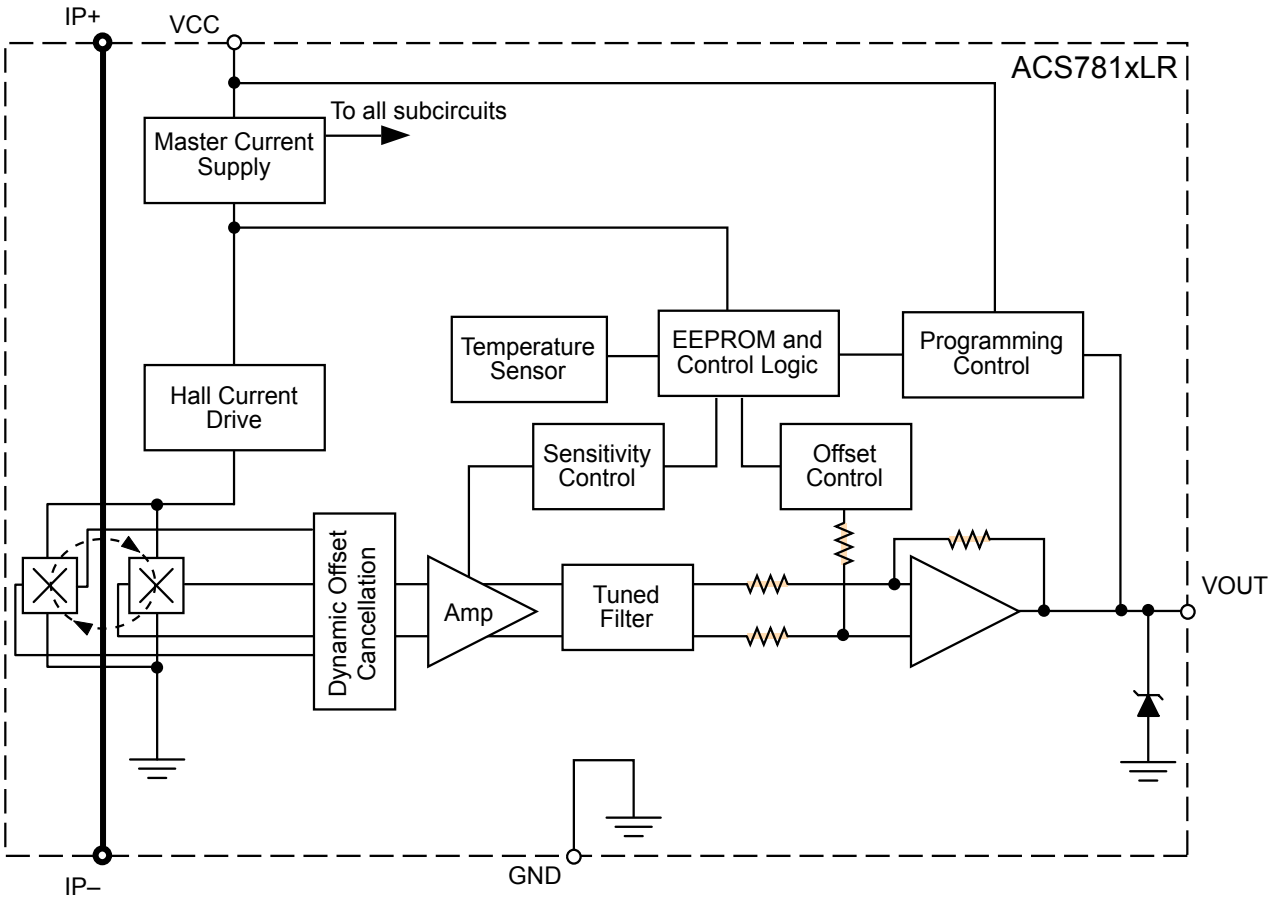
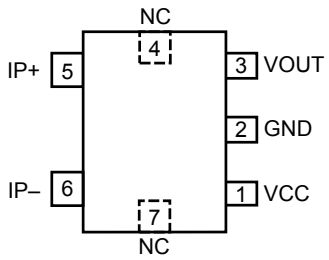


Functional Block Diagram



Pinout Diagram

Pinout List

Number	Name	Description
1	VCC	Device power supply terminal
2	GND	Signal ground terminal
3	VOUT	Analog output signal
4	NC	No connection, connect to GND for optimal ESD performance
5	IP+	Terminal for current being sampled
6	IP–	Terminal for current being sampled
7	NC	No connection, connect to GND for optimal ESD performance

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COMMON OPERATING CHARACTERISTICS: Valid at T_{OP} = –40°C to 150°C and V_{CC} = 3.3 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}		3	3.3	3.6	V
Supply Current	I_{CC}	Output open	–	11	15	mA
Power-On Time	t_{PO}	T_A = 25°C, C_{BYPASS} = Open, C_L = 1 nF	–	180	–	µs
Temperature Compensation Time	t_{TC}	C_{BYPASS} = Open, C_L = 1 nF	–	50	–	µs
Power-On Reset Voltage	V_{PORH}	T_A = 25°C, V_{CC} rising	–	2.85	–	V
	V_{PORL}	T_A = 25°C, V_{CC} falling	–	2.6	–	V
Power-On Reset Hysteresis	$V_{PORHYST}$		–	250	–	mV
Power-On Reset Release Time	t_{PORR}	T_A = 25°C, V_{CC} rising	–	150	–	µs
Power-On Reset Disable Time	t_{PORD}	T_A = 25°C, C_L = 1 nF	–	14	–	µs
Supply Zener Clamp Voltage	V_z	T_A = 25°C, I_{CC} = 30 mA	6.5	7.5	–	V
Internal Bandwidth	BW_i	Small signal –3 dB, C_L = 1 nF, T_A = 25°C	–	120	–	kHz
Chopping Frequency	f_C	T_A = 25°C	–	500	–	kHz
Oscillator Frequency	f_{OSC}	T_A = 25°C	–	8	–	MHz
OUTPUT CHARACTERISTICS						
Propagation Delay Time	t_{pd}	T_A = 25°C, C_L = 1 nF	–	2.2	–	µs
Rise Time	t_r	T_A = 25°C, C_L = 1 nF	–	3	–	µs
Response Time	$t_{RESPONSE}$	T_A = 25°C, C_L = 1 nF	–	3.6	–	µs
Output Saturation Voltage	$V_{SAT(HIGH)}$	T_A = 25°C, R_{LOAD} = 10 kΩ to GND	3.1	–	–	V
	$V_{SAT(LOW)}$	T_A = 25°C, R_{LOAD} = 10 kΩ to VCC	–	–	200	mV
DC Output Resistance	R_{OUT}	R_L = 4.7 kΩ from VOUT to GND, V_{OUT} = V_{CC}/2	–	<1	–	Ω
Output Load Resistance	$R_{L(PULLUP)}$	VOUT to VCC	4.7	–	–	kΩ
	$R_{L(PULLDWN)}$	VOUT to GND	4.7	–	–	kΩ
Output Load Capacitance	C_L	VOUT to GND	–	1	10	nF
Primary Conductor Resistance	$R_{PRIMARY}$	T_A = 25°C	–	200	–	µΩ
Quiescent Output Voltage	$V_{OUT(QBI)}$	I_P = 0 A, T_A = 25°C	–	V_{CC}/2	–	V
	$V_{OUT(QU)}$	Unidirectional variant, I_P = 0 A, T_A = 25°C	–	V_{CC} × 0.1	–	V
Ratiometry Quiescent Output Voltage Error	$Rat_{ERRVOUT(Q)}$	Through supply voltage range (V_{CC} = 3.3 V)	–	0	–	%
Ratiometry Sensitivity Error	$Rat_{ERRSens}$	Through supply voltage range (V_{CC} = 3.3 V)	–	< ±0.5	–	%
Common-Mode Magnetic Field Rejection	CMFR	Magnetic field perpendicular to Hall plates	–	–35	–	dB

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*X*050B PERFORMANCE CHARACTERISTICS [1]: T_{OP} = –40°C to 150°C, V_{CC} = 3.3 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Primary Sampled Current	I_P		–50	–	50	A
Sensitivity	$Sens_{TA}$	Measured using 50% of full-scale I_P, T_A = 25°C	25.5	26.4	27.258	mV/A
	$Sens_{(TOP)HT}$	Measured using 50% of full-scale I_P, T_{OP} = 25°C to 150°C	25.542	26.4	27.258	mV/A
	$Sens_{(TOP)LT}$	Measured using 50% of full-scale I_P, T_{OP} = –40°C to 25°C	25.41	26.4	27.39	mV/A
Noise [2]	$V_{NOISEPP}$	Peak-to-peak, T_A= 25°C, 1 nF on VOUT pin to GND	–	36	–	mV
	I_{NOISE}	Input referred	–	0.6	–	$mA_{RMS}/\sqrt{(Hz)}$
Nonlinearity	E_{LIN}	Measured using ±32 A and ±16 A	–1	–	1	%
Electrical Offset Voltage [3][4]	$V_{OE(TA)}$	I_P = 0 A, T_A = 25°C	–10	±3	10	mV
	$V_{OE(TOP)HT}$	I_P = 0 A, T_{OP} = 25°C to 150°C	–10	±5	10	mV
	$V_{OE(TOP)LT}$	I_P = 0 A, T_{OP} = –40°C to 25°C	–20	±10	20	mV
Electric Offset Voltage Over Lifetime [5]	$\Delta V_{OE(LIFE)}$	T_{OP} = –40°C to 150°C, estimated shift after AEC-Q100 grade 0 qualification testing	–	±1	–	mV
Total Output Error	$E_{TOT(HT)}$	Measured using 50% of full-scale I_P, T_{OP} = 25°C to 150°C	–3.25	±0.8	3.25	%
	$E_{TOT(LT)}$	Measured using 50% of full-scale I_P, T_{OP} = –40°C to 25°C	–3.75	±1.5	3.75	%
Total Output Error Including Lifetime Drift [6]	$E_{TOT(HT,LIFE)}$	Measured using 50% of full-scale I_P, T_{OP} = 25°C to 150°C	–4.1	±2.28	4.1	%
	$E_{TOT(LT,LIFE)}$	Measured using 50% of full-scale I_P, T_{OP} = –40°C to 25°C	–5.6	±2.98	5.6	%

[1] See Characteristic Performance Data page for parameter distributions over temperature range.
[2] ±3 sigma noise voltage.
[3] Drift is referred to ideal $V_{OUT(QBI)}$ = 1.65 V.
[4] This parameter may drift a maximum of $\Delta V_{OE(LIFE)}$ over lifetime.
[5] Based on characterization data obtained during standardized stress test for Qualification of Integrated Circuits, including Package Hysteresis. Cannot be guaranteed. Drift is a function of customer application conditions. Contact Allegro MicroSystems for further information.
[6] The maximum drift of any single device during qualification testing was 4%. Total Output Error Including Lifetime Drift incorporates both sensitivity over lifetime and electrical offset voltage over lifetime.

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Primary Sampled Current	I_P		0	–	50	A
Sensitivity	$Sens_{TA}$	Measured using 50% of full-scale I_P, T_A = 25°C	38.3	39.6	40.887	mV/A
	$Sens_{(TOP)HT}$	Measured using 50% of full-scale I_P, T_{OP} = 25°C to 150°C	38.313	39.6	40.887	mV/A
	$Sens_{(TOP)LT}$	Measured using 50% of full-scale I_P, T_{OP} = –40°C to 25°C	38.115	39.6	41.085	mV/A
Noise [2]	$V_{NOISEPP}$	Peak-to-peak, T_A= 25°C, 1 nF on VOUT pin to GND	–	35.6	–	mV
	I_{NOISE}	Input referred	–	0.6	–	$mA_{RMS}/\sqrt{(Hz)}$
Nonlinearity	E_{LIN}	Measured using 32 A and 16 A	–1	–	1	%
Electrical Offset Voltage [3][4]	$V_{OE(TA)}$	I_P = 0 A, T_A = 25°C	–10	±3	10	mV
	$V_{OE(TOP)HT}$	I_P = 0 A, T_{OP} = 25°C to 150°C	–10	±5	10	mV
	$V_{OE(TOP)LT}$	I_P = 0 A, T_{OP} = –40°C to 25°C	–20	±10	20	mV
Electric Offset Voltage Over Lifetime [5]	$\Delta V_{OE(LIFE)}$	T_{OP} = –40°C to 150°C, estimated shift after AEC-Q100 grade 0 qualification testing	–	±1	–	mV
Total Output Error	$E_{TOT(HT)}$	Measured using 50% of full-scale I_P, T_{OP} = 25°C to 150°C	–3.25	±0.8	3.25	%
	$E_{TOT(LT)}$	Measured using 50% of full-scale I_P, T_{OP} = –40°C to 25°C	–3.75	±1.5	3.75	%
Total Output Error Including Lifetime Drift [6]	$E_{TOT(HT,LIFE)}$	Measured using 50% of full-scale I_P, T_{OP} = 25°C to 150°C	–4.1	±2.28	4.1	%
	$E_{TOT(LT,LIFE)}$	Measured using 50% of full-scale I_P, T_{OP} = –40°C to 25°C	–5.6	±2.98	5.6	%

[1] See Characteristic Performance Data page for parameter distributions over temperature range.
[2] ±3 sigma noise voltage.
[3] Drift is referred to ideal $V_{OUT(QU)}$= 0.33 V.
[4] This parameter may drift a maximum of $\Delta V_{OE(LIFE)}$ over lifetime.
[5] Based on characterization data obtained during standardized stress test for Qualification of Integrated Circuits, including Package Hysteresis. Cannot be guaranteed. Drift is a function of customer application conditions. Contact Allegro MicroSystems for further information.
[6] The maximum drift of any single device during qualification testing was 4%. Total Output Error Including Lifetime Drift incorporates both sensitivity over lifetime and electrical offset voltage over lifetime.

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*X*100B PERFORMANCE CHARACTERISTICS [1]: T_{OP} = –40°C to 150°C, V_{CC} = 3.3 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Primary Sampled Current	I_P		–100	–	100	A
Sensitivity	$Sens_{TA}$	Measured using 33% of full-scale I_P, T_A = 25°C	12.8	13.2	13.629	mV/A
	$Sens_{(TOP)HT}$	Measured using 33% of full-scale I_P, T_{OP} = 25°C to 150°C	12.771	13.2	13.629	mV/A
	$Sens_{(TOP)LT}$	Measured using 33% of full-scale I_P, T_{OP} = –40°C to 25°C	12.705	13.2	13.695	mV/A
Noise [2]	$V_{NOISEPP}$	Peak-to-peak, T_A = 25°C, 1 nF on VOUT pin to GND	–	18	–	mV
	I_{NOISE}	Input referred	–	0.6	–	$mA_{RMS}/\sqrt{(Hz)}$
Nonlinearity	E_{LIN}	Measured using ±36 A and ±18 A	–1	–	1	%
Electrical Offset Voltage [3][4]	$V_{OE(TA)}$	I_P = 0 A, T_A = 25°C	–10	±3	10	mV
	$V_{OE(TOP)HT}$	I_P = 0 A, T_{OP} = 25°C to 150°C	–10	±5	10	mV
	$V_{OE(TOP)LT}$	I_P = 0 A, T_{OP} = –40°C to 25°C	–20	±10	20	mV
Electric Offset Voltage Over Lifetime [5]	$\Delta V_{OE(LIFE)}$	T_{OP} = –40°C to 150°C, estimated shift after AEC-Q100 grade 0 qualification testing	–	±1	–	mV
Total Output Error	$E_{TOT(HT)}$	Measured using 33% of full-scale I_P, T_{OP} = 25°C to 150°C	–3.25	±0.8	3.25	%
	$E_{TOT(LT)}$	Measured using 33% of full-scale I_P, T_{OP} = –40°C to 25°C	–3.75	±1.5	3.75	%
Total Output Error Including Lifetime Drift [6]	$E_{TOT(HT,LIFE)}$	Measured using 33% of full-scale I_P, T_{OP} = 25°C to 150°C	–4.1	±2.28	4.1	%
	$E_{TOT(LT,LIFE)}$	Measured using 33% of full-scale I_P, T_{OP} = –40°C to 25°C	–5.6	±2.98	5.6	%

[1] See Characteristic Performance Data page for parameter distributions over temperature range.
[2] ±3 sigma noise voltage.
[3] Drift is referred to ideal $V_{OUT(QBI)}$ = 1.65 V.
[4] This parameter may drift a maximum of $\Delta V_{OE(LIFE)}$ over lifetime.
[5] Based on characterization data obtained during standardized stress test for Qualification of Integrated Circuits, including Package Hysteresis. Cannot be guaranteed. Drift is a function of customer application conditions. Contact Allegro MicroSystems for further information.
[6] The maximum drift of any single device during qualification testing was 4%. Total Output Error Including Lifetime Drift incorporates both sensitivity over lifetime and electrical offset voltage over lifetime.

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Primary Sampled Current	I_P		0	–	100	A
Sensitivity	$Sens_{TA}$	Measured using 33% of full-scale I_P, T_A = 25°C	25.5	26.4	27.258	mV/A
	$Sens_{(TOP)HT}$	Measured using 33% of full-scale I_P, T_{OP} = 25°C to 150°C	25.542	26.4	27.258	mV/A
	$Sens_{(TOP)LT}$	Measured using 33% of full-scale I_P, T_{OP} = –40°C to 25°C	25.41	26.4	27.39	mV/A
Noise [2]	$V_{NOISEPP}$	Peak-to-peak, T_A= 25°C, 1 nF on VOUT pin to GND	–	36	–	mV
	I_{NOISE}	Input referred	–	0.6	–	$mA_{RMS}/\sqrt{(Hz)}$
Nonlinearity	E_{LIN}	Measured using 36 A and 18 A	–1	–	1	%
Electrical Offset Voltage [3][4]	$V_{OE(TA)}$	I_P = 0 A, T_A = 25°C	–10	±3	10	mV
	$V_{OE(TOP)HT}$	I_P = 0 A, T_{OP} = 25°C to 150°C	–10	±5	10	mV
	$V_{OE(TOP)LT}$	I_P = 0 A, T_{OP} = –40°C to 25°C	–20	±10	20	mV
Electric Offset Voltage Over Lifetime [5]	$\Delta V_{OE(LIFE)}$	T_{OP} = –40°C to 150°C, estimated shift after AEC-Q100 grade 0 qualification testing	–	±1	–	mV
Total Output Error	$E_{TOT(HT)}$	Measured using 33% of full-scale I_P, T_{OP} = 25°C to 150°C	–3.25	±0.8	3.25	%
	$E_{TOT(LT)}$	Measured using 33% of full-scale I_P, T_{OP} = –40°C to 25°C	–3.75	±1.5	3.75	%
Total Output Error Including Lifetime Drift [6]	$E_{TOT(HT,LIFE)}$	Measured using 33% of full-scale I_P, T_{OP} = 25°C to 150°C	–4.1	±2.28	4.1	%
	$E_{TOT(LT,LIFE)}$	Measured using 33% of full-scale I_P, T_{OP} = –40°C to 25°C	–5.6	±2.98	5.6	%

[1] See Characteristic Performance Data page for parameter distributions over temperature range.
[2] ±3 sigma noise voltage.
[3] Drift is referred to ideal $V_{OUT(QU)}$ = 0.33 V.
[4] This parameter may drift a maximum of $\Delta V_{OE(LIFE)}$ over lifetime.
[5] Based on characterization data obtained during standardized stress test for Qualification of Integrated Circuits, including Package Hysteresis. Cannot be guaranteed. Drift is a function of customer application conditions. Contact Allegro MicroSystems for further information.
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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Primary Sampled Current	I_P	Transient	–150	–	150	A
		Continuous	–100	–	100	A
Sensitivity	$Sens_{TA}$	Measured using 25% of full-scale I_P, T_A = 25°C	8.5	8.8	9.08	mV/A
	$Sens_{(TOP)HT}$	Measured using 25% of full-scale I_P, T_{OP} = 25°C to 125°C	8.51	8.8	9.08	mV/A
	$Sens_{(TOP)LT}$	Measured using 25% of full-scale I_P, T_{OP} = –40°C to 25°C	8.47	8.8	9.13	mV/A
Noise [2]	$V_{NOISEPP}$	Peak-to-peak, T_A = 25°C, 1 nF on VOUT pin to GND	–	12	–	mV
	I_{NOISE}	Input referred	–	0.6	–	$mA_{RMS}/\sqrt{(Hz)}$
Nonlinearity	E_{LIN}	Measured using ±38 A and ±19 A	–1	–	1	%
Electrical Offset Voltage [3][4]	$V_{OE(TA)}$	I_P = 0 A, T_A = 25°C	–10	±3	10	mV
	$V_{OE(TOP)HT}$	I_P = 0 A, T_{OP} = 25°C to 125°C	–10	±5	10	mV
	$V_{OE(TOP)LT}$	I_P = 0 A, T_{OP} = –40°C to 25°C	–20	±10	20	mV
Electric Offset Voltage Over Lifetime [5]	$\Delta V_{OE(LIFE)}$	T_{OP} = –40°C to 125°C, estimated shift after AEC-Q100 grade 0 qualification testing	–	±1	–	mV
Total Output Error	$E_{TOT(HT)}$	Measured using 25% of full-scale I_P, T_{OP} = 25°C to 125°C	–3.25	±0.8	3.25	%
	$E_{TOT(LT)}$	Measured using 25% of full-scale I_P, T_{OP} = –40°C to 25°C	–3.75	±1.5	3.75	%
Total Output Error Including Lifetime Drift [6]	$E_{TOT(HT,LIFE)}$	Measured using 25% of full-scale I_P, T_{OP} = 25°C to 125°C	–4.1	±2.28	4.1	%
	$E_{TOT(LT,LIFE)}$	Measured using 25% of full-scale I_P, T_{OP} = –40°C to 25°C	–5.6	±2.98	5.6	%

[1] See Characteristic Performance Data page for parameter distributions over temperature range.
[2] ±3 sigma noise voltage.
[3] Drift is referred to ideal $V_{OUT(QBI)}$ = 1.65 V.
[4] This parameter may drift a maximum of $\Delta V_{OE(LIFE)}$ over lifetime.
[5] Based on characterization data obtained during standardized stress test for Qualification of Integrated Circuits, including Package Hysteresis. Cannot be guaranteed. Drift is a function of customer application conditions. Contact Allegro MicroSystems for further information.
[6] The maximum drift of any single device during qualification testing was 4%. Total Output Error Including Lifetime Drift incorporates both sensitivity over lifetime and electrical offset voltage over lifetime.

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*X*150U PERFORMANCE CHARACTERISTICS [1]: T_{OP} = –40°C to 125°C, V_{CC} = 3.3 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Primary Sampled Current	I_P	Transient	0	–	150	A
		Continuous	0	–	100	A
Sensitivity	$Sens_{TA}$	Measured using 25% of full-scale I_P, T_A = 25°C	17.0	17.6	18.17	mV/A
	$Sens_{(TOP)HT}$	Measured using 25% of full-scale I_P, T_{OP} = 25°C to 125°C	17.02	17.6	18.17	mV/A
	$Sens_{(TOP)LT}$	Measured using 25% of full-scale I_P, T_{OP} = –40°C to 25°C	16.94	17.6	18.26	mV/A
Noise [2]	$V_{NOISEPP}$	Peak-to-peak, T_A= 25°C, 1 nF on VOUT pin to GND	–	24	–	mV
	I_{NOISE}	Input referred	–	0.6	–	mA_{RMS} /√(Hz)
Nonlinearity	E_{LIN}	Measured using 38 A and 19 A	–1	–	1	%
Electrical Offset Voltage [3][4]	$V_{OE(TA)}$	I_P = 0 A, T_A = 25°C	–10	±3	10	mV
	$V_{OE(TOP)HT}$	I_P = 0 A, T_{OP} = 25°C to 125°C	–10	±5	10	mV
	$V_{OE(TOP)LT}$	I_P = 0 A, T_{OP} = –40°C to 25°C	–20	±10	20	mV
Electric Offset Voltage Over Lifetime [5]	$\Delta V_{OE(LIFE)}$	T_{OP} = –40°C to 125°C, estimated shift after AEC-Q100 grade 0 qualification testing	–	±1	–	mV
Total Output Error	$E_{TOT(HT)}$	Measured using 25% of full-scale I_P, T_{OP} = 25°C to 125°C	–3.25	±0.8	3.25	%
	$E_{TOT(LT)}$	Measured using 25% of full-scale I_P, T_{OP} = –40°C to 25°C	–3.75	±1.5	3.75	%
Total Output Error Including Lifetime Drift [6]	$E_{TOT(HT,LIFE)}$	Measured using 25% of full-scale I_P, T_{OP} = 25°C to 125°C	–4.1	±2.28	4.1	%
	$E_{TOT(LT,LIFE)}$	Measured using 25% of full-scale I_P, T_{OP} = –40°C to 25°C	–5.6	±2.98	5.6	%

[1] See Characteristic Performance Data page for parameter distributions over temperature range.
[2] ±3 sigma noise voltage.
[3] Drift is referred to ideal $V_{OUT(QU)}$ = 0.33 V.
[4] This parameter may drift a maximum of $\Delta V_{OE(LIFE)}$ over lifetime.
[5] Based on characterization data obtained during standardized stress test for Qualification of Integrated Circuits, including Package Hysteresis. Cannot be guaranteed. Drift is a function of customer application conditions. Contact Allegro MicroSystems for further information.
[6] The maximum drift of any single device during qualification testing was 4%. Total Output Error Including Lifetime Drift incorporates both sensitivity over lifetime and electrical offset voltage over lifetime.

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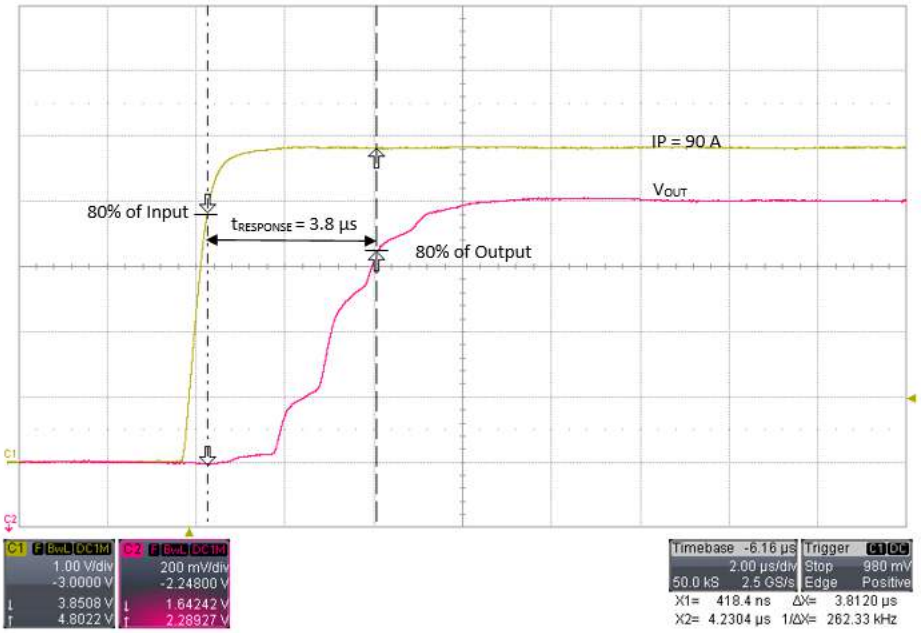
CHARACTERISTIC PERFORMANCE DATA
DATA TAKEN USING THE ACS781KLR-150B

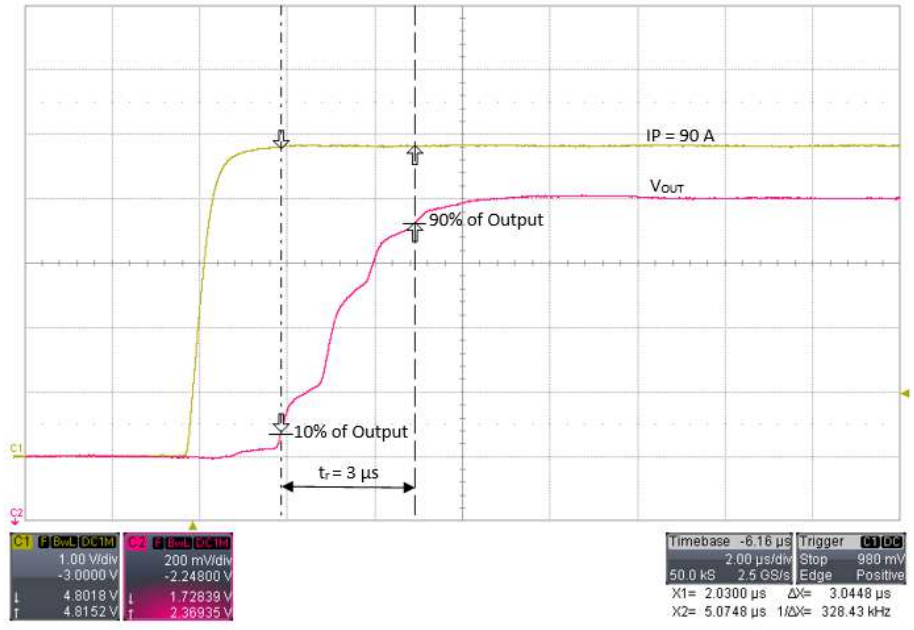
Response Time ($t_{RESPONSE}$)

I_P = 90 A with 10-90% rise time = 1 µs, C_{BYPASS} = 0.1 µF, CL = 1 nF



Rise Time (t_r)

I_P = 90 A with 10%-90% rise time = 1 µs, C_{BYPASS} = 0.1 µF, C_L = 1 nF



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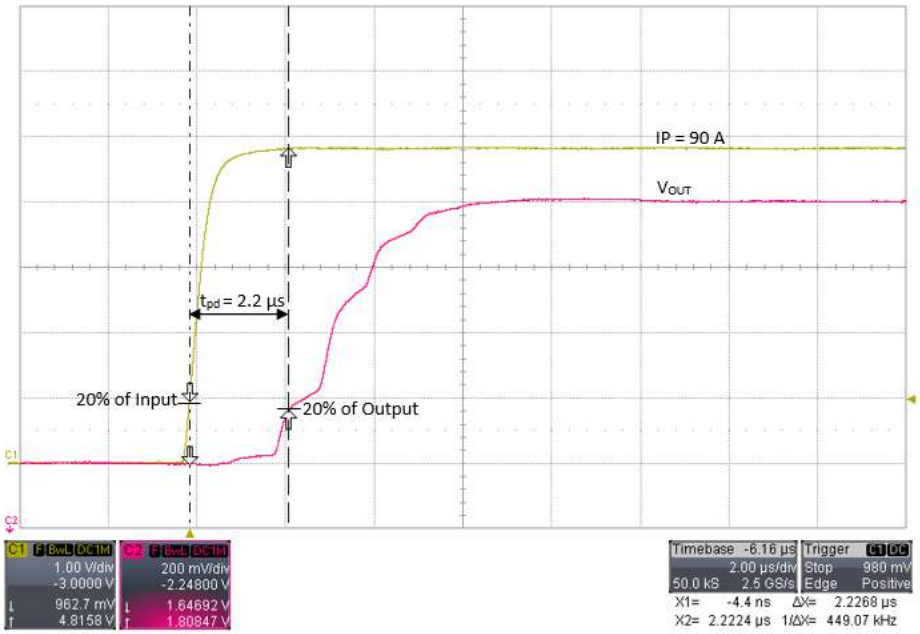
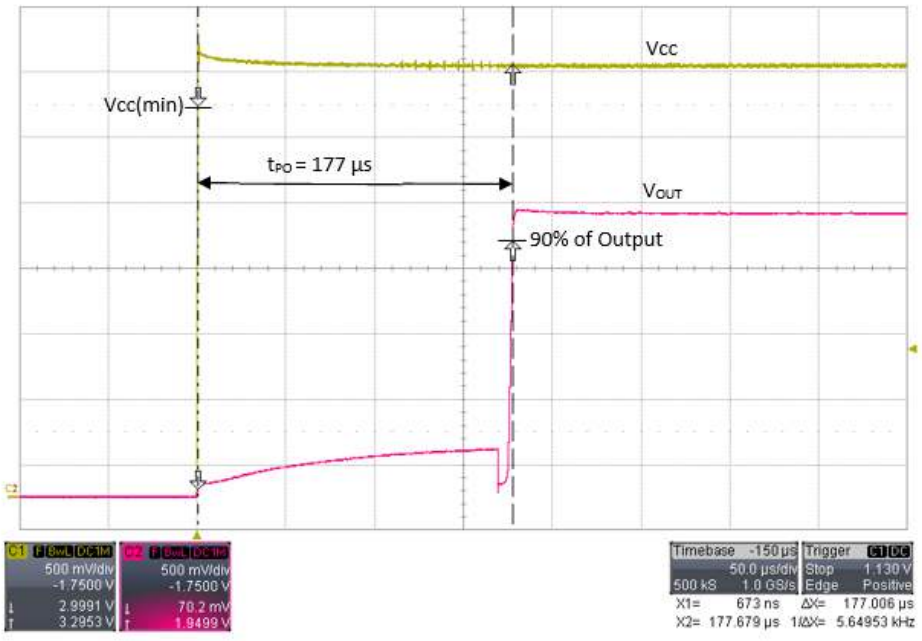
Propagation Delay (t_{PD})

I_P = 90 A with 10% - 90% rise time = 1 µs, C_{BYPASS} = 0.1 µF, C_L = 1 nF



Power-On Time (t_{PO})

I_P = 60 A DC, C_{BYPASS} = Open, C_L = 1 nF



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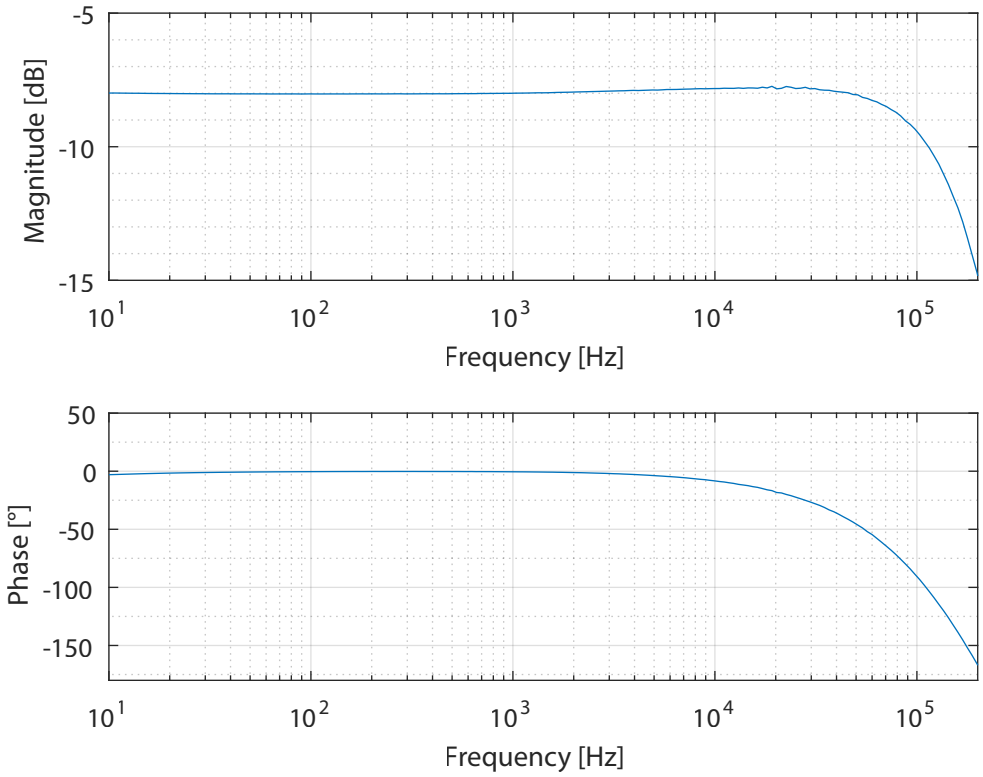
CHARACTERISTIC PERFORMANCE

ACS781 TYPICAL FREQUENCY RESPONSE



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CHARACTERISTIC DEFINITIONS

Definitions of Accuracy Characteristics

SENSITIVITY (Sens)

The change in device output in response to a 1 A change through the primary conductor. The sensitivity is the product of the magnetic circuit sensitivity (G/A) and the linear IC amplifier gain (mV/G). The linear IC amplifier gain is programmed at the factory to optimize the sensitivity (mV/A) for the half-scale current of the device.

NOISE (V_{NOISE})

The noise floor is derived from the thermal and shot noise observed in Hall elements. Dividing the noise (mV) by the sensitivity (mV/A) provides the smallest current that the device can resolve.

NONLINEARITY (E_{LIN})

The ACS781xLR is designed to provide a linear output in response to a ramping current. Consider two current levels: I1 and I2. Ideally, the sensitivity of a device is the same for both currents, for a given supply voltage and temperature. Nonlinearity is present when there is a difference between the sensitivities measured at I1 and I2. Nonlinearity is calculated separately for the positive (E_{LINpos}) and negative (E_{LINneg}) applied currents as follows:

$$E_{LINpos} = 100\ (\%) \times \{1 - (Sens_{IPOS2} / Sens_{IPOS1})\}$$

$$E_{LINneg} = 100\ (\%) \times \{1 - (Sens_{INEG2} / Sens_{INEG1})\}$$

where:

$$Sens_{Ix} = (V_{IOUT(Ix)} - V_{IOUT(Q)}) / Ix$$

and I_{POSx} and I_{NEGx} are positive and negative currents.

Then:

$$E_{LIN} = \max(E_{LINpos}, E_{LINneg})$$

RATIOMETRY

The device features a ratiometric output. This means that the quiescent voltage output, V_{OUTQ}, and the magnetic sensitivity, Sens, are proportional to the supply voltage, V_{CC}. The ratiometric change (%) in the quiescent voltage output is defined as:

$$Rat_{ERRVOUT(Q)} = \left(1 - \frac{V_{OUT(Q)(V_{CC})} / V_{OUT(Q)(3.3V)}}{V_{CC} / 3.3\ V}\right) \times 100\%$$

and the ratiometric change (%) in sensitivity is defined as:

$$Rat_{ERRSens} = \left(1 - \frac{Sens_{(V_{CC})} / Sens_{(3.3V)}}{V_{CC} / 3.3\ V}\right) \times 100\%$$

QUIESCENT OUTPUT VOLTAGE ($V_{OUT(Q)}$)

The output of the device when the primary current is zero. For bidirectional sensors, it nominally remains at $V_{CC}/2$ and for unidirectional sensors at $0.1 \times V_{CC}$. Thus, V_{CC} = 3.3 V translates into $V_{OUT(BI)}$ = 1.65 V and $V_{OUT(QU)}$ = 0.33 V. Variation in $V_{OUT(Q)}$ can be attributed to the resolution of the Allegro linear IC quiescent voltage trim and thermal drift.

ELECTRICAL OFFSET VOLTAGE (V_{OE})

The deviation of the device output from its ideal quiescent value due to nonmagnetic causes.

TOTAL OUTPUT ERROR (E_{TOT})

The maximum deviation of the actual output from its ideal value, also referred to as *accuracy*, illustrated graphically in the output voltage versus current chart on the following page.

E_{TOT} is divided into four areas:

- **0 A at 25°C.** Accuracy at the zero current flow at 25°C, without the effects of temperature.
- **0 A over Δ temperature.** Accuracy at the zero current flow including temperature effects.
- **Full-scale current at 25°C.** Accuracy at the full-scale current at 25°C, without the effects of temperature.
- **Full-scale current over Δ temperature.** Accuracy at the full-scale current flow including temperature effects.

$$E_{TOT(IP)} = \frac{V_{IOUT(IP)} - V_{IOUT\_IDEAL(IP)}}{Sens_{IDEAL} \times I_P} \times 100\ (\%)$$

where

$$V_{IOUT\_IDEAL(IP)} = V_{IOUT(Q)} + (Sens_{IDEAL} \times I_P)$$

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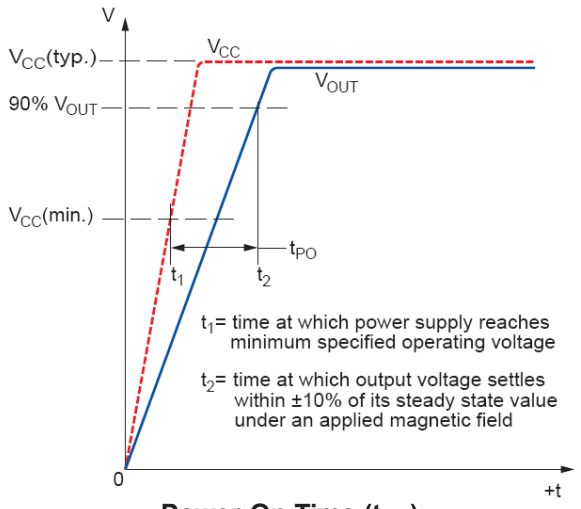
DEFINITIONS OF DYNAMIC RESPONSE CHARACTERISTICS

POWER-ON TIME (t_{PO})

When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before responding to an input magnetic field.

Power-On Time, t_{PO}, is defined as the time it takes for the output voltage to settle within ±10% of its steady state value under an applied magnetic field, after the power supply has reached its minimum specified operating voltage, V_{CC}(min), as shown in the chart at right.



Power-On Time (t_{PO})

RISE TIME (t_r)

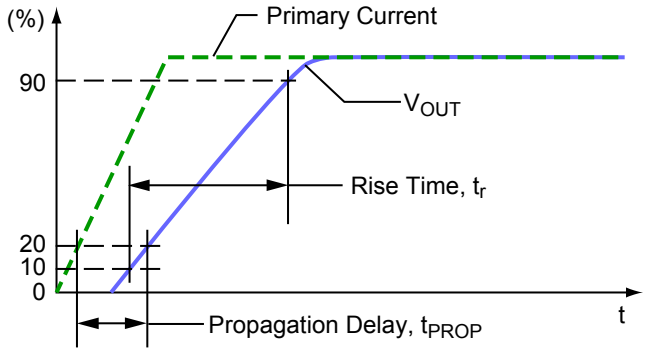
The time interval between a) when the device reaches 10% of its full-scale value, and b) when it reaches 90% of its full scale value. Both t_r and $t_{RESPONSE}$ are detrimentally affected by eddy current losses observed in the conductive IC ground plane.

RESPONSE TIME ($t_{RESPONSE}$)

The time interval between a) when the applied current reaches 80% of its final value, and b) when the sensor reaches 80% of its output corresponding to the applied current.

PROPAGATION DELAY (t_{PD})

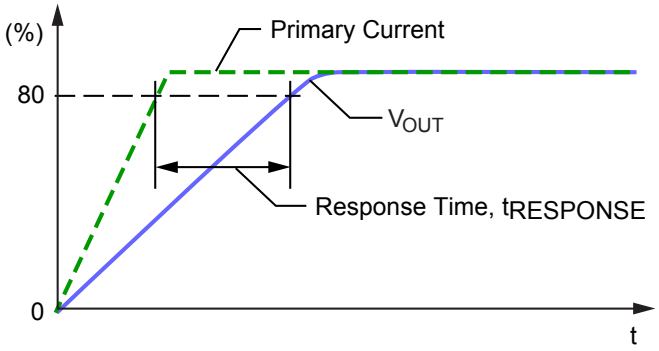
The time interval between a) when the input current reaches 20% of its final value, and b) when the output reaches 20% of its final value.



Propagation Delay (t_{PD}) and Rise Time (t_r)

POWER-ON RESET VOLTAGE (V_{POR})

At power-up, to initialize to a known state and avoid current spikes, the sensor is held in Reset state. The Reset signal is disabled when V_{CC} reaches V_{PORH} and time t_{PORR} has elapsed, allowing output voltage to go from a high-impedance state into normal operation. During power-down, the Reset signal is enabled when V_{CC} reaches V_{PORL}, causing output voltage to go into a high-impedance state. (Note that a detailed description of POR operation can be found in the Functional Description section.)



Response Time ($t_{RESPONSE}$)

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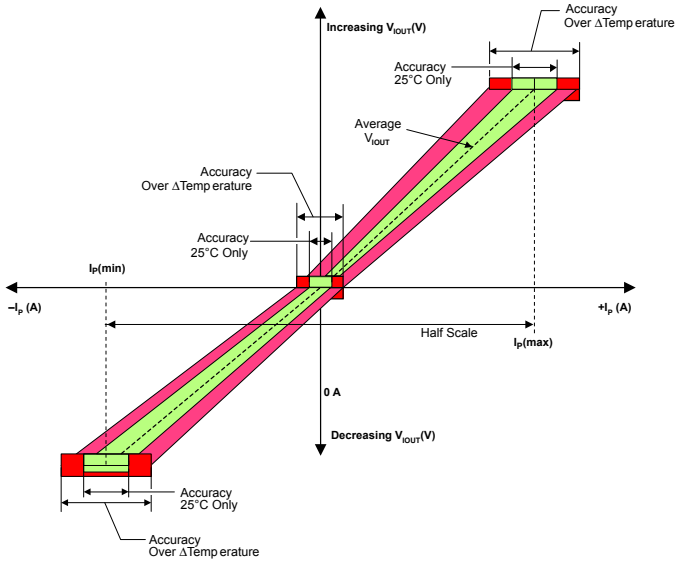
POWER-ON RESET RELEASE TIME (t_{PORR})

When V_{CC} rises to V_{PORH}, the Power-On Reset Counter starts. The sensor output voltage will transition from a high-impedance state to normal operation only when the Power-On Reset Counter has reached t_{PORR}.



Output Voltage versus Sampled Current
Total Output Error at 0 A and at Full-Scale Current

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FUNCTIONAL DESCRIPTION

Power-On Reset (POR)

The descriptions in this section assume: temperature = 25°C, no output load (R_L, C_L) , and I_P = 0 A.

- ***Power-Up.*** At power-up, as V_{CC} ramps up, the output is in a high-impedance state. When V_{CC} crosses V_{PORH} (location [1] in Figure 1 and [1'] in Figure 2), the POR Release counter starts counting for t_{PORRC} [2], [2']. At this point, the EEPROM content will be loaded in volatile memory after t_{EELOAD} [3],[3'] and the output will go to V_{CC}/ 2 after t_{PORD} [4], [4']. The temperature compensation engine will then adjust the device Sensitivity and QVO after time t_{TC} [5], [5']. ***V_{CC} drops below V_{CC}(min) = 3.0 V.*** If V_{CC} drops below V_{PORH} [6'] but remains higher than V_{PORL} [7'] the output will continue to be V_{CC} /2.
- ***Power-Down.*** As V_{CC} ramps down below V_{PORL} [6],[8'], the output will enter a high-impedance state.

EEPROM Error Checking and Correction

Hamming code methodology is implemented for EEPROM checking and correction. The device has ECC enabled after power-up. If an uncorrectable error has occurred, the VOUT pin will go to high impedance and the device will not respond to applied magnetic field.

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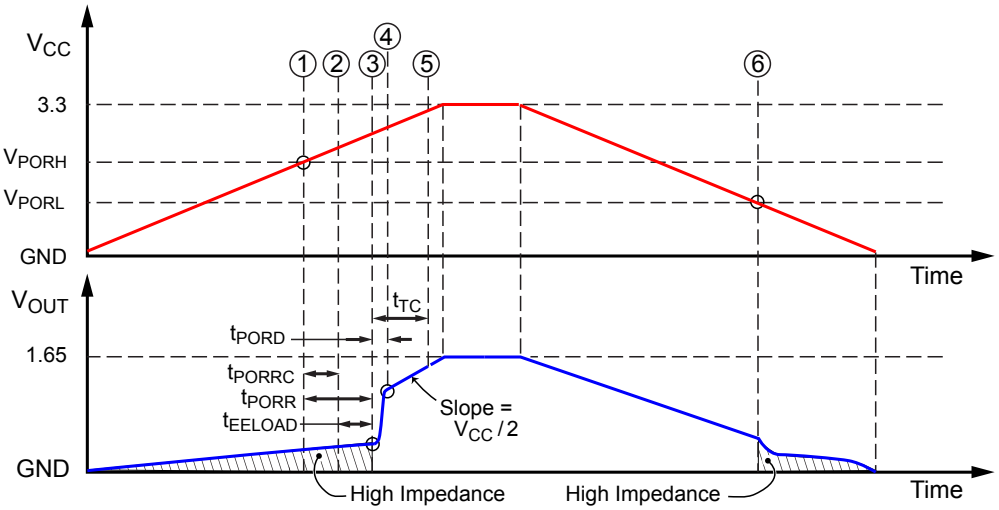

Figure 1: POR Operation: Slow Rise Time Case

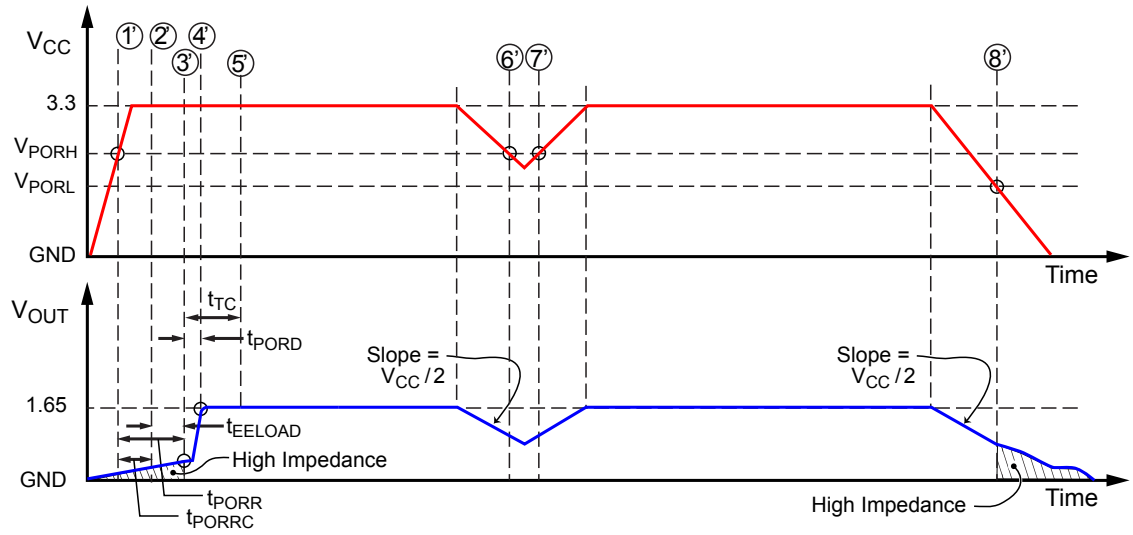

Figure 2: POR Operation: Fast Rise Time Case

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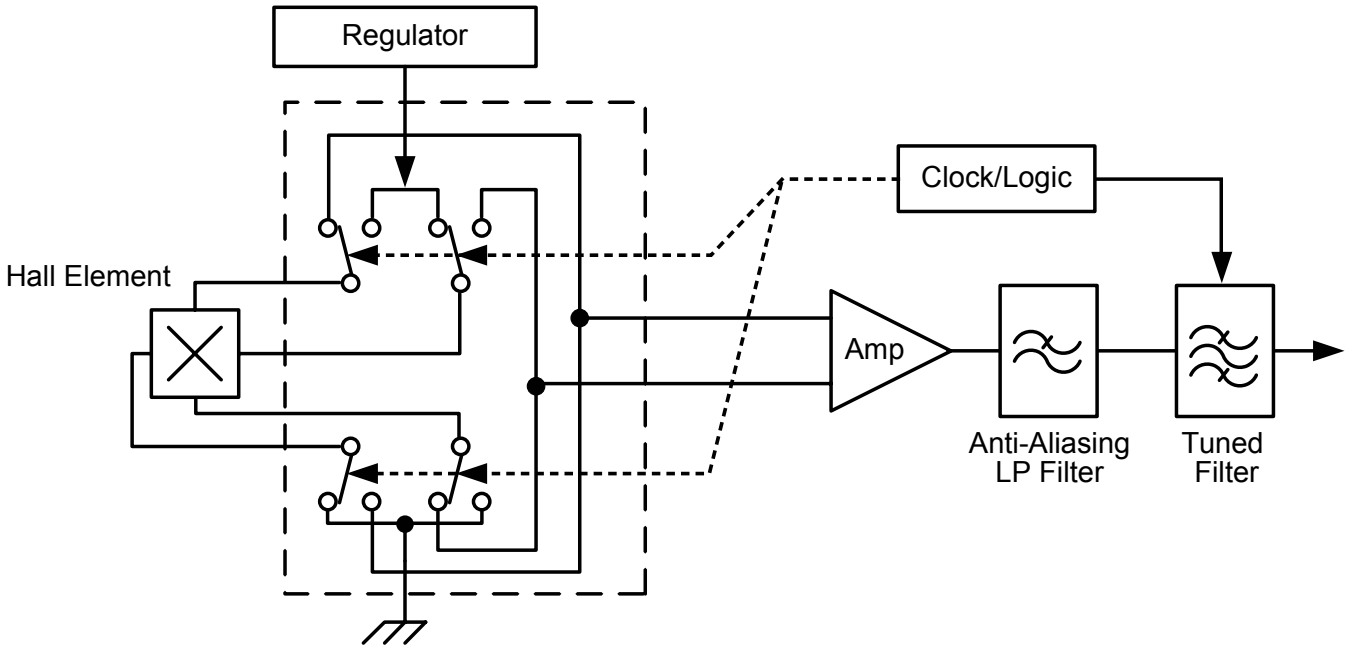
Chopper Stabilization Technique

When using Hall-effect technology, a limiting factor for switch point accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionally small relative to the offset that can be produced at the output of the Hall sensor IC. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges.

Chopper stabilization is a unique approach used to minimize Hall offset on the chip. Allegro employs a technique to remove key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain, through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field-induced signal to recover its original spectrum at baseband, while the DC offset becomes a high-frequency signal. The magnetic-sourced signal then can pass through a low-pass filter, while the modulated DC offset is suppressed.

In addition to the removal of the thermal and stress-related offset, this novel technique also reduces the amount of thermal noise in the Hall sensor IC while completely removing the modulated residue resulting from the chopper operation. The chopper stabilization technique uses a high-frequency sampling clock. For demodulation process, a sample-and-hold technique is used. This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible by using a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.



Concept of Chopper Stabilization Technique

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APPLICATION-SPECIFIC INFORMATION

Field from Nearby Current Path

To best use the CMR capabilities of these devices, the circuit board containing the ICs should be designed to make the external magnetic fields on both Hall plates equal. This helps to minimize error due to external fields generated by the current-carrying PCB traces themselves. There are three main parameters for each current-carrying trace that determine the error that it will induce on an IC: *distance* from the IC, *width* of the current-carrying conductor, and the *angle* between it and the IC. Figure 3 shows an example of a current-carrying conductor routed near an IC. The distance between the device and the conductor, *d*, is the distance from the device center to the center of the conductor. The width of the current path is *w*. The angle between the device and the current path, *θ*, is defined as the angle between a straight line connecting the two Hall plates and a line perpendicular to the current path.

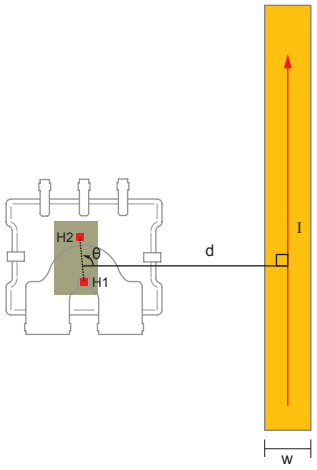

Figure 3: ACS781 with nearby current path, viewed from the bottom of the sensor

When it is not possible to keep θ close to 90°, the next best option is to keep the distance from the current path to the current sensor IC, d, as large as possible. Assuming that the current path is at the worst-case angle in relation to the IC, θ = 0° or 180°, the equation:

$$Error = \frac{2 \times I}{Cf} \times \left[\frac{1}{d - \frac{H_{space}}{2} \times \cos\theta} - \frac{1}{d + \frac{H_{space}}{2} \times \cos\theta} \right]$$

where H_{space} is the distance between the two Hall plates and Cf is the coupling factor of the IC. This coupling factor varies between the different ICs. The ACS781 has a coupling factor of 5 to 5.5 G/A, whereas other Allegro ICs can range from 10 to 15 G/A.

Other Layout Practices to Consider

When laying out a board that contains an Allegro current sensor IC with CMR, the direction and proximity of all current-carrying paths are important, but they are not the only factors to consider when optimizing IC performance. Other sources of stray fields that can contribute to system error include traces that connect to the IC's integrated current conductor, as well as the position of nearby permanent magnets.

The way that the circuit board connects to a current sensor IC must be planned with care. Common mistakes that can impact performance are:

- The angle of approach of the current path to the I_P pins
- Extending the current trace too far beneath the IC

THE ANGLE OF APPROACH

One common mistake when using an Allegro current sensor IC is to bring the current in from an undesirable angle. Figure 4 shows an example of the approach of the current traces to the IC (in this case, the ACS781). In this figure, traces are shown for I_P+ and I_P–. The light green region is the desired area of approach for the current trace going to I_P+. This region is from 0° to 85°. This rule applies likewise for the I_P– trace.

The limitation of this region is to prevent the current-carrying trace from contributing any stray field that can cause error on the IC output. When the current traces connected to I_P are outside this region, they must be treated as discussed above (Field from a Nearby Current Path).

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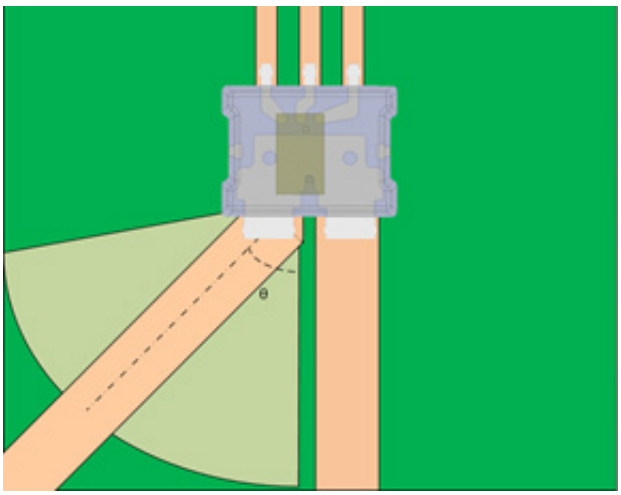

Figure 4: ACS781 Current Trace Approach – the desired range of the angle θ is from 0° to 85°

ENCROACHMENT UNDER THE IC

In the LR package, the encroachment of the current-carrying trace under the device changes the path of the current flowing through the I_P bus. This can cause a change in the coupling factor of the I_P bus to the IC and can significantly reduce device performance. Using ANSYS Maxwell Electromagnetic Suites, the current density and magnetic field generated from the current flow were simulated. In Figure 5, there are results from two different simulations. The first is the case where the current trace leading up to the I_P bus terminates at the desired point. The second case is where the current trace encroaches far up the I_P bus. The red arrows in both simulations represent the areas of high current density. In the simulation with no excess overlap, the red areas, and hence the current density, are very different from the simulation with the excess overlap. It was also observed that the field on H1 was larger when there was no excess overlap. This can be observed by the darker shade of blue.

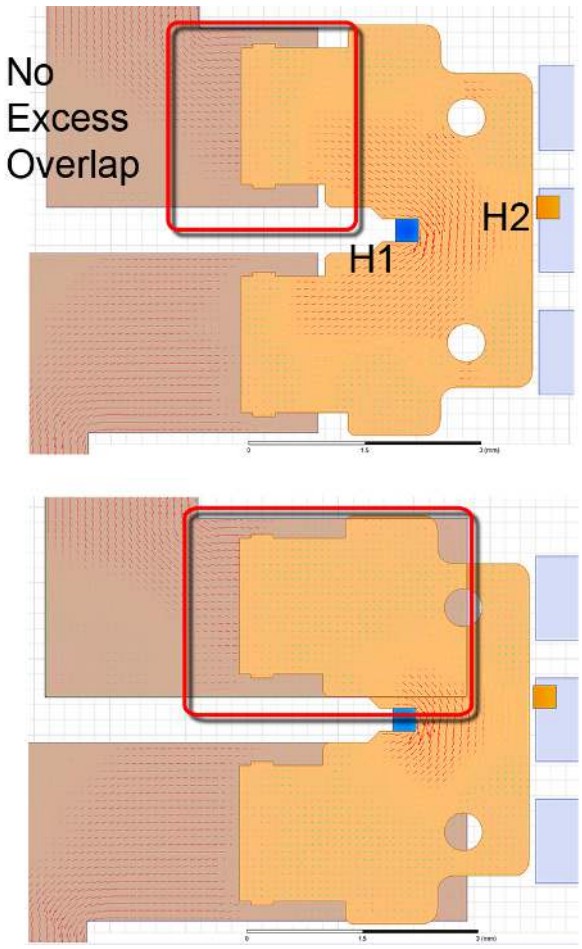

Figure 5: Simulations of ACS781 Leadframe with Different Overlap of the Current Trace and the I_P Bus

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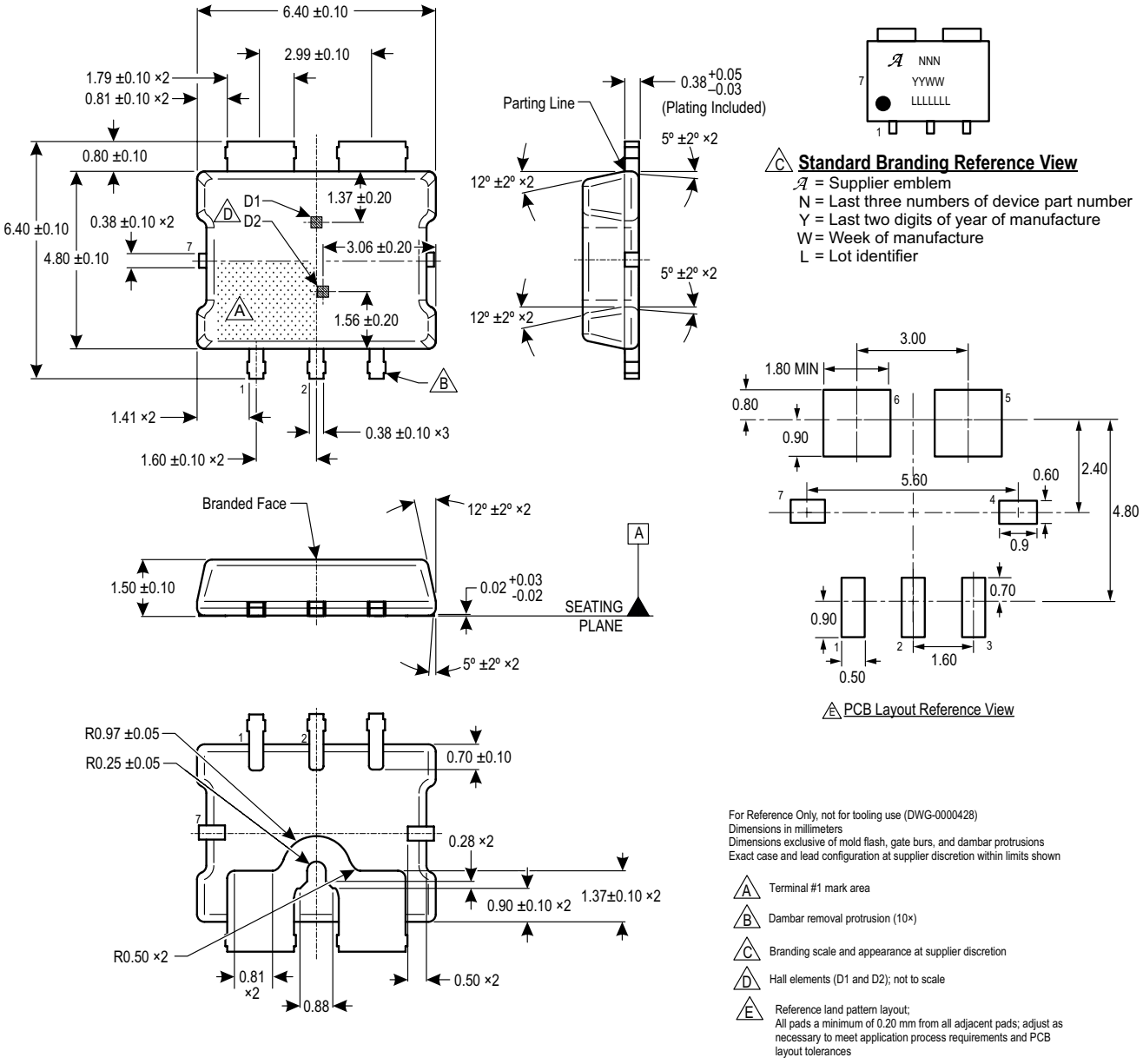
PACKAGE OUTLINE DRAWING



C **Standard Branding Reference View**
𝒜 = Supplier emblem
N = Last three numbers of device part number
Y = Last two digits of year of manufacture
W = Week of manufacture
L = Lot identifier

E PCB Layout Reference View

For Reference Only, not for tooling use (DWG-0000428)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area
B Dambar removal protrusion (10×)
C Branding scale and appearance at supplier discretion
D Hall elements (D1 and D2); not to scale
E Reference land pattern layout;
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

Package LR, 7-Pin PSOF Package

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REVISION HISTORY

Number	Date	Description
–	August 8, 2016	Initial release
1	August 14, 2017	Added Typical Frequency Response charts (p. 14)
2	October 23, 2017	Corrected Primary Conductor Resistance value (p. 5), Nonlinearity test conditions (p. 6-11), and Package Outline Drawing (p. 22)
3	January 30, 2018	Added EEPROM Error Checking and Correction section (page 18)
4	February 7, 2019	Minor editorial updates
5	February 12, 2020	Minor editorial updates
6	May 17, 2021	Removed footnote 2 and updated footnote 6 (pages 6-11)

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