VP0109

P-Channel Enhancement-Mode Vertical DMOS FET

Features

- · Free from Secondary Breakdown
- · Low Power Drive Requirement
- · Ease of Paralleling
- Low C_{ISS} and Fast Switching Speeds
- · Excellent Thermal Stability
- · Integral Source-Drain Diode
- · High Input Impedance and High Gain

Applications

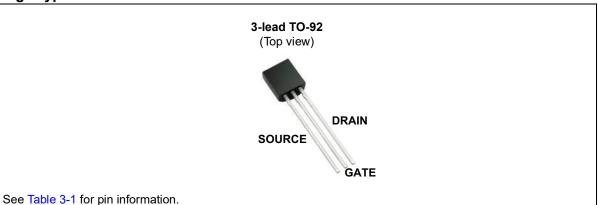
- · Motor Controls
- · Converters, Amplifiers and Switches
- · Power Supply Circuits
- Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

General Description

The VP0109 low-threshold, Enhancement-mode (normally-off) transistor uses a vertical DMOS structure and a well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

Microchip's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Type



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Drain-to-Source Voltage	BV _{DSS}
Drain-to-Gate Voltage	
Gate-to-Source Voltage	200
Operating Ambient Temperature, T _A	
Storage Temperature, T _S	

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: $T_A = 25^{\circ}$ C unless otherwise specified. All DC parameters are 100% tested at 25°C unless otherwise stated. Pulse test: 300 µs pulse, 2% duty cycle

Parameter	Sym.	Min.	Тур.	Max.	Unit	Conditions			
Drain-to-Source Breakdown Voltage	BV _{DSS}	-90	_	_	V	$V_{GS} = 0V$, $I_D = -1$ mA			
Gate Threshold Voltage	V _{GS(th)}	-1.5	_	-3.5	٧	$V_{GS} = V_{DS}$, $I_D = -1$ mA			
Change in V _{GS(th)} with Temperature	$\Delta V_{GS(th)}$	_	5.8	6.5	mV/°C	$V_{GS} = V_{DS}$, $I_D = -1$ mA (Note 1)			
Gate Body Leakage Current	I _{GSS}	_	-1	-100	nA	V_{GS} = ±20V, V_{DS} = 0V			
		_	l	-10	μΑ	V _{GS} = 0V, V _{DS} = Maximum rating			
Zero-Gate Voltage Drain Current	I _{DSS}		l	-1	mA	V_{DS} = 0.8 Maximum rating, V_{GS} = 0V, T_A = 125°C (Note 1)			
On-State Drain Current	l	-0.15	-0.25	_	Α	$V_{GS} = -5V, V_{DS} = -25V$			
On-State Drain Gunent	I _{D(ON)}	-0.5	-1.2	_	Α	$V_{GS} = -10V, V_{DS} = -25V$			
Static Drain-to-Source On-State Resistance	D	_	11	15	Ω	$V_{GS} = -5V$, $I_{D} = -100 \text{ mA}$			
Static Diani-to-Source Off-State Resistance	R _{DS(ON)}	_	6	8	Ω	$V_{GS} = -10V$, $I_{D} = -500$ mA			
Change in R _{DS(ON)} with Temperature	$\Delta R_{DS(ON)}$	_	0.55	1	%/°C	$V_{GS} = -10V$, $I_{D} = -500$ mA (Note 1)			

Note 1: Specification is obtained by characterization and is not 100% tested.

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: T _A = 25°C unless otherwise specified. All AC parameters are not 100% sample tested.									
Parameter	Sym.	Min.	Тур.	Max.	Unit	Conditions			
Forward Transconductance	G _{FS}	150	190	_	mmho	$V_{DS} = -25V$, $I_{D} = -500$ mA			
Input Capacitance	C _{ISS}	_	45	60	pF	$V_{GS} = 0V$,			
Common-Source Output Capacitance		_	22	30	pF	$V_{DS} = -25V$,			
Reverse Transfer Capacitance	C _{RSS}	_	3	8	pF	f = 1 MHz			
Turn-On Delay Time	t _{d(ON)}	_	4	6	ns				
Rise Time	t _r	_	3	10	ns	$V_{DD} = -25V$,			
Turn-Off Delay Time		_	8	12	ns	I_D –500 mA, R_{GEN} = 25 Ω			
Fall Time		_	4	10	ns	GEN			
DIODE PARAMETER									
Diode Forward Voltage Drop	V _{SD}	_	-1.2	-2	V	V _{GS} = 0V, I _{SD} = -1A (Note 1)			
Reverse Recovery Time	t _{rr}	_	400	_	ns	$V_{GS} = 0V, I_{SD} = -1A$			

Note 1: Unless otherwise stated, all DC parameters are 100% tested at 25°C. Pulse test: 300 μs pulse, 2% duty cycle

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Тур.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T _A	-55	_	+150	°C	
Storage Temperature	T _S	-55	_	+150	°C	
PACKAGE THERMAL RESISTANCE						
3-lead TO-92	$\theta_{\sf JA}$	_	132	_	°C/W	

THERMAL CHARACTERISTICS

Package	I _D (Note 1) (Continuous) (mA)	I _D (Pulsed) (mA)	Power Dissipation at T _A = 25°C (W)	I _{DR} (Note 1) (mA)	I _{DRM} (mA)
3-lead TO-92	-250	-800	1	-250	-800

Note 1: I_D (continuous) is limited by maximum rated T_J .

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

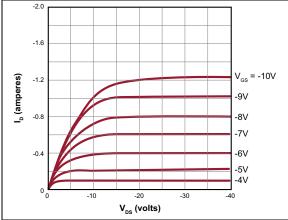


FIGURE 2-1: Output Characteristics.

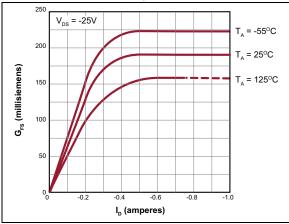


FIGURE 2-2: Transconductance vs. Drain

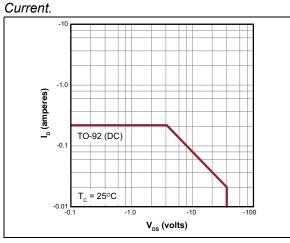


FIGURE 2-3: Maximum Rated Safe Operating Area.

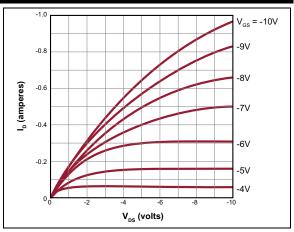


FIGURE 2-4: Saturation Characteristics.

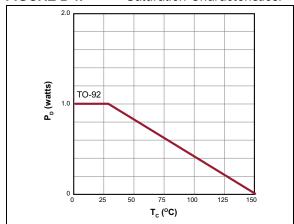


FIGURE 2-5: Power Dissipation vs. Case Temperature.

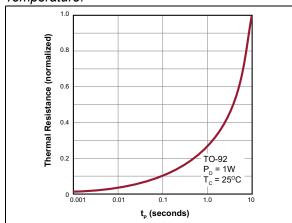


FIGURE 2-6: Thermal Response Characteristics.

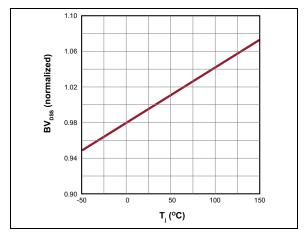


FIGURE 2-7: BV_{DSS} Variation with Temperature.

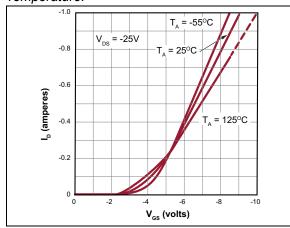


FIGURE 2-8: Transfer Characteristics.

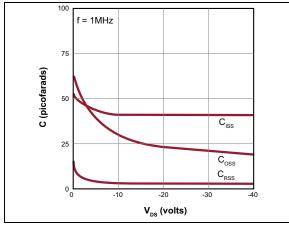


FIGURE 2-9: Capacitance vs. Drain-to-Source Voltage.

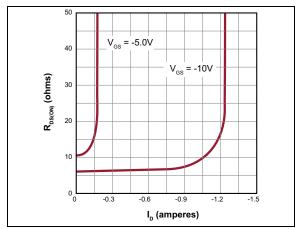


FIGURE 2-10: On-Resistance vs. Drain Current.

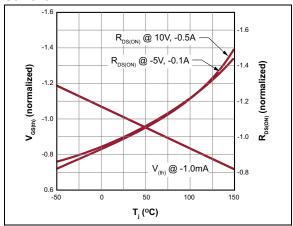


FIGURE 2-11: $V_{(th)}$ and R_{DS} Variation with Temperature.

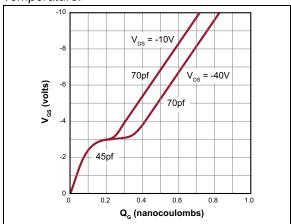


FIGURE 2-12: Gate Drive Dynamic Characteristics.

VP0109

3.0 PIN DESCRIPTION

The details on the pins of VP0109 are listed in Table 3-1. Refer to **Package Type** for the location of pins.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description					
1	Source	Source					
2	Gate	Gate					
3	Drain	Drain					

4.0 FUNCTIONAL DESCRIPTION

Figure 4-1 illustrates the switching waveforms and test circuit for VP0109.

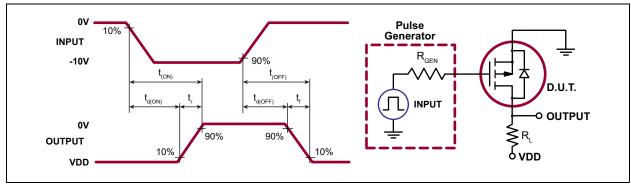


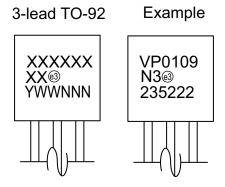
FIGURE 4-1: Switching Waveforms and Test Circuit.

TABLE 4-1: PRODUCT SUMMARY

BV _{DSS} /BV _{DGS} (V)	R _{DS(ON)} (Maximum) (Ω)	I _{D(ON)} (Minimum) (mA)
-90	8	-500

5.0 PACKAGING INFORMATION

5.1 Package Marking Information

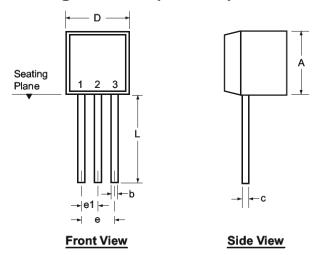


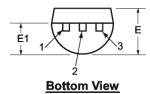
Legend: XX...X Product Code or Customer-specific information
Y Year code (last digit of calendar year)
YY Year code (last 2 digits of calendar year)
WW Week code (week of January 1 is week '01')
NNN Alphanumeric traceability code

(e3 Pb-free JEDEC® designator for Matte Tin (Sn)
* This package is Pb-free. The Pb-free JEDEC designator (e3)
can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

3-Lead TO-92 Package Outline (L/LL/N3)





Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Symb	ol	Α	b	С	D	Е	E1	е	e1	L
	MIN	.170	.014 [†]	.014 [†]	.175	.125	.080	.095	.045	.500
Dimensions (inches)	NOM	-	-	-	-	-	-	-	-	-
(51100)	MAX	.210	.022 [†]	.022†	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.
* This dimension is not specified in the JEDEC drawing.
† This dimension differs from the JEDEC drawing.

Drawings not to scale.



NOTES:

APPENDIX A: REVISION HISTORY

Revision A (April 2022)

- Converted Supertex Doc# DSFP-VP0109 to Microchip DS20006001A
- Changed the package marking format
- Removed the 3-lead TO-92 N3 P002, P003, P005, P013, and P014 media types
- Added some sections to comply with the standard Microchip format
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	<u> </u>		- X - X	Example:	
Device	Packa Optio		Environmental Media Type	a) VP0109N3-G:	P-Channel Enhancement- Mode, Vertical DMOS FET, 3-lead TO-92, 1000/Bag
Device:	VP0109	=	P-Channel Enhancement-Mode Vertical DMOS FET		
Package:	N3	=	3-lead TO-92		
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package		
Media Type:	(blank)	=	1000/Bag for an N3 Package		
1					

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