High-Accuracy Hall-Effect Transmission Speed Sensor IC

FEATURES AND BENEFITS

- **Differential Hall-effect sensor** measures ring magnets and ferrous targets with inherent stray field immunity
- **SolidSpeed Digital Architecture** supports advanced algorithms, maintaining pitch and duty cycle accuracy during dynamic air gap disturbances
- **Integrated solution** includes a capacitor in a single overmolded package
- **ISO 26262:2011 ASIL B** with integrated diagnostics and certified safety design process
- **Two-wire current source output** protocol supporting speed and ASIL error reporting
- **EEPROM** enables traceability throughout product life cycle

PACKAGE:

2-Pin SIP
(suffix UB)

Not to scale

DESCRIPTION

The A19420 is an optimized Hall-effect integrated circuit (IC) that measures the speed of rotating targets. This sensor IC can be used to directly measure ring magnets or be back-biased with a magnet to measure ferrous targets. The package features an integrated capacitor for electromagnetic compatibility (EMC).

The A19420 SolidSpeed Digital Architecture offers intelligent algorithms capable of stable operation during sudden and dynamic air gap movements. The sophisticated digital controller provides highly accurate speed detection ideal for transmission applications. In addition, the A19420 differential sensing offers inherent rejection of interfering common-mode magnetic fields.

The A19420 was developed in accordance with ISO 26262:2011 as a hardware safety element out of context with ASIL B capability for use in automotive safety-related systems when integrated and used in the manner prescribed in the applicable safety manual and datasheet.
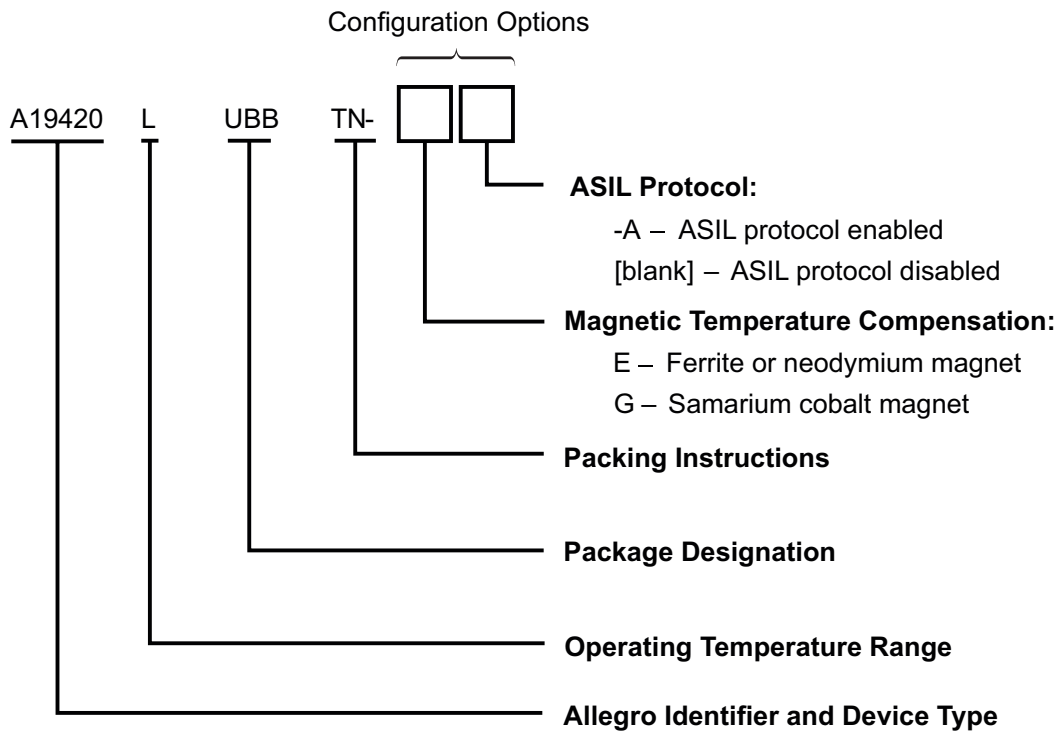
The A19420 is provided in a 2-pin SIP package (suffix UB) that is lead (Pb) free, with tin leadframe plating. The UB package includes an IC and capacitor integrated into a single overmolded package, with an additional molded lead-stabilizing bar for robust shipping and ease of assembly.

Functional Block Diagram
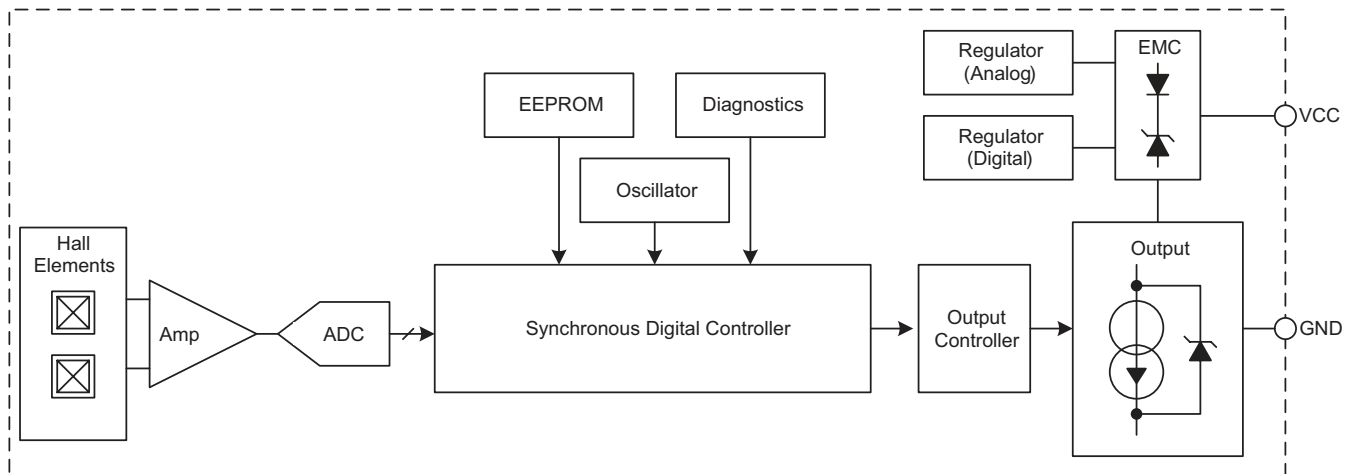
SELECTION GUIDE

| Part Number	Packing
A19420LUBBTN-E	Tape and reel, 4000 pieces per 13-inch reel
A19420LUBBTN-G	Tape and reel, 4000 pieces per 13-inch reel

Configuration Options

A19420   L   UBB   TN-☐☐

ASIL Protocol:

    -A – ASIL protocol enabled

    [blank] – ASIL protocol disabled

Magnetic Temperature Compensation:

    E – Ferrite or neodymium magnet

    G – Samarium cobalt magnet

Packing Instructions

Package Designation

Operating Temperature Range

Allegro Identifier and Device Type

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{CC}	Refer to Power Derating section	28	V
Reverse Supply Voltage	V_{RCC}		−18	V
Operating Ambient Temperature	T_A		−40 to 150	°C
Maximum Junction Temperature	$T_{J(max)}$		165	°C
Storage Temperature	T_{stg}		−65 to 170	°C

INTERNAL DISCRETE CAPACITOR RATINGS

Characteristic	Symbol	Test Conditions	Value (Typ.)	Unit
Nominal Capacitance	C_{SUPPLY}	Connected between pin 1 and pin 2 (refer to Figure 1)	10	nF

PINOUT DIAGRAM AND TERMINAL LIST
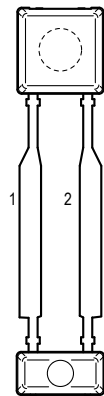
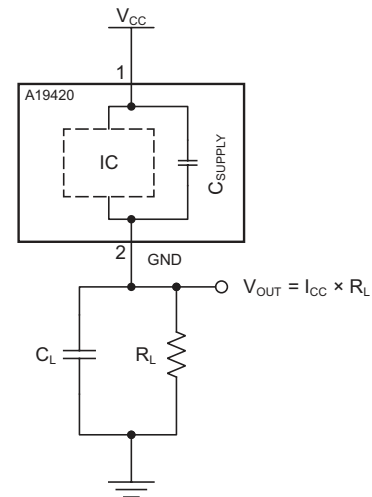
UB Package, 2-Pin SIP Pinout Diagram

Figure 1: Typical Application Circuit

Terminal List Table

Name	Number	Function
VCC	1	Supply Voltage
GND	2	Ground

OPERATING CHARACTERISTICS: Valid throughout full operating and temperature ranges, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
GENERAL						
Supply Voltage [2]	V_{CC}	Operating, $T_J < T_{J(max)}$, voltage across pin 1 and pin 2; does not include voltage across R_L	4	–	24	V
Undervoltage Lockout	$V_{CC(UV)}$	V_{CC} 0 V → 5 V or 5 V → 0 V	–	3.6	3.95	V
Reverse Supply Current [3]	I_{RCC}	$V_{CC} = V_{RCC(max)}$	–10	–	–	mA
Supply Current	$I_{CC(LOW)}$	Low-current state	5.9	7	8	mA
	$I_{CC(HIGH)}$	High-current state	12	14	16	mA
	$I_{CC(HIGH)}$ / $I_{CC(LOW)}$	Ratio of high current to low current (isothermal)	1.9	–	–	–
ASIL Safety Current	I_{RESET}	See Figure 9	1.5	–	3.9	mA
PROTECTION CIRCUITS						
Supply Zener Clamp Voltage	$V_{Zsupply}$	I_{CC} = 19 mA, T_A = 25°C	28	–	–	V
POWER-ON CHARACTERISTICS						
Power-On State	POS	$V_{CC} > V_{CC(min)}$, as connected in Figure 1		$I_{CC(LOW)}$		mA
Power-On Time [4]	t_{PO}	$V_{CC} > V_{CC(min)}$, time to when device is ready to give an output transition	–	–	1	ms
CALIBRATION CHARACTERISTICS						
First Output Edge	–	Amount of target rotation (constant direction) following power-on time until first electrical output transition; see Figure 3	–	–	1.5 × T_{CYCLE}	–
OUTPUT CHARACTERISTICS [5]						
Output Rise Time	t_r	Voltage measured at pin 2, R_L = 100 Ω, C_L = 10 pF, see Figure 1; measured between 90% and 10% of the $I_{CC(HIGH)}$ and $I_{CC(LOW)}$ signal transition	0	2	4	µs
Output Fall Time	t_r	Voltage measured at pin 2, R_L = 100 Ω, C_L = 10 pF, see Figure 1; measured between 90% and 10% of the $I_{CC(HIGH)}$ and $I_{CC(LOW)}$ signal transition	0	2	4	µs
Pulse Width, ASIL Warning [5]	$t_{w(ASILwarn)}$	R_L = 100 Ω, C_L = 10 pF, see Figure 1	63	–	121	µs
Pulse Width, ASIL Critical [5]	$t_{w(ASILcrit)}$	R_L = 100 Ω, C_L = 10 pF, see Figure 1	4	–	8	ms
SWITCHPOINT CHARACTERISTICS						
Operate Point	B_{OP}	% of $B_{DIFF(pk-pk)}$	–	70	–	%
Release Point	B_{RP}	% of $B_{DIFF(pk-pk)}$	–	30	–	%

Continued on next page...

[1] Typical values are at T_A = 25°C and V_{CC} = 12 V. Performance may vary for individual units, within the specified maximum and minimum limits.
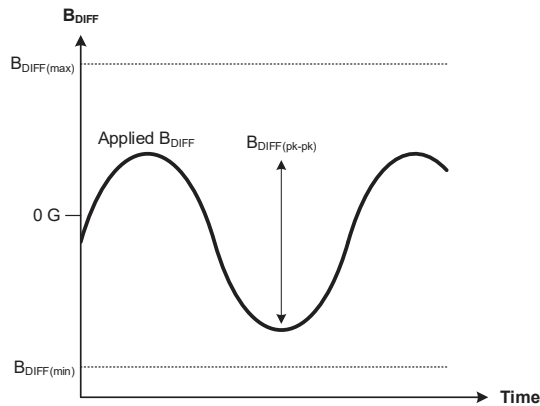[2] Maximum voltage must be adjusted for power dissipation and junction temperature; see representative for Power Derating discussions.
[3] Negative current is defined as conventional current coming out of (sourced from) the specified device terminal.
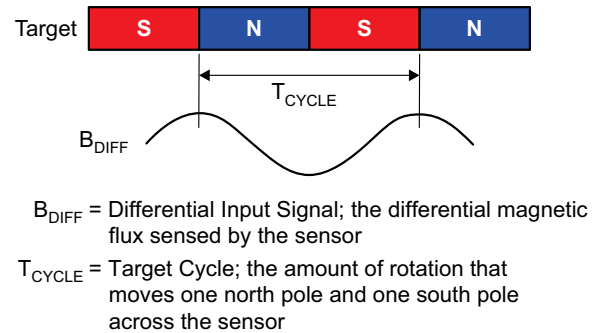[4] Output transients prior to t_{PO} should be ignored.
[5] Measured pulse width will vary on load circuit configurations and thresholds. Pulse width measured at threshold of (I_{RESET} + $I_{CC(LOW)}$) / 2.

OPERATING CHARACTERISTICS (continued): Valid throughout full operating temperature ranges, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
PERFORMANCE CHARACTERISTICS						
Operating Frequency	f_{OP}	Sinusoidal magnetic input signal	–	–	12	kHz
Operating Magnetic Input [6]	$B_{DIFF(pk-pk)}$	Differential peak-to-peak magnetic input signal, see Figure 2	20	–	–	G
Operating Magnetic Input Range [6]	B_{DIFF}	Differential magnetic input range, see Figure 2	–750	–	750	G
Operating Magnetic Input Signal Variation	$\Delta B_{DIFF(pk-pk)}$	Bounded amplitude ratio within T_{WINDOW} [7]; no missed output transitions or flat line condition; see Figure 4 and Figure 5	0.55	–	–	–
Operating Magnetic Input Signal Window	T_{WINDOW}	Rolling window in which $\Delta B_{DIFF(pk-pk)}$ cannot exceed bounded ratio; See Figure 3, Figure 4, and Figure 5	3 × T_{CYCLE}	–	–	–
THERMAL CHARACTERISTICS						
Magnetic Temperature Coefficient [8]	T_C	Based on ferrite and neodymium magnet (-E variant)	–	0.16	–	%/°C
		Based on samarium cobalt magnet (-G variant)	–	0.04	–	%/°C
Package Thermal Resistance [9]	$R_{\theta JA}$	Single-layer PCB with copper limited to solder pads	–	213	–	°C/W

Figure 2: Differential Magnetic Input

B_{DIFF} = Differential Input Signal; the differential magnetic flux sensed by the sensor

T_{CYCLE} = Target Cycle; the amount of rotation that moves one north pole and one south pole across the sensor

Figure 3: Definition of T_{CYCLE}

[6] Differential magnetic field is measured for Channel A as (E1-E2). Magnetic field is measured orthogonally to the front of the package.
[7] Symmetrical signal variation is defined as the largest amplitude ratio from B_n to $B_n + T_{WINDOW}$. Signal variation may occur continuously while B_{DIFF} remains in the operating magnetic range.
[8] Magnets and magnetic encoders decrease in magnetic strength with rising temperature. The device temperature coefficient compensates, to help maintain a consistent air gap over temperature.
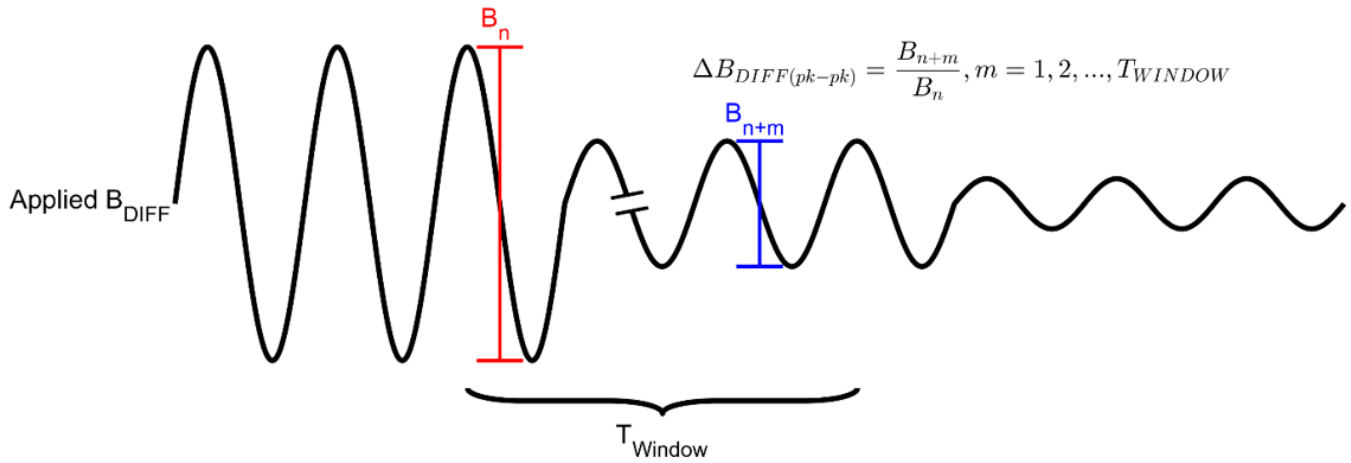[9] Additional thermal information is available on the Allegro website.

$$\Delta B_{DIFF(pk-pk)} = \frac{B_{n+m}}{B_n}, m = 1, 2, ..., T_{WINDOW}$$

Figure 4: Single Period-to-Period Variation

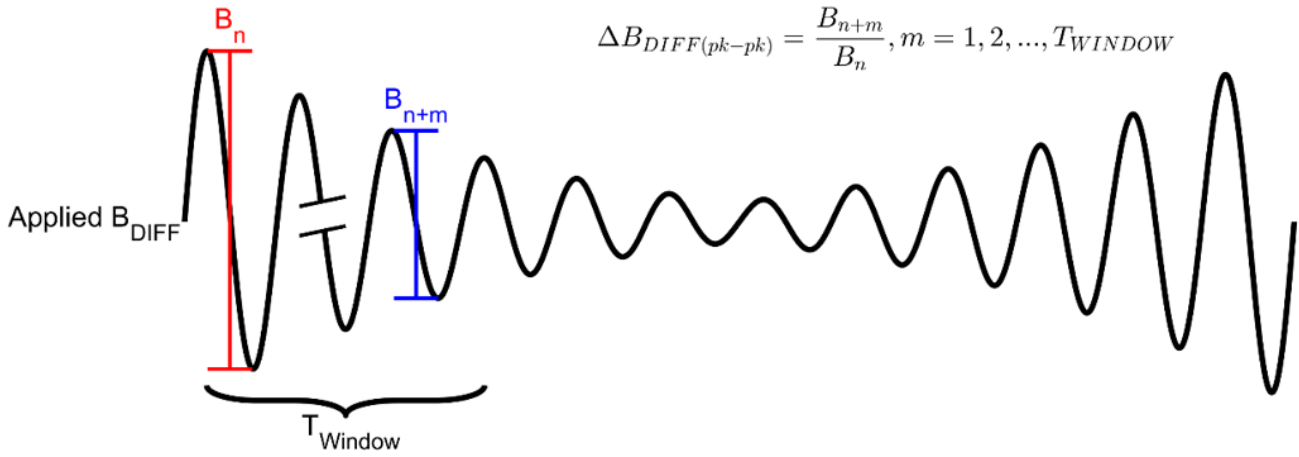$$\Delta B_{DIFF(pk-pk)} = \frac{B_{n+m}}{B_n}, m = 1, 2, ..., T_{WINDOW}$$

Figure 5: Repeated Period-to-Period Variation

FUNCTIONAL DESCRIPTION

The A19420 sensor IC contains a single-chip Hall-effect circuit that supports one differential channel used to convey speed and edge position data over a two-wire digital interface. The sensor is intended for use with ring magnet targets, or, when back-biased with an appropriate magnet, with ferrous targets. The IC detects the peaks of the sensed magnetic signals and sets dynamic thresholds based on these detected signals. Output edges are triggered by B_{DIFF} transitions through the switchpoints.

Figure 6 and Figure 8 demonstrate how the ring magnet, or ferrous target, magnetic systems generate magnetic fields. From generated magnetic fields, the A19420 derives differential magnetic signals using Hall elements, and converts the analog signal into a digital value using a full range analog to digital converter. The low noise analog to digital converter allows for accurate and repeatable edge information.
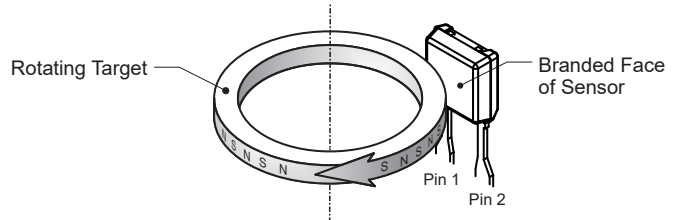

Figure 7: Target Orientation Relative to Device (Ring Magnet Shown)

Mechanical sensor to target relationship is depicted in Figure 7 for a radial type target. For best signal conduction, it is recommended to align the Hall elements center point, refer to Figure 10, with the center of the target diameter and the center of the target thickness.
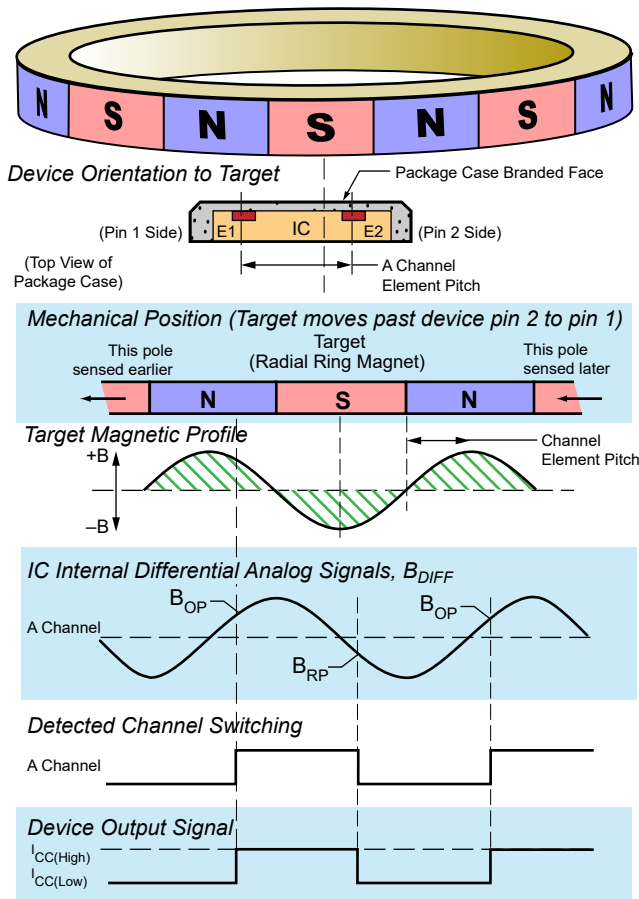

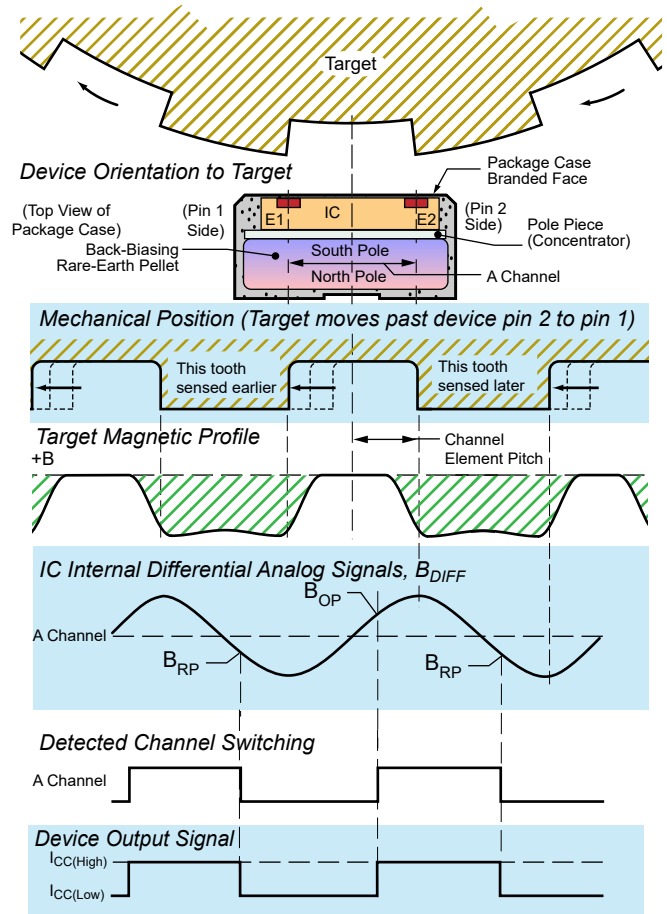**Figure 6: Basic Operation (Ring Magnet)**

Figure 8: Basic Operation (Back-Biased Solution)

7

Safe State Description

The -x-A variant contains diagnostic circuitry that will continuously monitor occurrences of failure defects within the IC. Refer to Figure 9 for the output protocol of the ASIL Safe State after a fault has been detected. Error protocol will result from faults which cause incorrect signal transmission (i.e., too few or too many output edges).

Note: If a fault exists continuously, the device will attempt recovery indefinitely. Refer to the A19420 Safety Manual for additional details on the ASIL Safe State Output Protocol.
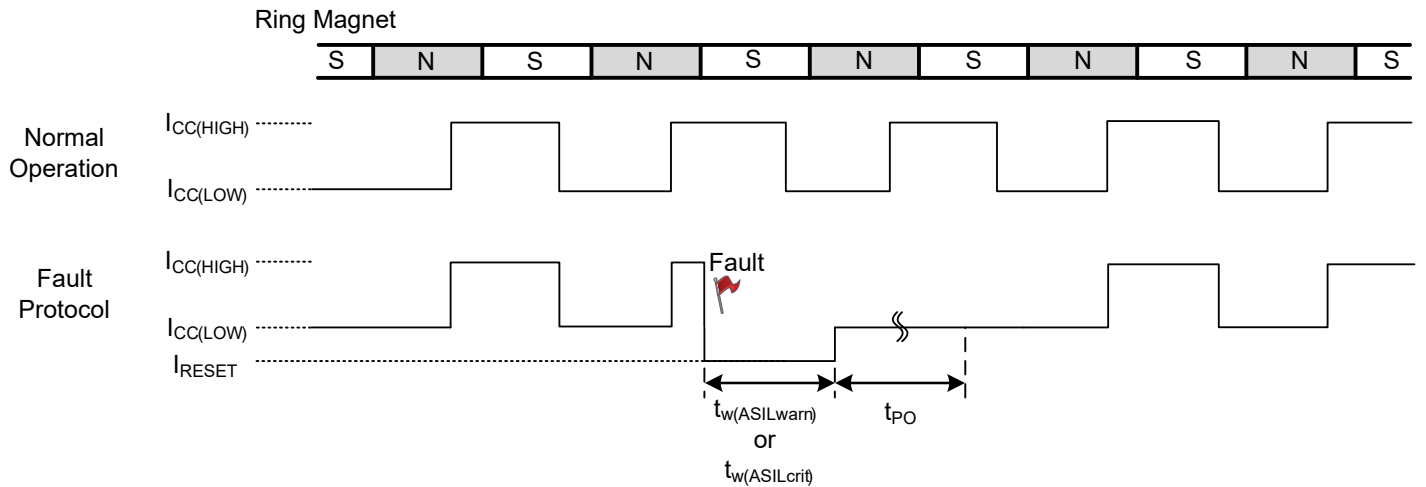
Figure 9: Output Protocol (ASIL Safe State)

POWER DERATING

The device must be operated below the maximum junction temperature of the device ($T_{J(max)}$). Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems website.)

The Package Thermal Resistance ($R_{\theta JA}$) is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity (K) of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case ($R_{\theta JC}$) is a relatively small component of $R_{\theta JA}$. Ambient air temperature (T_A) and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation or P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \qquad (1)$$
$$\Delta T = P_D \times R_{\theta JA} \qquad (2)$$
$$T_J = T_A + \Delta T \qquad (3)$$

For example, given common conditions such as: $T_A = 25°C$, $V_{CC} = 12$ V, $I_{CC(avg)} = 10.5$ mA, and $R_{\theta JA} = 213°C/W$, then:

$$P_D = V_{CC} \times I_{CC(avg)} = 12\,V \times 10.5\,mA = 126\,mW$$
$$\Delta T = P_D \times R_{\theta JA} = 126\,mW \times 213°C/W = 26.8°C$$
$$T_J = T_A + \Delta T = 25°C + 26.8°C = 51.8°C$$

A worst-case estimate, $P_{D(max)}$, represents the maximum allowable power level ($V_{CC(max)}$, $I_{CC(max)}$), without exceeding $T_{J(max)}$, at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{CC} at $T_A = 150°C$, package UB, using 1-layer PCB.

Observe the worst-case ratings for the device, specifically: $R_{\theta JA} = 213°C/W$, $T_{J(max)} = 165°C$, $V_{CC(max)} = 24$ V, and $I_{CC(max)} = 16$ mA.

Calculate the maximum allowable power level ($P_{D(max)}$). First, invert equation 3:

$$\Delta T_{max} = T_{J(max)} - T_A = 165°C - 150°C = 15°C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

$$P_{D(max)} = \Delta T_{max} \div R_{\theta JA} = 15°C \div 213°C/W = 70.4\,mW$$

Finally, invert equation 1 with respect to voltage:

$$V_{CC(est)} = P_{D(max)} \div I_{CC(max)} = 70.4\,mW \div 16\,mA = 4.4\,V$$

The results indicate that, at T_A, the application and device can dissipate adequate amounts of heat at voltages $\leq V_{CC(est)}$.

Compare $V_{CC(est)}$ to $V_{CC(max)}$. If $V_{CC(est)} \leq V_{CC(max)}$, then reliable operation between $V_{CC(est)}$ and $V_{CC(max)}$ requires enhanced $R_{\theta JA}$. If $V_{CC(est)} \geq V_{CC(max)}$, then operation between $V_{CC(est)}$ and $V_{CC(max)}$ is reliable under these conditions.

Power Derating Curve
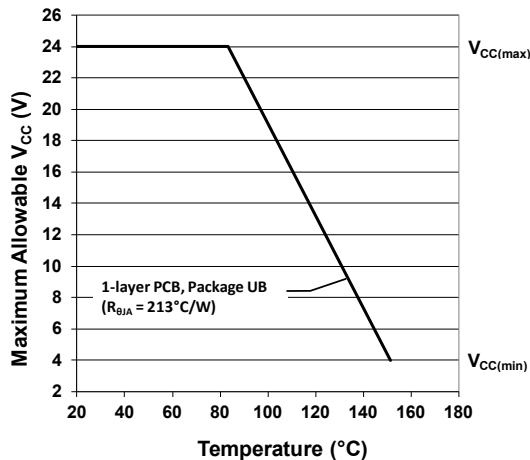
Power Dissipation versus Ambient Temperature
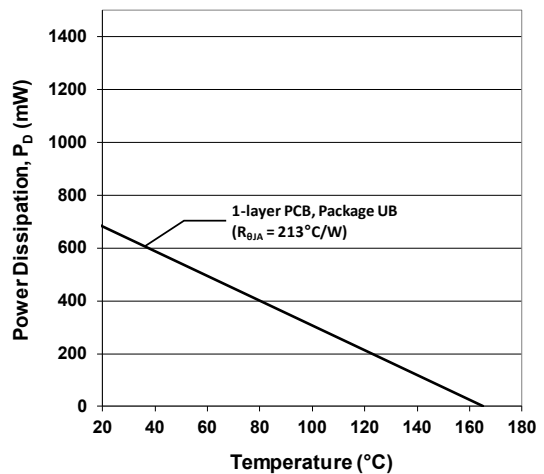
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference DWG-0000408, Rev. 4)
Dimensions in millimeters – NOT TO SCALE
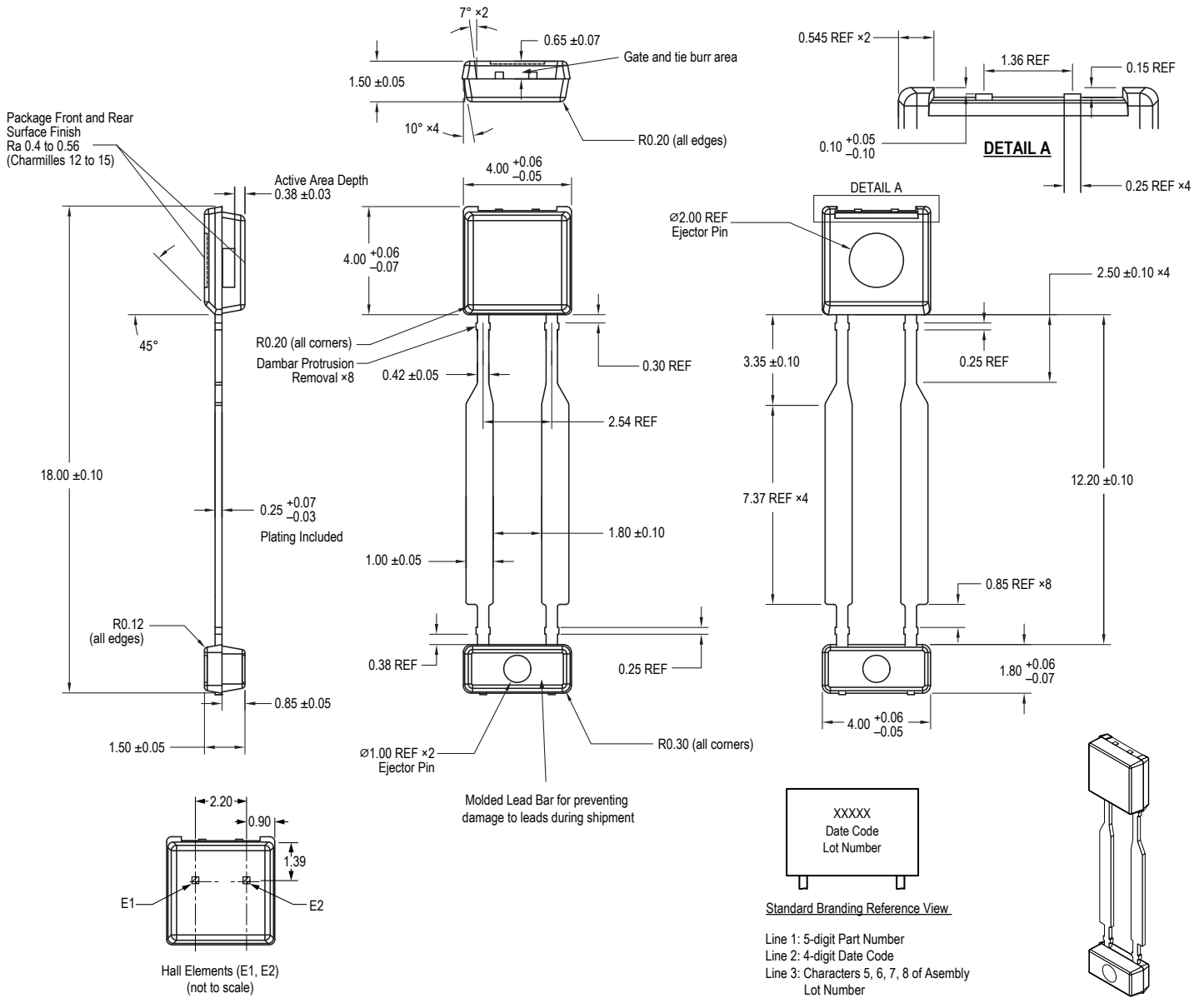Exact case and lead configuration at supplier discretion within limits shown

7° ×2
0.65 ±0.07
Gate and tie burr area
1.50 ±0.05
10° ×4
R0.20 (all edges)

0.545 REF ×2
1.36 REF
0.15 REF
0.10 +0.05 −0.10
DETAIL A
0.25 REF ×4

Package Front and Rear
Surface Finish
Ra 0.4 to 0.56
(Charmilles 12 to 15)

Active Area Depth
0.38 ±0.03

45°

18.00 ±0.10

0.25 +0.07 −0.03
Plating Included

R0.12
(all edges)

0.85 ±0.05

1.50 ±0.05

2.20
0.90
1.39
E1
E2

Hall Elements (E1, E2)
(not to scale)

4.00 +0.06 −0.05
4.00 +0.06 −0.07
R0.20 (all corners)
Dambar Protrusion
Removal ×8
0.42 ±0.05
0.30 REF
2.54 REF
1.80 ±0.10
1.00 ±0.05
0.38 REF
0.25 REF
Ø1.00 REF ×2
Ejector Pin
R0.30 (all corners)

Molded Lead Bar for preventing
damage to leads during shipment

Ø2.00 REF
Ejector Pin
DETAIL A
2.50 ±0.10 ×4
3.35 ±0.10
0.25 REF
7.37 REF ×4
12.20 ±0.10
0.85 REF ×8
1.80 +0.06 −0.07
4.00 +0.06 −0.05

XXXXX
Date Code
Lot Number

Standard Branding Reference View

Line 1: 5-digit Part Number
Line 2: 4-digit Date Code
Line 3: Characters 5, 6, 7, 8 of Asembly
      Lot Number

Branding scale and appearance at supplier discretion

Figure 10: Package UB, 2-Pin SIP

Revision History

Number	Date	Description
–	May 10, 2019	Initial release
1	June 24, 2021	Updated ASIL status (pages 1-2)
2	July 8, 2022	Updated package drawing (page 10)

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