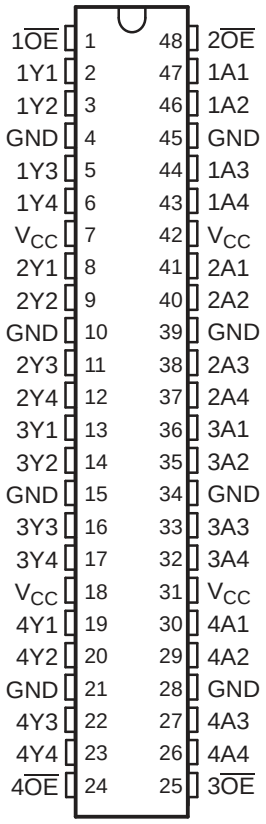
# SN54LVTH162244, SN74LVTH162244
# 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS258N – JUNE 1993 – REVISED NOVEMBER 2006

## FEATURES

- **Members of the Texas Instruments Widebus™ Family**
- **Output Ports Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required**
- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V $V_{CC}$)**
- **Support Unregulated Battery Operation Down to 2.7 V**
- **Typical $V_{OLP}$ (Output Ground Bounce) <0.8 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C**
- **$I_{off}$ and Power-Up 3-State Support Hot Insertion**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Distributed $V_{CC}$ and GND Pins Minimize High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Latch-Up Performance Exceeds 500 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**

**SN54LVTH162244 . . . WD PACKAGE**
**SN74LVTH162244 . . . DGG OR DL PACKAGE**
**(TOP VIEW)**




## DESCRIPTION/ORDERING INFORMATION

### ORDERING INFORMATION

| $T_A$ | PACKAGE(1) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –40°C to 85°C | FBGA – GRD | Reel of 1000 | 74LVTH162244GRDR | LL2244 |
| | FBGA – ZRD (Pb-free) | | 74LVTH162244ZRDR | |
| | SSOP – DL | Tube of 25 | SN74LVTH162244DL | LVTH162244 |
| | | | SN74LVTH162244DLG4 | |
| | | Reel of 1000 | SN74LVTH162244DLR | |
| | | | 74LVTH162244DLRG4 | |
| | TSSOP – DGG | Reel of 2000 | SN74LVTH162244DGGR | LVTH162244 |
| | | | 74LVTH162244DGGRG4 | |
| | | | 74LVTH162244GRE4 | |
| | VFBGA – GQL | Reel of 1000 | SN74LVTH162244KR | LL2244 |
| | VFBGA – ZQL (Pb-free) | | 74LVTH162244ZQLR | |
| –55°C to 125°C | CFP – WD | Tube | SNJ54LVTH162244WD | SNJ54LVTH162244WD |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

## DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The 'LVTH162244 devices are 16-bit buffers and line drivers designed for low-voltage (3.3-V) $V_{CC}$ operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and symmetrical active-low output-enable ($\overline{OE}$) inputs.

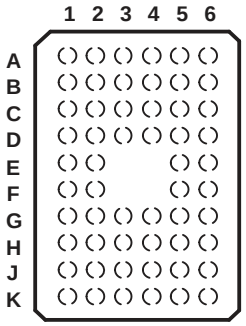
The outputs, which are designed to source or sink up to 12 mA, include equivalent 22-Ω series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When $V_{CC}$ is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using $I_{off}$ and power-up 3-state. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

**GQL OR ZQL PACKAGE**
**(TOP VIEW)**

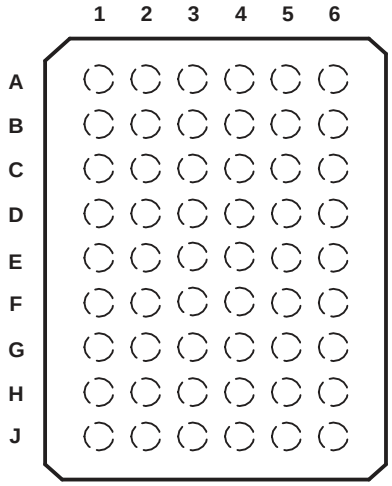



**TERMINAL ASSIGNMENTS(1)**
**(56-Ball GQL/ZQL Package)**

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| **A** | 1$\overline{OE}$ | NC | NC | NC | NC | 2$\overline{OE}$ |
| **B** | 1Y2 | 1Y1 | GND | GND | 1A1 | 1A2 |
| **C** | 1Y4 | 1Y3 | $V_{CC}$ | $V_{CC}$ | 1A3 | 1A4 |
| **D** | 2Y2 | 2Y1 | GND | GND | 2A1 | 2A2 |
| **E** | 2Y4 | 2Y3 | | | 2A3 | 2A4 |
| **F** | 3Y1 | 3Y2 | | | 3A2 | 3A1 |
| **G** | 3Y3 | 3Y4 | GND | GND | 3A4 | 3A3 |
| **H** | 4Y1 | 4Y2 | $V_{CC}$ | $V_{CC}$ | 4A2 | 4A1 |
| **J** | 4Y3 | 4Y4 | GND | GND | 4A4 | 4A3 |
| **K** | 4$\overline{OE}$ | NC | NC | NC | NC | 3$\overline{OE}$ |

(1) NC – No internal connection

**GRD OR ZRD PACKAGE**
**(TOP VIEW)**




**TERMINAL ASSIGNMENTS(1)**
**(54-Ball GRD/ZRD Package)**

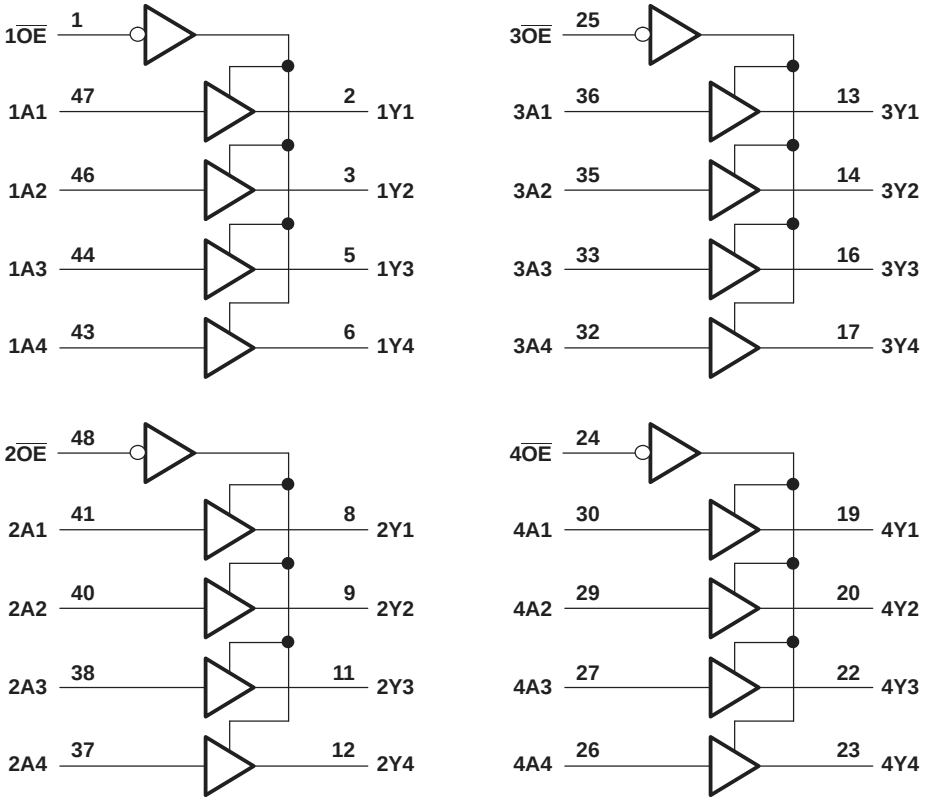
| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| **A** | 1Y1 | NC | 1$\overline{OE}$ | 2$\overline{OE}$ | NC | 1A1 |
| **B** | 1Y3 | 1Y2 | NC | NC | 1A2 | 1A3 |
| **C** | 2Y1 | 1Y4 | $V_{CC}$ | $V_{CC}$ | 1A4 | 2A1 |
| **D** | 2Y3 | 2Y2 | GND | GND | 2A2 | 2A3 |
| **E** | 3Y1 | 2Y4 | GND | GND | 2A4 | 3A1 |
| **F** | 3Y3 | 3Y2 | GND | GND | 3A2 | 3A3 |
| **G** | 4Y1 | 3Y4 | $V_{CC}$ | $V_{CC}$ | 3A4 | 4A1 |
| **H** | 4Y3 | 4Y2 | NC | NC | 4A2 | 4A3 |
| **J** | 4Y4 | NC | 4$\overline{OE}$ | 3$\overline{OE}$ | NC | 4A4 |

(1) NC – No internal connection

**FUNCTION TABLE**
**(EACH 4-BIT BUFFER)**

| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{OE}$ | A | Y |
| L | H | H |
| L | L | L |
| H | X | Z |

## LOGIC DIAGRAM (POSITIVE LOGIC)




Pin numbers shown are for the DGG, DL, and WD packages.

## Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | –0.5 | 4.6 | V |
| $V_I$ | Input voltage range(2) | | –0.5 | 7 | V |
| $V_O$ | Voltage range applied to any output in the high-impedance or power-off state(2) | | –0.5 | 7 | V |
| $V_O$ | Voltage range applied to any output in the high state(2) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_O$ | Current into any output in the low state | | | 30 | mA |
| $I_O$ | Current into any output in the high state(3) | | | 30 | mA |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | –50 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 | | –50 | mA |
| $\theta_{JA}$ | Package thermal impedance(4) | DGG package | | 70 | °C/W |
| | | DL package | | 63 | |
| | | GQL/ZQL package | | 42 | |
| | | GRD/ZRD package | | 36 | |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) This current flows only when the output is in the high state and $V_O > V_{CC}$.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

## Recommended Operating Conditions[1]

| | | | SN54LVTH162244 | | SN74LVTH162244 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2.7 | 3.6 | 2.7 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | | 5.5 | | 5.5 | V |
| $I_{OH}$ | High-level output current | | | –12 | | –12 | mA |
| $I_{OL}$ | Low-level output current | | | 12 | | 12 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | | 10 | | 10 | ns/V |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate | | 200 | | 200 | | µs/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

(1) All unused control inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54LVTH162244 | | | SN74LVTH162244 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP[1] | MAX | MIN | TYP[1] | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 2.7 V, | $I_I$ = –18 mA | | | –1.2 | | | –1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 3 V, | $I_{OH}$ = –12 mA | 2 | | | 2 | | | V |
| $V_{OL}$ | | $V_{CC}$ = 3 V, | $I_{OL}$ = 12 mA | | | 0.8 | | | 0.8 | V |
| $I_I$ | | $V_{CC}$ = 0 or 3.6 V, | $V_I$ = 5.5 V | | | 10 | | | 10 | µA |
| | Control inputs | $V_{CC}$ = 3.6 V, | $V_I$ = $V_{CC}$ or GND | | | ±1 | | | ±1 | |
| | Data inputs | $V_{CC}$ = 3.6 V | $V_I$ = $V_{CC}$ | | | 1 | | | 1 | |
| | | | $V_I$ = 0 | | | –5 | | | –5 | |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O$ = 0 to 4.5 V | | | | | | ±100 | µA |
| $I_{I(hold)}$ | Data inputs | $V_{CC}$ = 3 V | $V_I$ = 0.8 V | 75 | | | 75 | | | µA |
| | | | $V_I$ = 2 V | –75 | | | –75 | | | |
| | | $V_{CC}$ = 3.6 V,[2] | $V_I$ = 0 to 3.6 V | | | | | | 500<br>–750 | |
| $I_{OZH}$ | | $V_{CC}$ = 3.6 V, | $V_O$ = 3 V | | | 5 | | | 5 | µA |
| $I_{OZL}$ | | $V_{CC}$ = 3.6 V, | $V_O$ = 0.5 V | | | –5 | | | –5 | µA |
| $I_{OZPU}$ | | $V_{CC}$ = 0 to 1.5 V, $V_O$ = 0.5 V to 3 V, $\overline{OE}$ = don't care | | | | ±100[3] | | | ±100 | µA |
| $I_{OZPD}$ | | $V_{CC}$ = 1.5 V to 0, $V_O$ = 0.5 V to 3 V, $\overline{OE}$ = don't care | | | | ±100[3] | | | ±100 | µA |
| $I_{CC}$ | | $V_{CC}$ = 3.6 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | Outputs high | | | 0.19 | | | 0.19 | mA |
| | | | Outputs low | | | 5 | | | 5 | |
| | | | Outputs disabled | | | 0.19 | | | 0.19 | |
| $\Delta I_{CC}$[4] | | $V_{CC}$ = 3 V to 3.6 V, One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | | | | 0.2 | | | 0.2 | mA |
| $C_i$ | | $V_I$ = 3 V or 0 | | | 4 | | | 4 | | pF |
| $C_o$ | | $V_O$ = 3 V or 0 | | | 9 | | | 9 | | pF |

(1) All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
(3) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than $V_{CC}$ or GND.

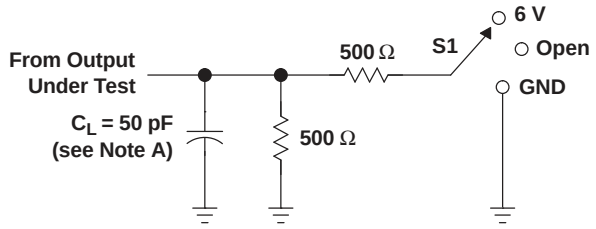
## Switching Characteristics

over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH162244 | | | | SN74LVTH162244 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | | $V_{CC}$ = 2.7 V | |
| | | | MIN | MAX | MIN | MAX | MIN | TYP(1) | MAX | MIN MAX | |
| $t_{PLH}$ | A | Y | 1.1 | 4.6 | | 5.1 | 1.4 | 3.4 | 4 | 4.8 | ns |
| $t_{PHL}$ | | | 1.1 | 3.9 | | 4.5 | 1.2 | 2.9 | 3.6 | 4.1 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | 1.1 | 5.4 | | 6.7 | 1.2 | 3.9 | 5.1 | 6.5 | ns |
| $t_{PZL}$ | | | 1.3 | 4.9 | | 6.1 | 1.4 | 3.8 | 4.5 | 5.8 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | 1.6 | 5.9 | | 6.5 | 2.2 | 4.4 | 5.0 | 5.4 | ns |
| $t_{PLZ}$ | | | 1 | 5.9 | | 5.8 | 2 | 4.2 | 5.0 | 5.4 | |
| $t_{sk(LH)}$ | | | | | | | | | 0.5 | | ns |
| $t_{sk(HL)}$ | | | | | | | | | 0.5 | | |

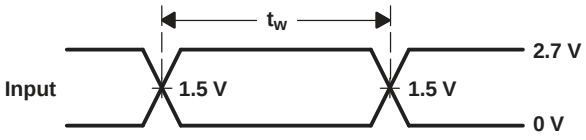
(1) All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.

## PARAMETER MEASUREMENT INFORMATION

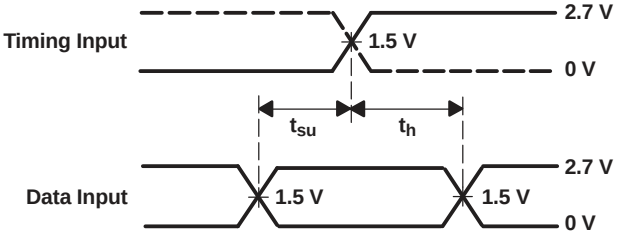



LOAD CIRCUIT

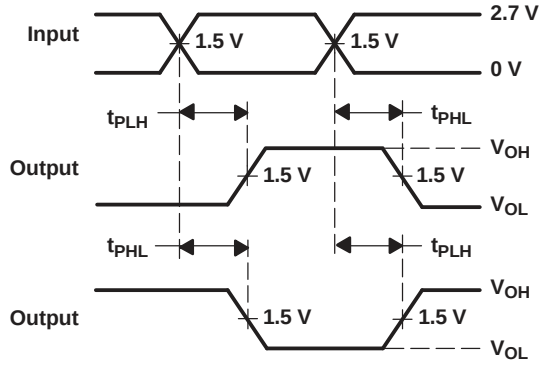
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 6 V |
| $t_{PHZ}/t_{PZH}$ | GND |



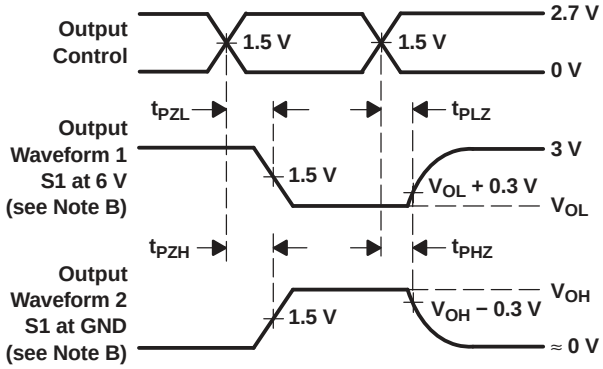

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-9680901QXA | ACTIVE | CFP | WD | 48 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9680901QX A SNJ54LVTH16224 4WD | Samples |
| 5962-9680901VXA | ACTIVE | CFP | WD | 48 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9680901VX A SNV54LVTH16224 4WD | Samples |
| SN74LVTH162244DGGR | ACTIVE | TSSOP | DGG | 48 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVTH162244 | Samples |
| SN74LVTH162244DL | ACTIVE | SSOP | DL | 48 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVTH162244 | Samples |
| SN74LVTH162244DLR | ACTIVE | SSOP | DL | 48 | 1000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVTH162244 | Samples |
| SNJ54LVTH162244WD | ACTIVE | CFP | WD | 48 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9680901QX A SNJ54LVTH16224 4WD | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



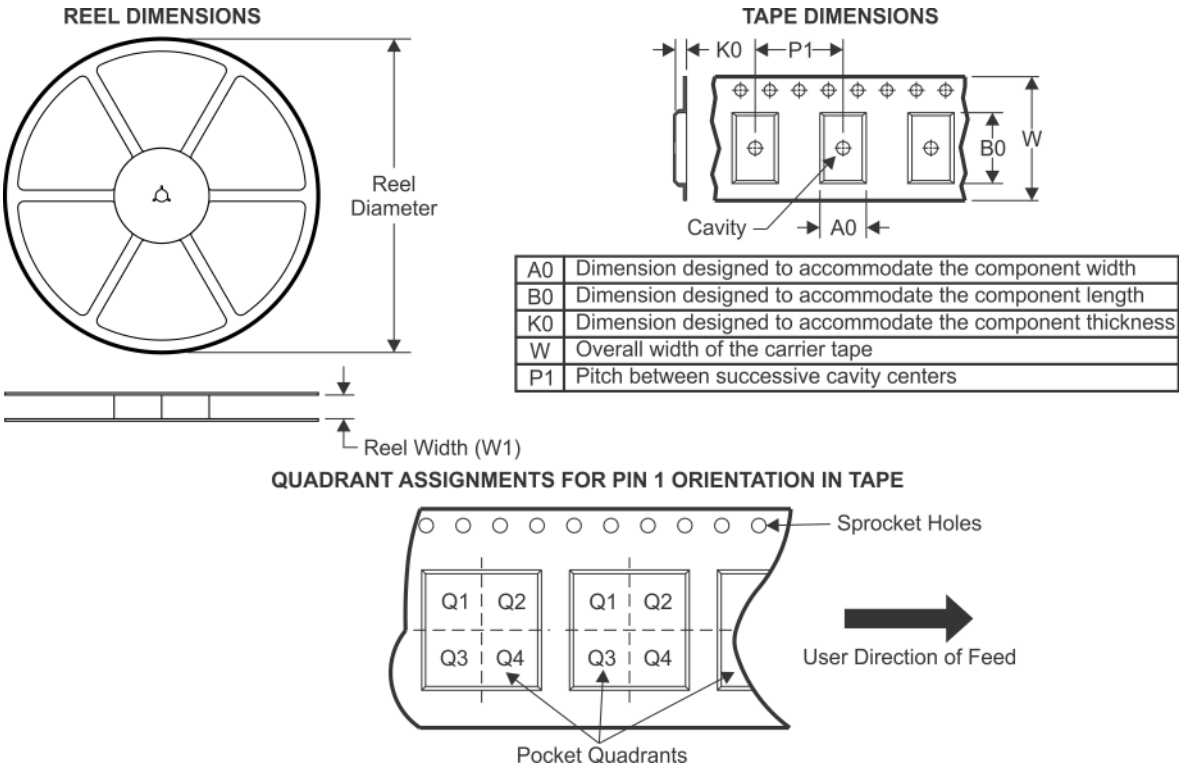
**OTHER QUALIFIED VERSIONS OF SN54LVTH162244, SN54LVTH162244-SP, SN74LVTH162244 :**

- Catalog: SN74LVTH162244, SN54LVTH162244
- Enhanced Product: SN74LVTH162244-EP, SN74LVTH162244-EP
- Military: SN54LVTH162244
- Space: SN54LVTH162244-SP

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## TAPE AND REEL INFORMATION

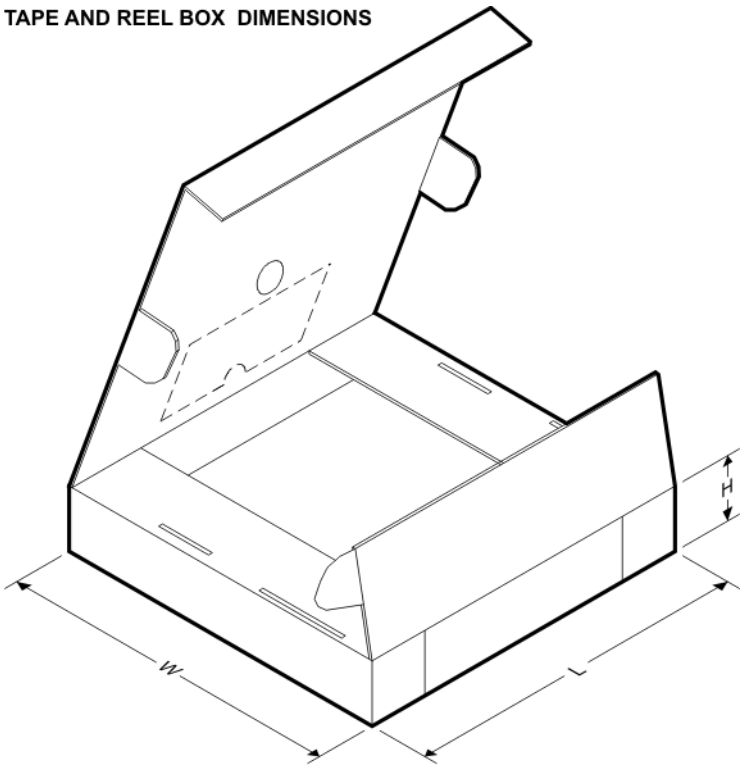



| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVTH162244DGGR | TSSOP | DGG | 48 | 2000 | 330.0 | 24.4 | 8.6 | 13.0 | 1.8 | 12.0 | 24.0 | Q1 |
| SN74LVTH162244DLR | SSOP | DL | 48 | 1000 | 330.0 | 32.4 | 11.35 | 16.2 | 3.1 | 16.0 | 32.0 | Q1 |

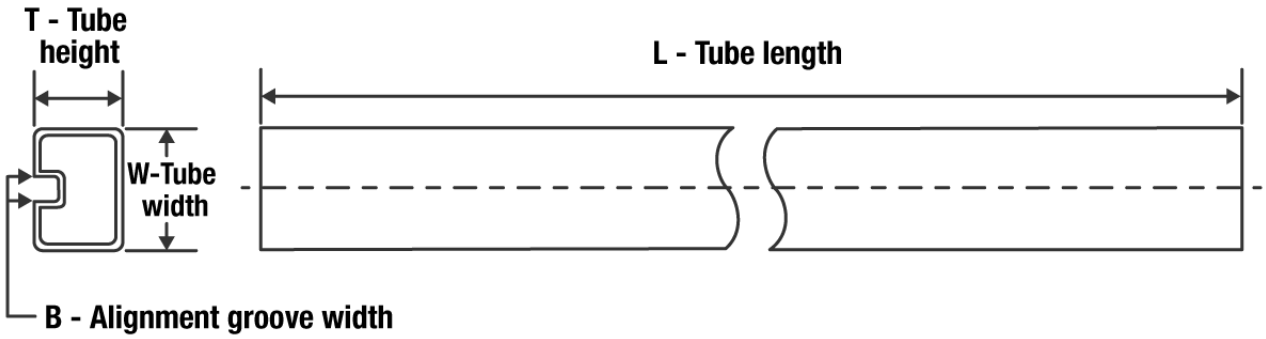
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LVTH162244DGGR | TSSOP | DGG | 48 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LVTH162244DLR | SSOP | DL | 48 | 1000 | 367.0 | 367.0 | 55.0 |

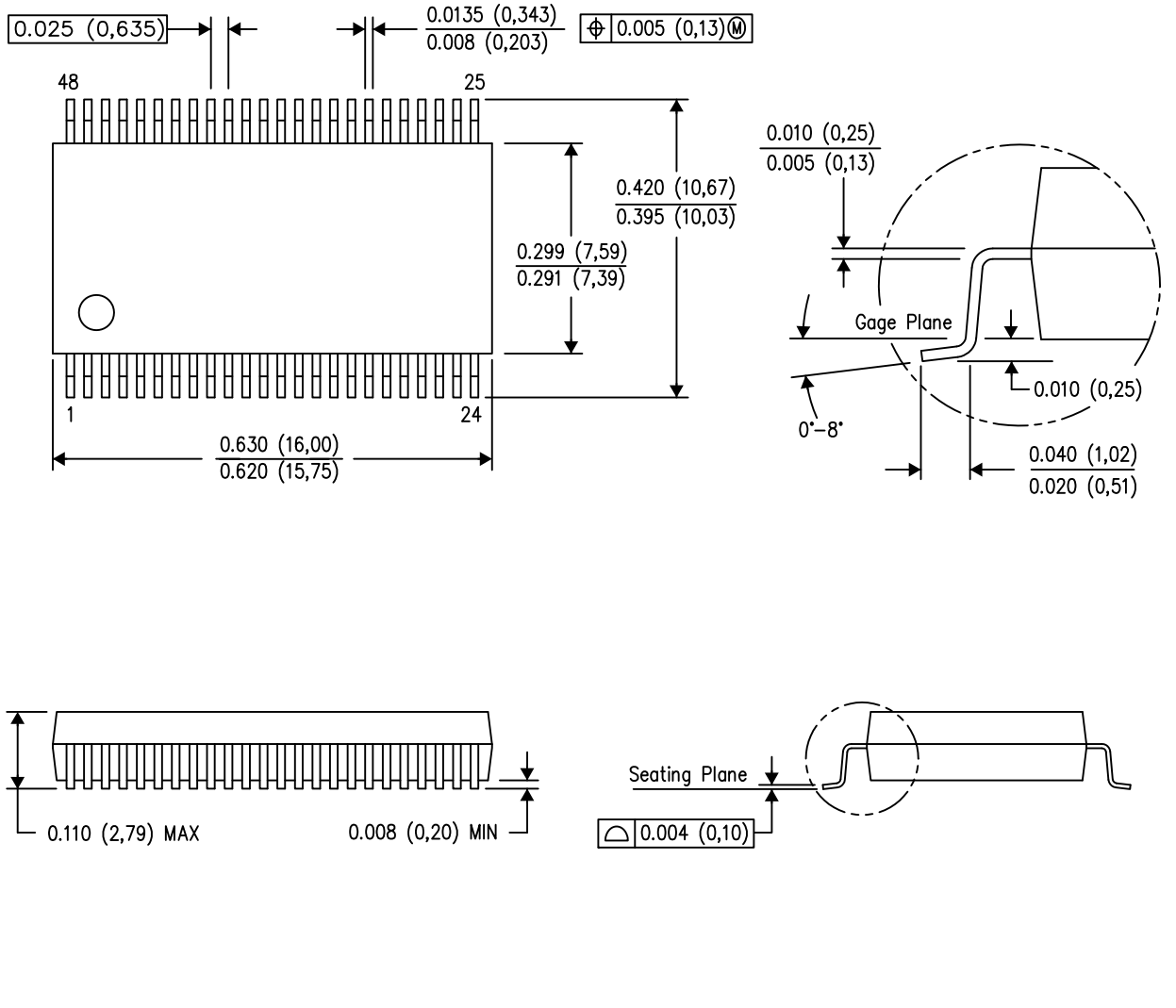
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| SN74LVTH162244DL | DL | SSOP | 48 | 25 | 473.7 | 14.24 | 5110 | 7.87 |

DL (R–PDSO–G48) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

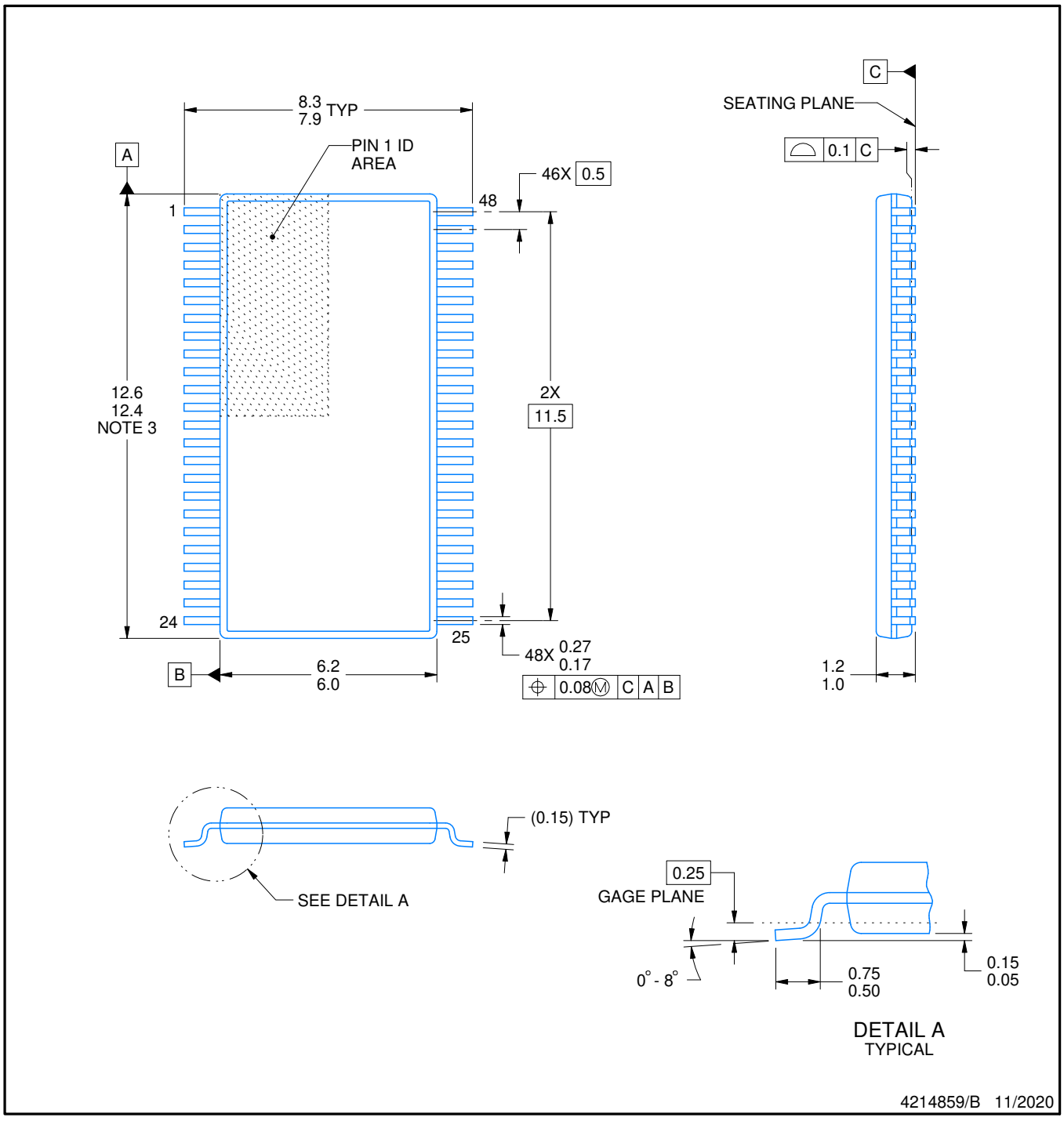
PowerPAD is a trademark of Texas Instruments.

# PACKAGE OUTLINE

## DGG0048A

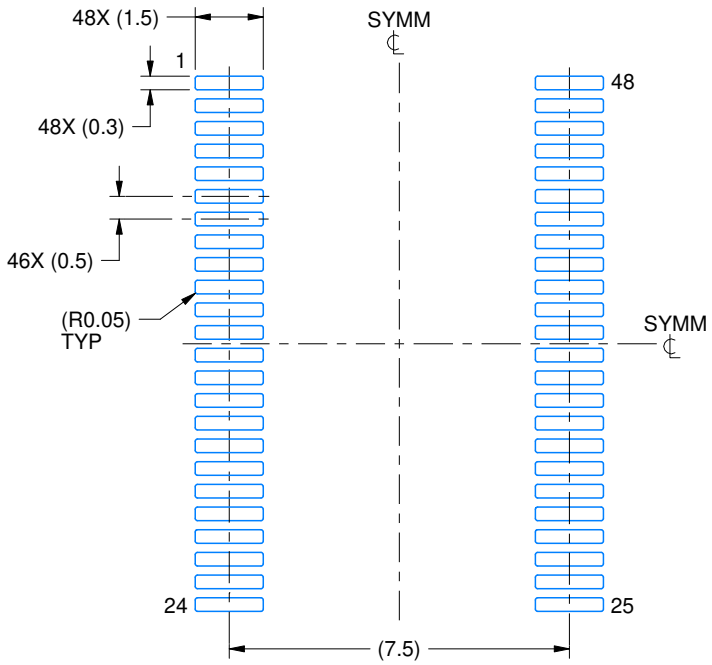
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

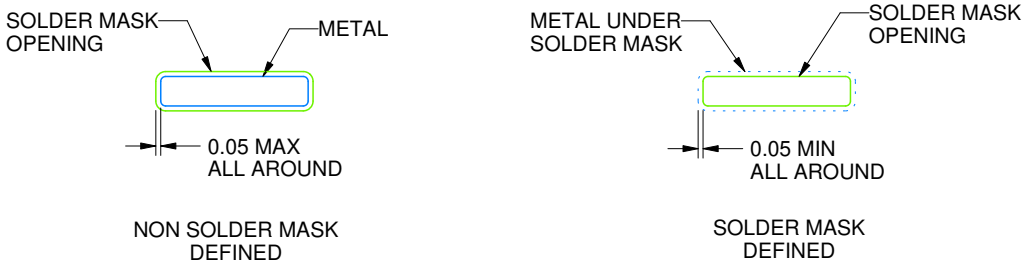



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
SCALE:6X

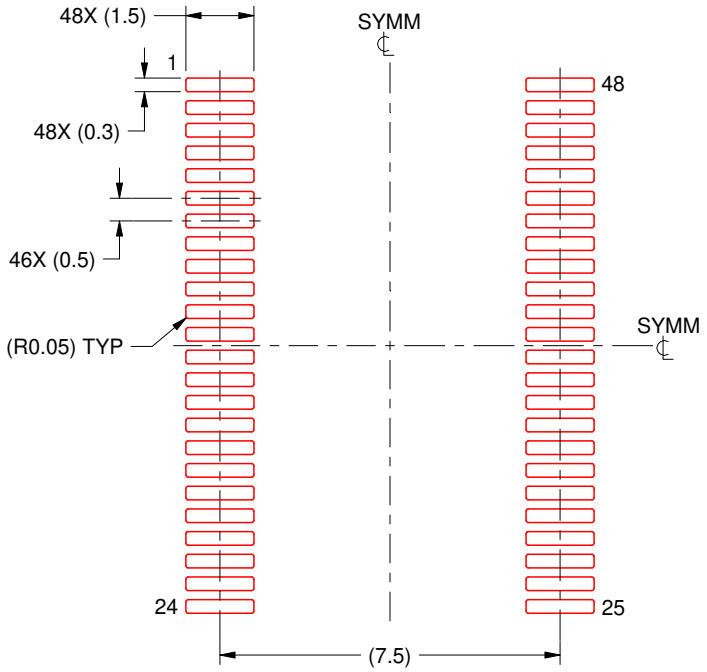



SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4214859/B 11/2020

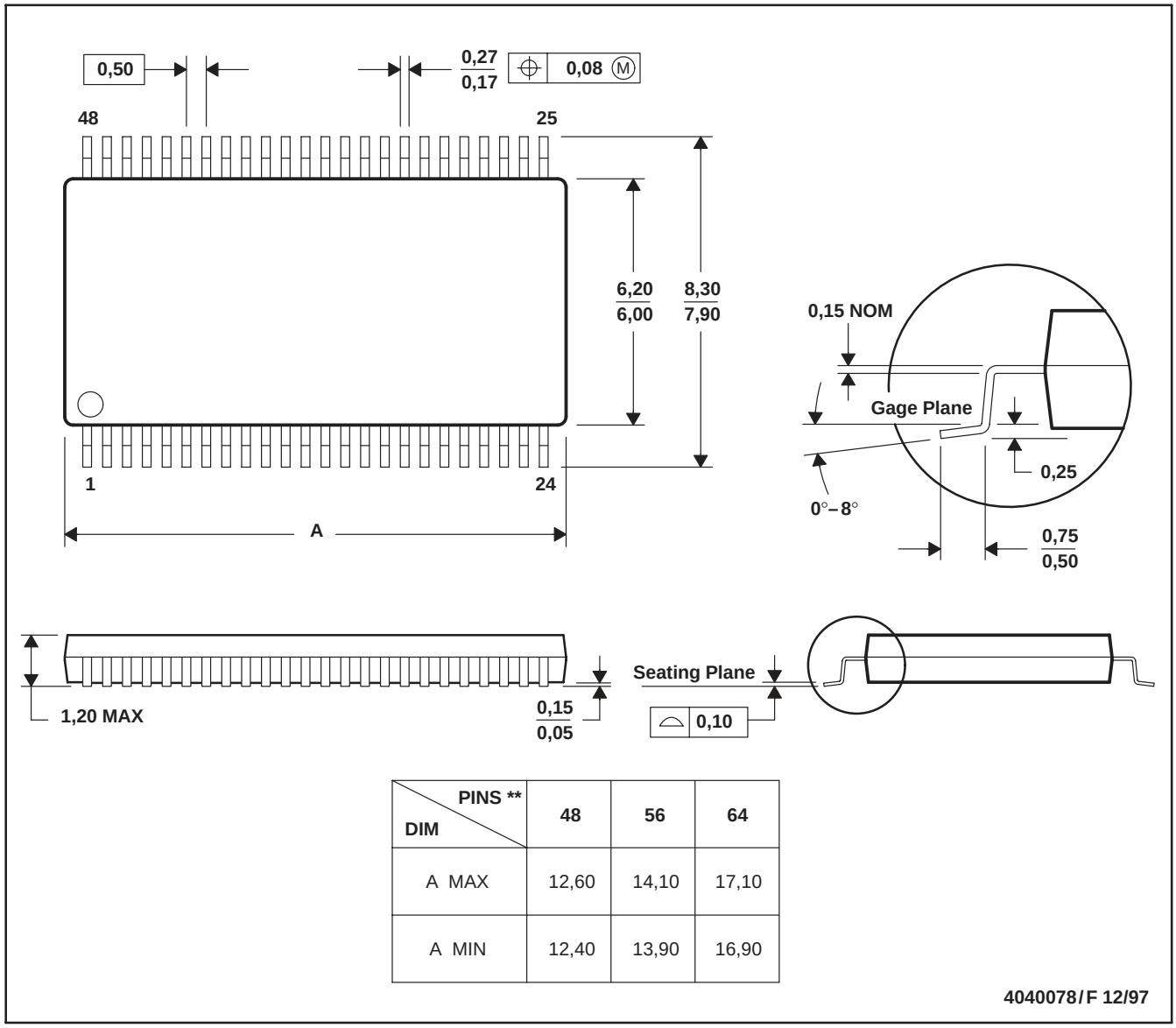
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MTSS003D – JANUARY 1995 – REVISED JANUARY 1998

**DGG (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**48 PINS SHOWN**

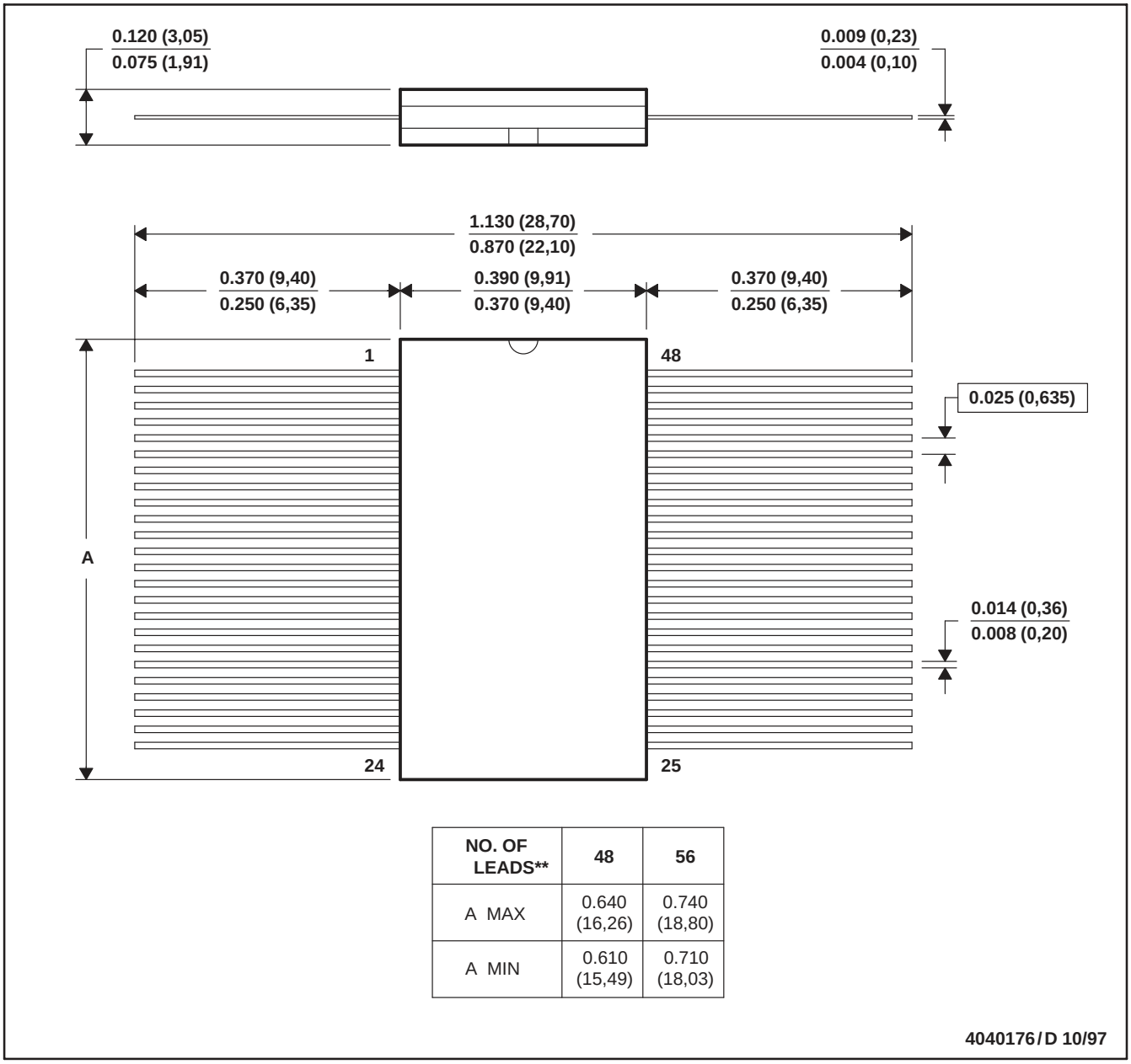



| DIM \ PINS ** | 48 | 56 | 64 |
|---|---|---|---|
| A MAX | 12,60 | 14,10 | 17,10 |
| A MIN | 12,40 | 13,90 | 16,90 |

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

**WD (R-GDFP-F**)** **CERAMIC DUAL FLATPACK**

**48 LEADS SHOWN**




| NO. OF LEADS** | 48 | 56 |
|---|---|---|
| A MAX | 0.640 (16,26) | 0.740 (18,80) |
| A MIN | 0.610 (15,49) | 0.710 (18,03) |

**4040176/D 10/97**

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only
E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA
GDFP1-F56 and JEDEC MO-146AB

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