



RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

Designed for GSM and GSM EDGE base station applications with frequencies from 1930 to 1990 MHz. Suitable for TDMA, CDMA, and multicarrier amplifier applications.

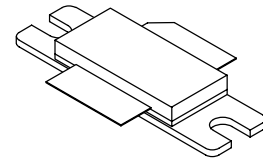
- GSM and GSM EDGE Performance, Full Frequency Band (1930 - 1990 MHz)
Power Gain - 12.5 dB (Typ) @ 85 Watts CW
Efficiency - 50% (Typ) @ 85 Watts CW
- Capable of Handling 5:1 VSWR, @ 26 Vdc, 1960 MHz, 85 Watts CW Output Power

Features

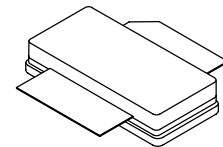
- Internally Matched for Ease of Use
- High Gain, High Efficiency, and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Available with Low Gold Plating Thickness on Leads. L Suffix Indicates 40μ" Nominal.
- RoHS Compliant
- In Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.

MRF18085BLR3
MRF18085BLSR3

1930-1990 MHz, 85 W, 26 V
GSM/GSM EDGE
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 465-06, STYLE 1
NI-780
MRF18085BLR3



CASE 465A-06, STYLE 1
NI-780S
MRF18085BLSR3

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Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V _{GS}	-0.5, +15	Vdc
Total Device Dissipation @ T _C = 25°C Derate above 25°C	P _D	273 1.56	W W/°C
Storage Temperature Range	T _{stg}	- 65 to +150	°C
Case Operating Temperature	T _C	150	°C
Operating Junction Temperature	T _J	200	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value ⁽¹⁾	Unit
Thermal Resistance, Junction to Case	R _{θJC}	0.79	°C/W

1. Refer to AN1955/D, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>.
Select Documentation/Application Notes - AN1955.

Table 3. ESD Protection Characteristics

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M3 (Minimum)

Table 4. Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Drain-Source Breakdown Voltage ($V_{GS} = 0 \text{ Vdc}$, $I_D = 100 \mu\text{Adc}$)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 26 \text{ Vdc}$, $V_{GS} = 0 \text{ Vdc}$)	I_{DSS}	—	—	10	μAdc
Gate-Source Leakage Current ($V_{GS} = 5 \text{ Vdc}$, $V_{DS} = 0 \text{ Vdc}$)	I_{GSS}	—	—	1	μAdc

On Characteristics

Gate Threshold Voltage ($V_{DS} = 10 \text{ Vdc}$, $I_D = 200 \mu\text{Adc}$)	$V_{GS(th)}$	2	—	4	Vdc
Gate Quiescent Voltage ($V_{DS} = 26 \text{ Vdc}$, $I_D = 600 \text{ mAdc}$)	$V_{GS(Q)}$	2.5	3.9	4.5	Vdc
Drain-Source On-Voltage ($V_{GS} = 10 \text{ Vdc}$, $I_D = 2 \text{ Adc}$)	$V_{DS(on)}$	—	0.18	0.21	Vdc

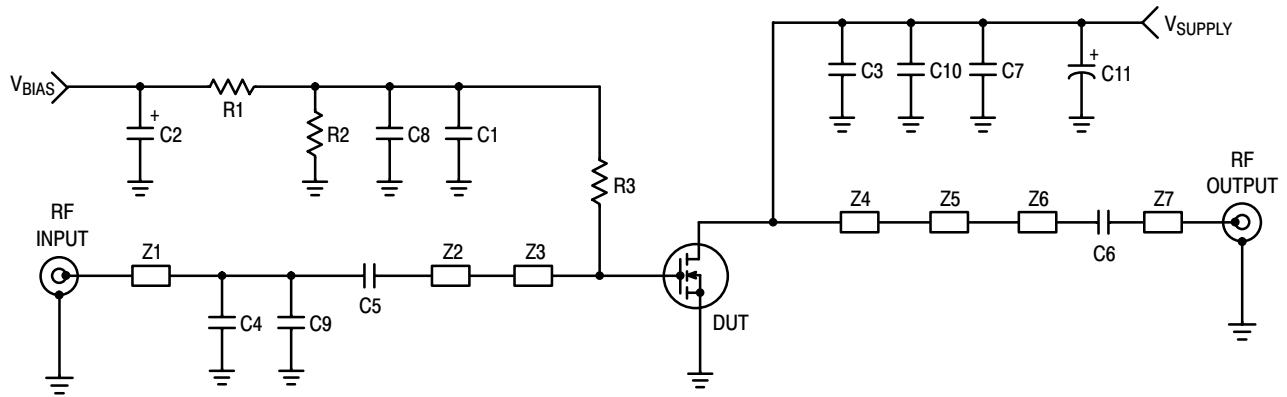
Dynamic Characteristics

Reverse Transfer Capacitance ⁽¹⁾ ($V_{DS} = 26 \text{ Vdc}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$)	C_{rss}	—	3.6	—	pF
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Functional Tests (In Freescale Test Fixture, 50 ohm system)

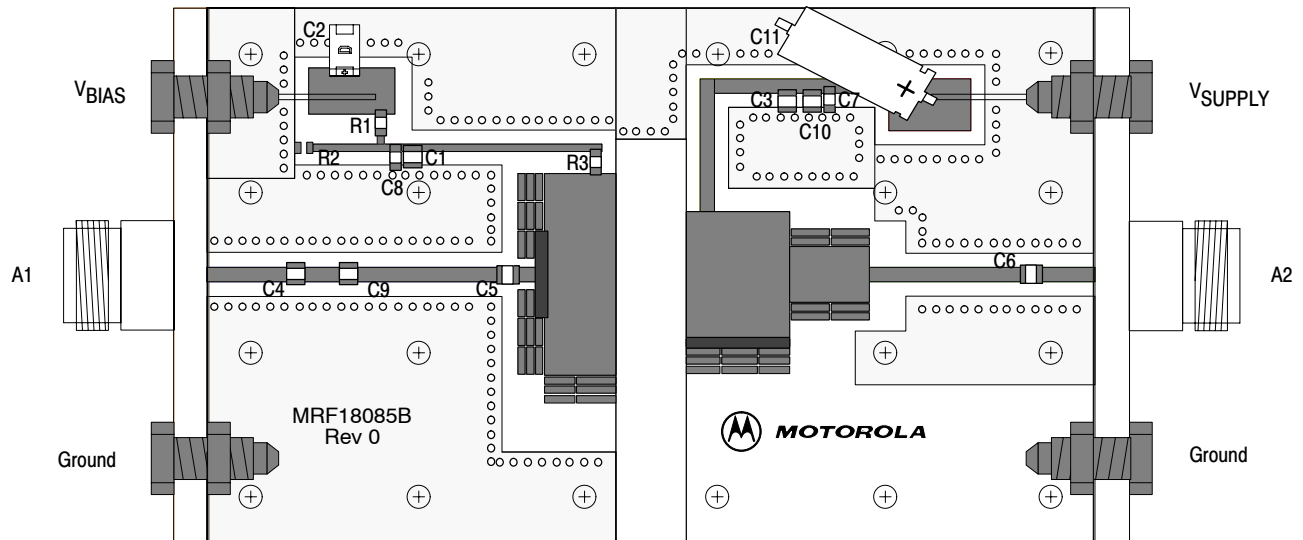
Common-Source Amplifier Power Gain @ 85 W ($V_{DD} = 26 \text{ Vdc}$, $I_{DQ} = 800 \text{ mA}$, $f = 1930 - 1990 \text{ MHz}$)	G_{ps}	11.5	12.5	—	dB
Drain Efficiency @ 85 W ($V_{DD} = 26 \text{ Vdc}$, $I_{DQ} = 800 \text{ mA}$, $f = 1930 - 1990 \text{ MHz}$)	η	46	50	—	%
Input Return Loss @ 85 W ($V_{DD} = 26 \text{ Vdc}$, $I_{DQ} = 800 \text{ mA}$, $f = 1930 - 1990 \text{ MHz}$)	IRL	—	-12	-9	dB
P1 dB Output Power ($V_{DD} = 26 \text{ Vdc}$, $I_{DQ} = 800 \text{ mA}$, $f = 1930 - 1990 \text{ MHz}$)	P1dB	80	90	—	W

1. Part is internally matched both on input and output.



C1, C10	1.0 nF Chip Capacitors, ATC	Z1	1.654" x 0.082" Microstrip
C2	10 μ F, 35 V Tantalum Capacitor	Z2	0.207" x 0.082" Microstrip
C3, C6	10 pF Chip Capacitors, ATC	Z3	0.362" x 1.260" Microstrip
C4	3.3 pF Chip Capacitor, ATC	Z4	0.583" x 0.669" Microstrip
C5	4.7 pF Chip Capacitor, ATC	Z5	0.449" x 0.179" Microstrip
C7, C8	100 nF Chip Capacitors, ACCU-P (1206)	Z6	0.877" x 0.082" Microstrip
C9	3.9 pF Chip Capacitor, ATC	Z7	0.326" x 0.082" Microstrip
C11	470 μ F, 63 V Electrolytic Capacitor	PCB	0.030" Glass Teflon [®] ($\epsilon_r = 2.55$)
R1, R2	1.0 k Ω Chip Resistors (0805)		
R3	2 x 18 k Ω Chip Resistor (1206)		

Figure 1. 1930 - 1990 MHz Test Fixture Schematic



Freescale has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescale Semiconductor signature/logo. PCBs may have either Motorola or Freescale markings during the transition period. These changes will have no impact on form, fit or function of the current product.

Figure 2. 1930 - 1990 MHz Test Fixture Component Layout

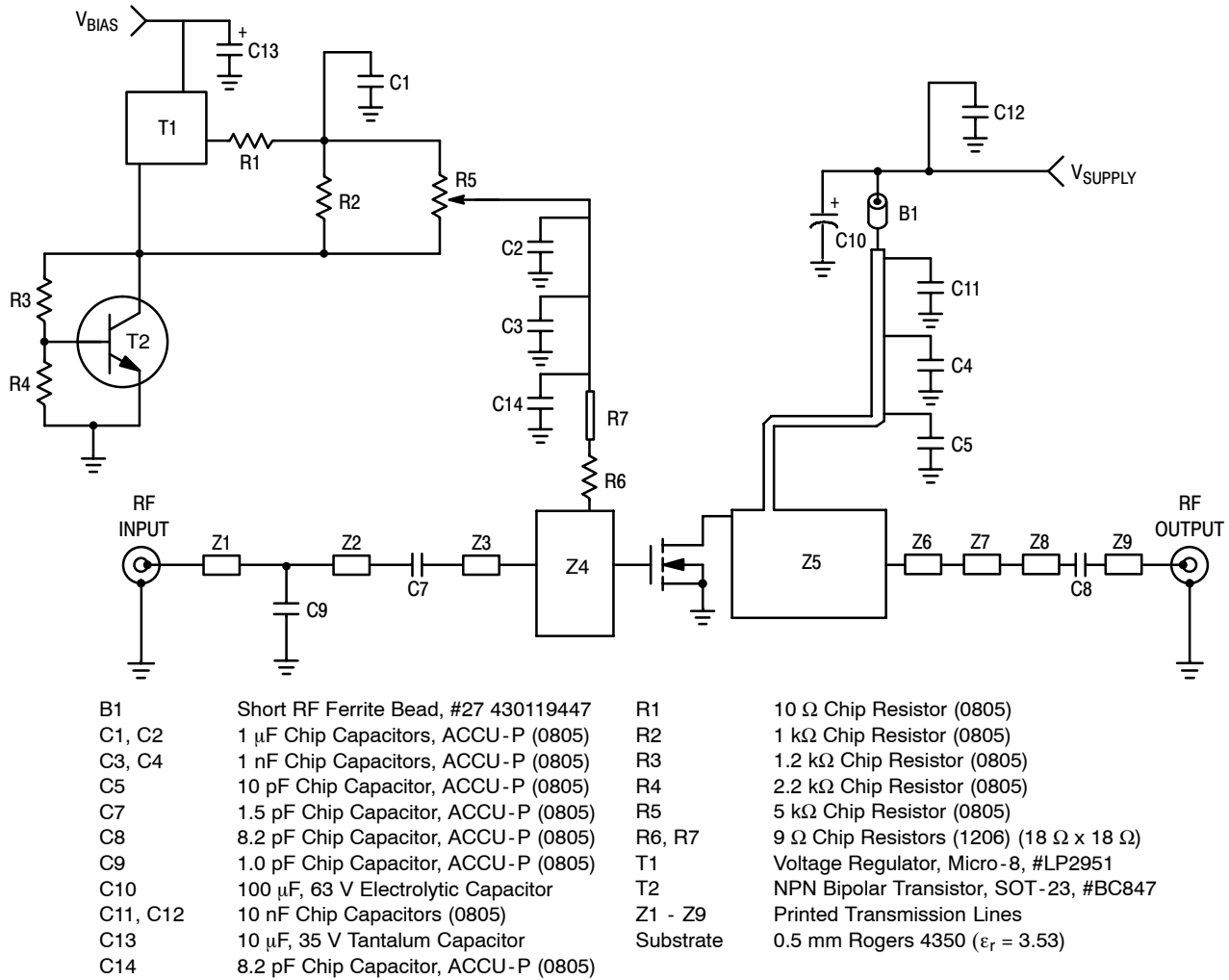
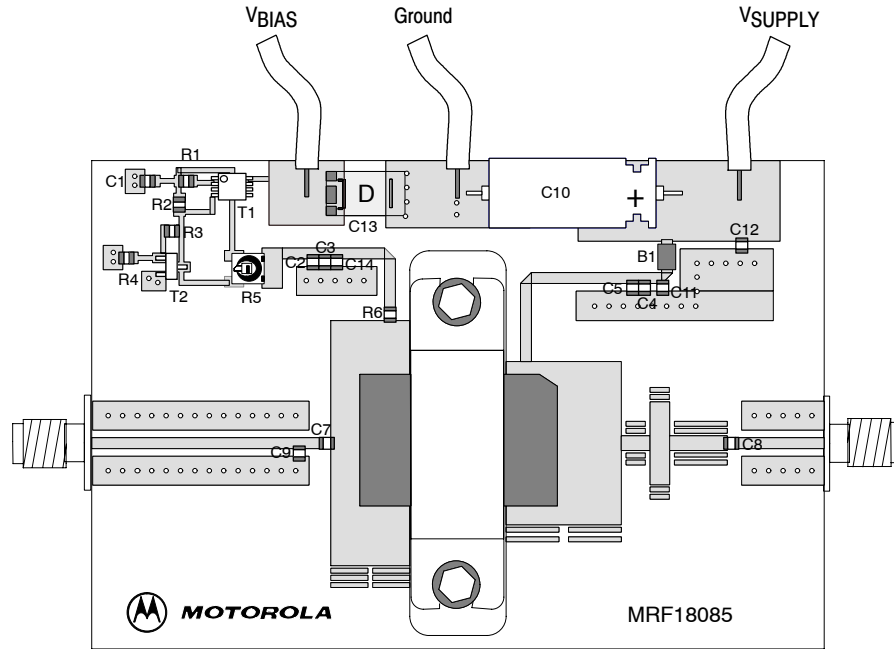


Figure 3. 1930 - 1990 MHz GSM EDGE Optimized Demo Board Schematic



Freescale has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescale Semiconductor signature/logo. PCBs may have either Motorola or Freescale markings during the transition period. These changes will have no impact on form, fit or function of the current product.

Figure 4. 1930 - 1990 MHz GSM EDGE Optimized Demo Board Component Layout

TYPICAL CHARACTERISTICS
(Performed on a GSM EDGE Optimized Demo Board)

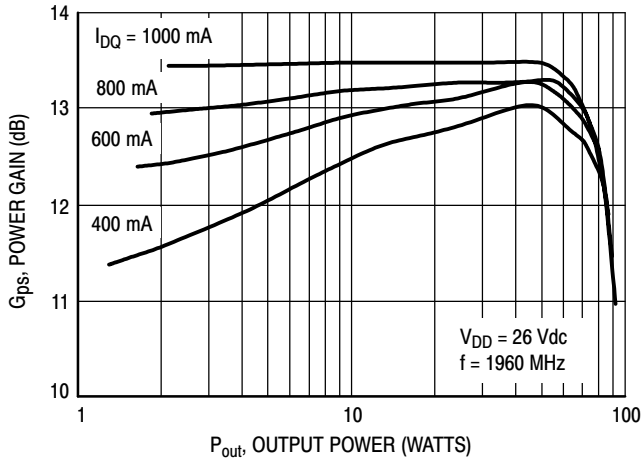


Figure 5. Power Gain versus Output Power

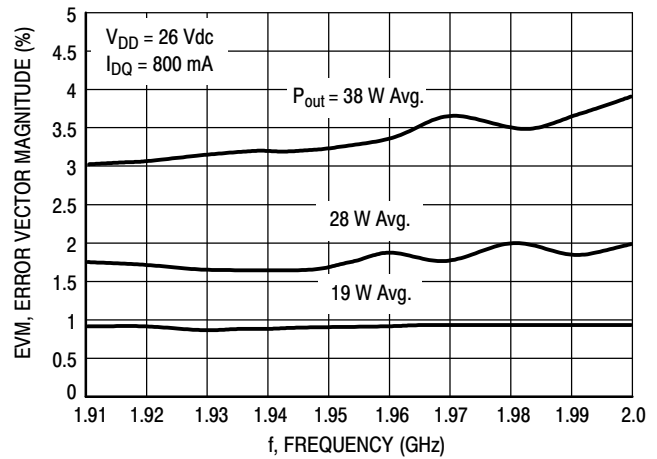


Figure 6. Error Vector Magnitude versus Frequency

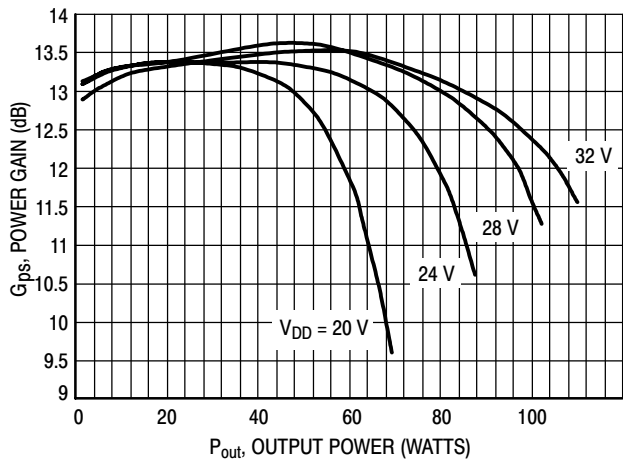


Figure 7. Power Gain versus Output Power

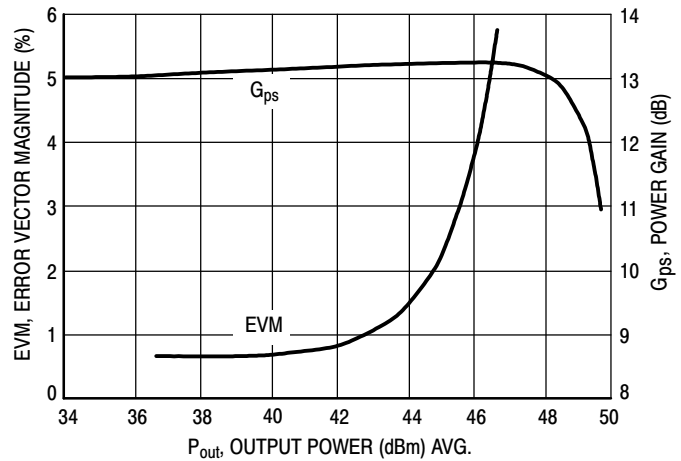


Figure 8. EVM and Gain versus Output Power

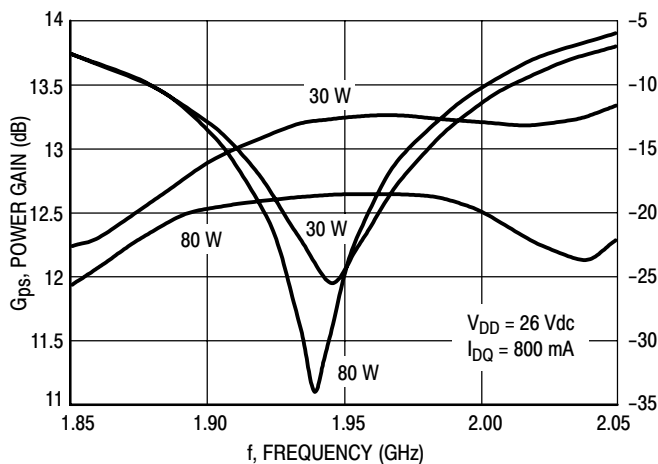


Figure 9. Power Gain and IRL versus Frequency

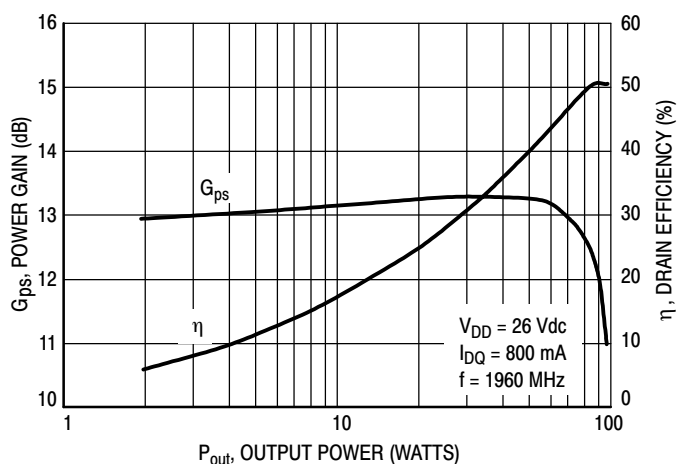


Figure 10. Power Gain and Efficiency versus Output Power

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GSM TEST SIGNAL

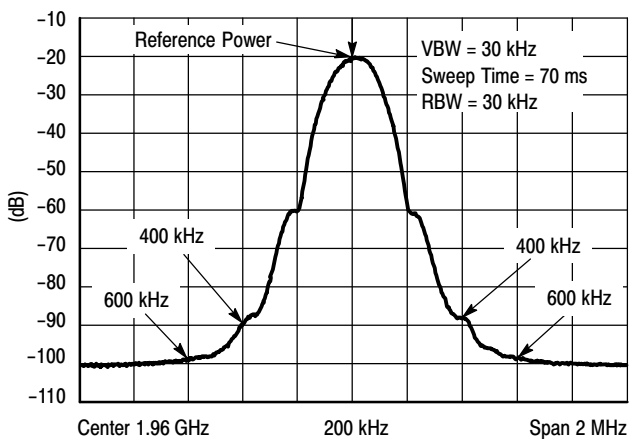
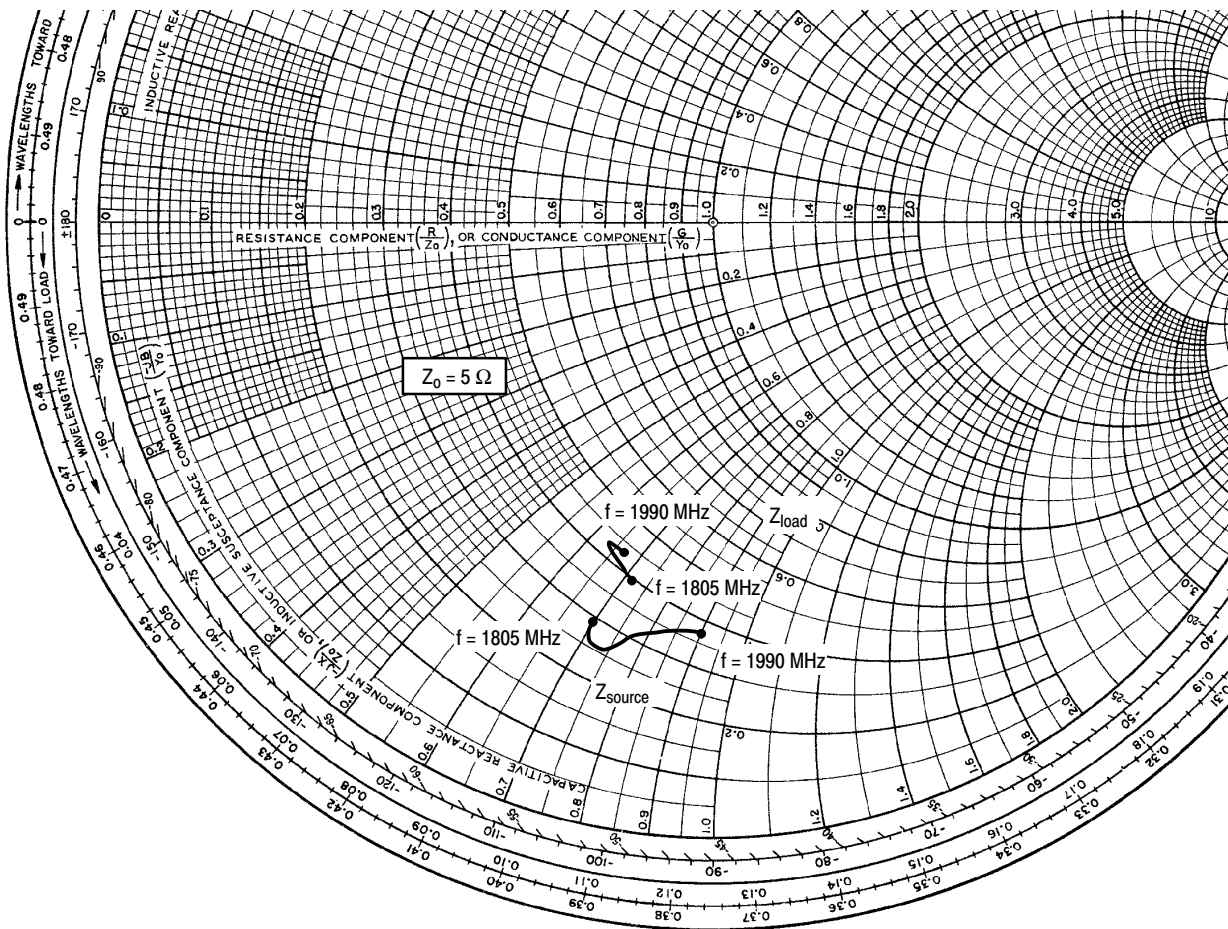


Figure 11. EDGE Spectrum

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$V_{DD} = 26\text{ V}$, $I_{DQ} = 800\text{ mA}$, $P_{out} = 85\text{ W CW}$

f MHz	Z_{source} Ω	Z_{load} Ω
1805	$1.43 - j3.74$	$2 - j3.60$
1880	$1.27 - j3.95$	$1.98 - j3.57$
1930	$1.5 - j4.13$	$2.13 - j3.16$
1990	$1.86 - j4.76$	$2.17 - j3.36$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

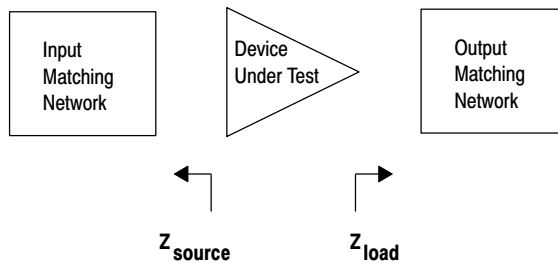


Figure 12. Series Equivalent Source and Load Impedance

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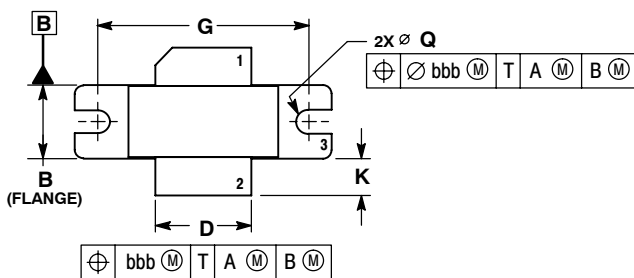
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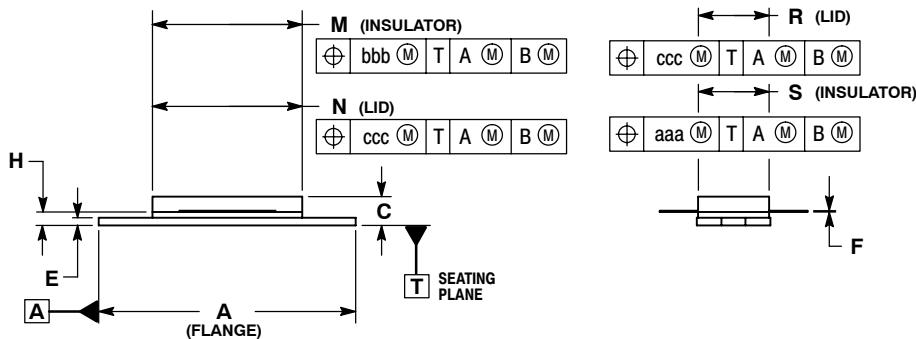
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PACKAGE DIMENSIONS



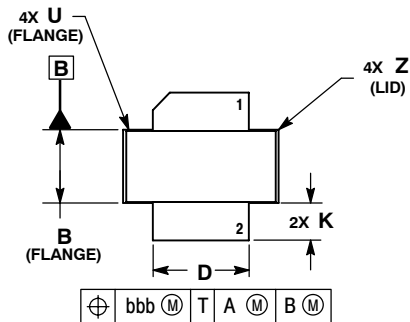
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
 2. CONTROLLING DIMENSION: INCH.
 3. DELETED
 4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC		27.94 BSC	
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.66	19.96
N	0.772	0.788	19.60	20.00
Q	∅.118	∅.138	∅3.00	∅3.51
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	



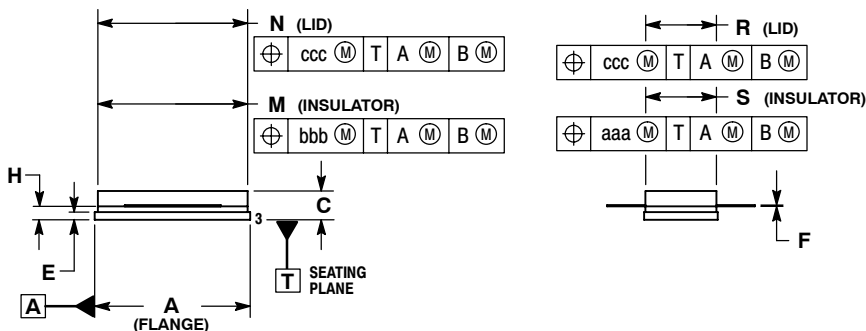
- STYLE 1:
 PIN 1. DRAIN
 2. GATE
 3. SOURCE

**CASE 465-06
 ISSUE G
 NI-780
 MRF18085BLR3**



- NOTES:
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DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.805	0.815	20.45	20.70
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.61	20.02
N	0.772	0.788	19.61	20.02
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
U	---	0.040	---	1.02
Z	---	0.030	---	0.76
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	



- STYLE 1:
 PIN 1. DRAIN
 2. GATE
 5. SOURCE

**CASE 465A-06
 ISSUE H
 NI-780S
 MRF18085BLSR3**

MRF18085BLR3 MRF18085BLSR3

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