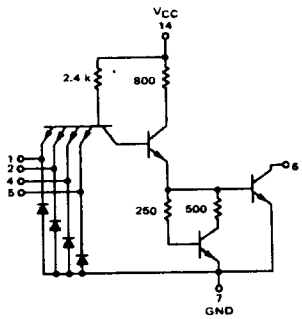
DUAL 4-INPUT "NAND" GATE
(Open Collector)

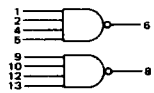
MC3112F • MC3012F
MC3112L • MC3012L,P

(54H22J) (74H22J,N)

1/2 OF CIRCUIT SHOWN



This device consists of two 4-input NAND gates with no output pull-up circuits. It can be used where the Wired-OR function is required or for driving discrete components.

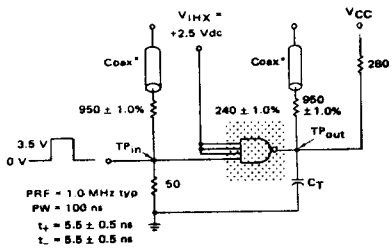


Positive Logic: $6 = \overline{1 \cdot 2 \cdot 4 \cdot 5}$
Negative Logic: $6 = \overline{1 + 2 + 4 + 5}$

Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 44 mW typ/pkg
Propagation Delay Time = 8.0 ns typ

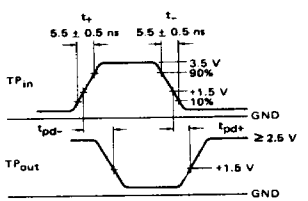
SWITCHING TIME TEST CIRCUIT



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

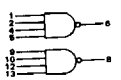
VOLTAGE WAVEFORMS AND DEFINITIONS



See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



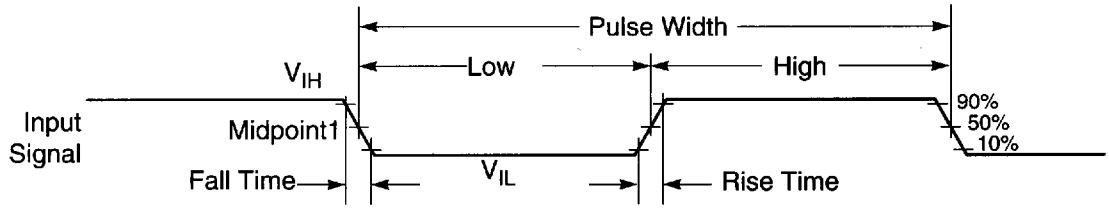
Characteristic	Symbol	Pin Under Test	MC3112 Test Limits −55°C Min	MC3112 Test Limits −55°C Max	MC3112 Test Limits +25°C Min	MC3112 Test Limits +25°C Max	MC3112 Test Limits +125°C Min	MC3112 Test Limits +125°C Max	MC3012 Test Limits 0°C Min	MC3012 Test Limits 0°C Max	MC3012 Test Limits +25°C Min	MC3012 Test Limits +25°C Max	MC3012 Test Limits +75°C Min	MC3012 Test Limits +75°C Max	Unit	@ Test Temperature	I_{OL} (mA)	I_{in} (mA)	I_D (mA)	V_R (Volts)	V_{BH} (Volts)	V_P (Volts)	V_E (Volts)	V_{BH} (Volts)	V_{CEX} (Volts)	V_{max} (Volts)	V_{CC} (Volts)	V_{CC1} (Volts)	V_{CCH} (Volts)	V_{BIX} (Volts)	Gnd
Input Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	mAdc	MC3112 −55°C	20	-	-	1.1	2.0	0.4	2.4	4.0	5.5	-	5.0	4.5	5.5	-	7*
Leakage Current	I_R	1	-	50	-	50	-	50	-	50	-	50	-	50	µAdc	MC3112 +25°C	20	1.0	-10	1.1	1.8	0.4	2.4	4.0	5.5	7.0	5.0	4.5	5.5	2.5	2,4,5,7*
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	MC3112 +125°C	20	-	-	0.8	1.8	0.4	2.4	4.0	5.5	-	5.0	4.75	5.25	-	2,4,5,7*
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	MC3012 0°C	20	-	-	1.1	2.0	0.4	2.5	4.0	5.5	7.0	5.0	4.75	5.25	2.5	7
Output Output Voltage	V_{OL}	6	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	MC3012 +25°C	20	1.0	-10	1.1	1.8	0.4	2.5	4.0	5.5	-	5.0	4.75	5.25	-	7*
Output Leakage Current	I_{CEX}	-	-	250	-	250	-	250	-	250	-	250	-	250	µAdc	MC3012 +75°C	20	-	-	0.9	1.8	0.4	2.5	4.0	5.5	-	5.0	4.75	5.25	-	7*
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	12.5	-	-	-	-	-	12.5	-	-	mAdc																
Power Supply Drain	I_{PDH}	14	-	18	-	18	-	18	-	18	-	18	-	18	mAdc																
	I_{PDL}	14	-	6.0	-	6.0	-	6.0	-	6.0	-	6.0	-	6.0	mAdc																
Switching Parameters Turn-On Delay	t_{pd-}	1,6	-	-	-	14	-	-	-	-	-	14	-	-	ns		Pulse In	Pulse Out													
Turn-Off Delay	t_{pd-}	1,6	-	-	-	20	-	-	-	-	-	20	-	-	ns		1	6	-	-	-	-	-	-	-	-	14	-	-	2,4,5	7*
																	1	6	-	-	-	-	-	-	-	-	14	-	-	2,4,5	7*

TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:

*Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

AC ELECTRICAL CHARACTERISTICS

The timing waveforms in the AC Electrical Characteristics are tested with a V_{IL} maximum of 0.5 V and a V_{IH} minimum of 2.4 V for all pins, except EXTAL, $\overline{\text{RESET}}$, MODA, MODB, and MODC. These pins are tested using the input levels set forth in the DC Electrical Characteristics. AC timing specifications that are referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal's transition. DSP56002 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.8 V and 2.0 V, respectively.



Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

AA0179

Figure 2-1 Signal Measurement Reference